Workshop on Low Power Design Impact on Test and Reliability

Grand Hotel Magestic, Pallanza, Lago Maggiore, Italy
Thursday, May, 29, 2008

Fringe to

General Chairs:

Alex Bystrov – Newcastle Univ. (UK)
J. Paulo Teixeira – IST / INESC-ID (P)

Invited Presentations:

Tom W. Williams,
Synopsys Fellow (USA)
"Moore's/Dennard Law and Low Power Techniques"

***Sandip Kundu*,**
Univ. Massachusetts at Amherst (USA)
"Emerging trends in nano-silicon systems and their implications on design and test"

***Kaushik Roy*,**
Purdue Univ. (USA)
"Power dissipation and process variation in Nanoscale CMOS design: test challenges and solutions"

Bashir Al-Hashimi*, *Peter Harrod
Southampton Univ., ARM (UK)
"Impact of adaptive energy management on DFT"

Janusz Rajski,
Mentor Graphics Corp. (USA)
"Power-aware DFT"

Tobias Bjerregaard,
CEO Teklatech (Denmark)
"Timing variability and noise margins: will scaling kill the guardbands?"

Enrico Macii,
Politecnico di Torino (Italy)
"Thermal-aware design"

Call for Papers

The *Low Power Design Impact on Test and Reliability (LPonTR)* workshop aims to bring together design, reliability and test engineers and researchers to discuss the impact of advanced low-power / low voltage design methodologies of nanometer silicon systems on test and reliability. Power and thermal issues, leakage, process variations, enhanced susceptibility to environmental and operation-induced disturbances are physical constraints that drive the need to the development of low-power, process-tolerant design techniques. However, these techniques generate a new set of test and reliability challenges, questing for an innovative set of methodologies and tools.

You are invited to participate and submit your contributions to LPonTR'08. Papers are invited that address both current trends, challenges and proposed solutions in the (but are not limited to) following areas:

- *Power and process variations aware design and test*
- *Challenges of Ultra Low-power design on test and reliability*
- *Design for Variability at different levels of abstraction and its effect on testing*
- *Reliability issues in silicon products on bellow 45 nm technologies*
- *Delay testing for high-performance, low-power products*
- *Signal integrity in test mode*
- *Statistical and parametric test*
- *Test and performance of physical on-chip infrastructures (power grid, clock generation and distribution nets, power management modules, test compression/decompression modules)*
- *Dynamic BIST and scan design for LP, process tolerant products*
- *Test and reliability issues in the presence of leakage*
- *Defect modelling, fault simulation and ATPG for emerging failure modes*
- *Discriminating physical defects from noise and uncertainty*
- *Low-power, low-voltage design for testability (DfT)*
- *Analog and mixed-signal low-power design, test and DfT*
- *SoC test with power and thermal management techniques (e.g., DVS, multi-V_{th})*
- *Test and reliability of highly dependable, redundant systems*
- *Asynchronous design and test*
- *EDA tools to support LP, process-tolerant design*

Publications – The organising committee invites authors to submit extended abstracts in the above areas. Accepted extended abstracts will be published in the informal proceedings of the workshop. Selected submissions will be invited for publication as full papers in the *Journal of Low Power Electronics (JOLPE).*

All attendees are encouraged to prepare posters either in addition to the oral presentation or as the main form of presentation. The combination of the poster session with discussion of challenges and the closing panel will invite informal communication and facilitate networking.

Submissions – *Format for extended abstracts*: 2 pages in the IEEE conference layout or latex8, font 10, two columns, paper A4, page numbering – none. Approximate dimensions: left/right margin 20mm, top/bottom margin 30mm, column separation 10mm.

Format for posters: space for A0-portrait will be provided.

Authors should submit their contributions to **a.bystrov@newcastle.ac.uk** by the submission date below. Notification will be sent out by April 14th, 2008.

Key Dates:

- Submission deadline : **March 31, 2008 (extended)**
- Notification of acceptance : **April, 14, 2008**
- Final manuscript (electronic format) : **April, 28, 2008**

Further Information:

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