Second International Workshop on

the Impact of Low−Power Design on Test and Reliability

(fringe to ETS 2009)

Proceedings

LPonTR 2009

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NH Central Convenciones, Seville, Spain

Statement of Aims:

The International Workshop on Impact of Low Power Design on Test and Reliability (LponTR) aims to bring together design, reliability and test engineers and researchers to discuss the impact of advanced low-power low-voltage design methodologies of nanometer silicon systems on test and reliability. Power and thermal issues, leakage, process variations, susceptibility to environmental and operation-induced interference are physical constraints that drive the development of low-power, process-tolerant design techniques. However, these techniques generate a new set of test and reliability challenges, questing for an innovative set of methodologies and tools.

Topics include, but not limited to the following list:

- Power and process variations aware design and test
- Challenges of Ultra Low-power design on test and reliability
- Design for Variability at different abstraction levels and its effect on testing
- Reliability issues in silicon products on bellow 45 nm technologies
- Delay testing for high-performance low-power products
- Signal integrity in test mode
- Test and performance of physical on-chip infrastructures (power grid, clock distribution nets, etc.)
- Dynamic BIST and scan design for LP, process tolerant products
- Test and reliability issues in the presence of leakage
- Defect modelling, fault simulation and ATPG for emerging failure modes
- Discriminating physical defects from noise and uncertainty
- Low-power, low-voltage DfT
- Analog and mixed-signal low-power design, test and DfT
- Test of SoC with power and thermal management (e.g., DVS, multi-Vth)
- Test and reliability of highly dependable, redundant systems
- Asynchronous design and test EDA tools to support LP, process-tolerant design

Statistical and parametric test

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2nd International Workshop on the Impact of Low Power design on Test and Reliability (LPonTR)

NH Central Convenciones, Seville, Spain
Friday, May, 29, 2009

LPonTR'09 Programme

8:15 – 9:00 Registration

9:00 – 9:20 Opening Remarks (*A. Bystrov, P. Girard*)

9:20 – 10:10 Keynote 1: *Are you using the right low-power test methodology?*
Mark Kassab, Mentor Graphics, USA

--------- Coffee break ---------

10:30 – 11:45 Regular papers

- ***S. Eggersglüß, D. Tille, R. Drechsler***
  A Two-Stage SAT-based ATPG Approach with Reduced Switching Activity
- ***R. Kothe***
  Simultaneous Reduction of Test Data and Switching Activity for Transition Delay Tests
- ***J. Freijedo, L.Costas, J. Semião, J.J. Rodríguez-Andina, M.J.Moure, F.Vargas, I.C.Teixeira, J.P.Teixeira***
  Delay Modeling for Power Noise-Aware Design and Test in 65nm FPGAs

11:50 – 12:40 Embedded Tutorial 1: *Test of power supply noise – causes, effects and testing*
Ilia Polian, University of Freiburg, Germany

13:00 – 14:30 **--------- Lunch ---------**

14:30 – 15:00 Keynote 2: *Defects and Margins in Low Voltage Memories*
Rob Aitken, ARM, USA

15:00 – 15:50 Regular papers

- ***I. Pomeranz, S. M. Reddy***
  Test Sequences with Reduced and Increased Switching Activity
- ***F.Wu, L.Dilillo, P.Girard, S.Pravossoudovitch, A.Virazel, A.Bosio, X.Wen***
  Trade-off between Power Dissipation and Delay Fault Coverage For LOS and LOC Testing Schemes

--------- Coffee break ---------

16:10 – 16:30 Keynote 3: *Low-power and the future of IDDQ testing*
Hans Manhaeve, Q-Star Test nv, Belgium

16:30 – 17:00 Embedded Tutorial 2**:** *Effects of IR-drop on VLSI testing and the impact on test generation and parametric test*
Xiaoqing Wen, Kyushu Institute of Technology, Japan

17:00 – 17:10 Closing Remarks (*A. Bystrov, P. Girard*)

Keynote 1: Are you using the right low-power test methodology?

Mark Kassab, Mentor Graphics, USA

Abstract:
Power has become one of the main concerns on the minds of test engineers. Excessive power consumption during capture increasingly compromises the value of at-speed test, and consequently a product's profit margins. Static power management methods introduce new challenges to achieving high quality goals. Several options with different trade-offs exist to deal with those challenges. As will be discussed, choosing the right methodology requires understanding what problems are being addressed, what is being tested, and what power conditions are required.

Keynote 2: Defects and Margins in Low Voltage Memories

Rob Aitken, ARM, USA

Abstract:
The distinction between defects and parametric variation in nanometer designs is becoming difficult to quantify in nanometer technologies. Low voltage operation adds another layer of complexity to the subject. Specific examples are given for SRAM operation. The implications of these on other circuits of interest are discussed.

Embedded Tutorial 1: Test of power supply noise – causes, effects and testing

Ilia Polian, University of Freiburg, Germany

Abstract:
Current trends in power density and voltage scaling imply a 225% increase in current per unit area for each new technology generation. Noise originating from the power grid increasingly disturbs the operation of integrated circuits. The resulting delay faults have complex activation conditions and are not screened out by conventional transition, gate-delay and path-delay patterns.

The tutorial will provide background information on low-frequency and high-frequency effects of power-grid related noise (sometimes called power integrity). It is possible to translate these effects to the circuit level, which enables the generation of test sequences that are able to identify power integrity issues. The generated patterns need to be sequential even for scan designs. We will present one approach to generate power integrity test sequences based on D-algorithm enriched by on-the-fly constraint generation. The obtained patterns can be used for manufacturing testing as well as for early silicon validation.

A Two-Stage SAT-based ATPG Approach with Reduced Switching Activity

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I. Introduction

Due to the rising performance and decreasing feature sizes of today's designs, the likelihood of delay defects increases. Therefore, transition fault testing is widely used to ensure that the delivered chips are free of fabrication defects. Due to the use of scan testing, the switching activity in the *Circuit Under Test* (CUT) is typically several times higher than during normal functional operation [1], [2]. This may lead to additional yield loss or even affect the reliability when "good" chips are exposed to excessive switching activity, which does not occur in normal operation mode. Common ATPG algorithms typically do not consider switching activity during test pattern generation for reasons of efficiency. However, in [3], a modified PODEM algorithm is applied to reduce the switching activity during test generation. In [4], power constraints are added to the circuit during test generation.

Recently, ATPG based on *Boolean Satisfiability* (SAT) has shown to be an efficient and robust alternative to classical ATPG algorithms [5]. A significant advantage of SAT-based algorithms is the powerful conflict analysis and the use of learned information.

In this paper, we present the concept of a SAT-based ATPG approach to generate tests with reduced switching activity between the launch cycle and the capture cycle. The approach consists of two consecutive stages. In the first stage, a normal transition fault test is generated. If the targeted fault is testable, the SAT instance is extended incrementally in the second stage to generate a test with reduced switching activity. In order to maintain a high fault coverage, a relaxation technique is described for the second stage.

II. SAT-based ATPG

State-of-the-art SAT solvers typically work on a Boolean formula represented in *Conjunctive Normal Form* (CNF). A CNF is a conjunction of clauses. A clause is a disjunction of literals and a literal is a Boolean variable in its positive form (x) or negative form ($\overline{x}$). To apply a SAT solver to a circuit-oriented problem, e.g. ATPG, the circuit has to be modeled in CNF. In the following, Φ_C corresponds to the CNF of circuit C. For generating a test for fault F, the fault specific constraints Φ_{FS} have to be added to Φ_C. Finally, information concerning the potential propagation paths, i.e. D-chains, – denoted by Φ_D – is added. Therefore, the CNF $\Phi_F = \Phi_C \wedge \Phi_{FS} \wedge \Phi_D$ describes the ATPG problem for some fault F in a circuit C. For more information on circuit-to-CNF transformation and fault modeling, we refer to [5].

In the following, we concentrate on transition faults. Evaluating the CNF Φ_F results in either untestability (if Φ_F is unsatisfiable) or in a test (if Φ_F is satisfiable). Here, the test is directly derived from the computed solution.

When generating delay tests, two time frames t_1, t_2 have to be considered. This is achieved by duplicating the circuit. Each copy represents one time frame. Consequently, a signal s is represented by two Boolean variables s^1, s^2, which describe the signal in the corresponding time frame. The behavior of the flip-flops is modeled by connections between both copies.

III. Encoding of Static Values

The representation of a signal with two Boolean values as used in common SAT-based ATPG approaches has the drawback that the absence of switching activity cannot be guaranteed. For example, consider a 2-input AND gate g. If both inputs switch in different directions, the Boolean representation causes that the output value of g remains 0 in t_1, t_2. This is because the controlling value 0 is assumed at one input in each time frame. The controlling value of a gate is the logic value, which, when assumed by one input, determines the output's value regardless from the value of other inputs. However, if the transitions on the inputs do not arrive simultaneously, a glitch is produced at the output which cannot be observed using the Boolean values.

For guaranteeing the absence of switching activity (transition and glitches) or manipulate the amount of switching activity, static values have to be encoded. This can be done by assigning a third variable s^s to signal s. The variable s^s determines whether the signal is static between t_1 and t_2 or not. Additional constraints have to be added to the SAT instance for the computation of static values. Given a gate g with inputs $i_1, \ldots, i_n$, the controlling value *cv* and the non-controlling value *ncv*. If g is static and assumes *ncv*, then $i_1, \ldots, i_n$ must be static, too. If g is static and assumes *cv*, then at least one input i_j with $1 \leq j \leq n$ must assume *cv*. formally, the following

These implications can be transformed into CNF and are denoted by Φ_S in the following. The CNF Φ_S is logically redundant, i.e. the solution space concerning the number of tests remains the same. However, due to the this formulation, the static signals can be identified and manipulated as shown in the next section. The advantage of this encoding is that it can be incrementally added to the SAT instance and thus, all learned information can be kept. The effectiveness of using this information in subsequent solving process was shown for example in [6].

IV. Two-Stage Approach

Here, the overall two-stage approach is described. The pseudo-code is presented in Algorithm 1. At first, transition fault test generation is performed as usual (first stage; lines 1-5). If the fault is untestable, the second stage is not entered. If the fault is testable, the second stage is started to find a test which is likely to have reduced switching activity. Therefore, the SAT instance Φ_F is augmented by the static value encoding Φ_S resulting in Φ_{SF} (line 7). As major benefit, the information learned so far during the search process is still valid and can therefore be applied in the second stage to exclude illegal signal value assignments.

To generate a test for fault F, the fault must be excited at the fault site and then be propagated to an observation point. The handling of the off-path inputs is crucial for the generation of a test with reduced switching activity. An off-path input is a signal that drives a gate on a propagation path, i.e. on a D-chain, but is itself not located on this path. Normally, the off-path inputs of the D-chain are only constrained to propagate the fault effect. But often, a large part of the combinational logic of the circuit is needed to justify the off-path inputs. Therefore, the goal is to increase the number of static off-paths inputs to reduce the overall switching activity.

This can be done by additional constraints. Consider a gate g with inputs $i_1, \ldots, i_n$. If, and only if, input i_j is on a D-chain, all other inputs have to assume static values to reduce the switching activity. The resulting implications in CNF are denoted by Φ_O. Then, the SAT instance consisting of Φ_{SF} and Φ_O is solved (including the learned information from the first stage; line 9). If the SAT instance is satisfiable, a test is found which is very likely to have reduced switching activity due to the static off-path inputs.

However, restricting the off-path inputs to static values results in a decreased fault coverage, because some faults may become untestable due to Φ_O. To keep the fault coverage high, a relaxation procedure is proposed for Φ_O. Because F was originally testable, the source of the unsatisfiability has to be in Φ_O. An *unsatisfiable core* [7] is therefore generated and used to pinpoint the source of the unsatisfiability. Afterwards, Φ_O can be relaxed according to the unsatisfiable core (line 11), i.e. some off-paths inputs do not have to assume static values. Then, the alternated SAT instance is solved again (lines 10-13) until a test is found. In the worst case, Φ_O is completely discarded. As an alternative to save run time, the test generated in the first stage can be directly used after the first iteration.

V. Preliminary Results

Table I shows the first results of a rough prototypical implementation for generating restricted broadside tests (without the relaxation technique). Here, the test from the first stage is taken if the second stage determines unsatisfiability. As measurement for switching activity, the number of switching gates was chosen. Column *Av. Sw.* shows the average number of switching gates for one test. The maximum number of switching gates per test is shown in column *Peak*. The average reduction of the number of switching gates is presented in column *Av. red. %*. The potential of the approach can clearly be seen. Here, the maximum switching activity is significantly reduced.

Algorithm 1 Pseudo-code of the two-stage approach

1: Select_Transition_Fault F;
2: Generate Φ_F;
3: Solve Φ_F;
4: **if** Φ_F = UNSAT **then**
5:    **return** UNTESTABLE
6: **else**
7:    $\Phi_{SF} = \Phi_F \wedge \Phi_S$;
8:    Generate Φ_O;
9:    Solve $(\Phi_{SF} \wedge \Phi_O)$;
10:    **while** $\Phi_{SF} \wedge \Phi_o$ = UNSAT **do**
11:       Relax Φ_O;
12:       Solve $\Phi_{SF} \wedge \Phi_O$;
13:    **end while**
14: **end if**
15: **return** Test T;

TABLE I
EXPERIMENTAL RESULTS - NUMBER OF SWITCHING GATES

	Classic			Two-stage			
Circ	Av. Sw.	Peak	time	Av. Sw.	Peak	time	Av. red.
b04	122.7	375	0:02m	101.0	292	0:03m	10.9%
b13	26.1	99	0:01m	22.2	72	0:01m	8.1%
b14	1067.7	5380	3:20m	656.1	4050	5:26m	32.8%
b15	924.3	2816	4:42m	691.7	2291	7:11m	17.2%

Furthermore, the number of switching gates is decreased as well by up to 32.8%. At the same time, the run time overhead is moderate.

VI. Conclusions and Outlook

We presented the concept for a two-stage SAT-based ATPG approach for generating tests with reduced switching activity. Constraints for reducing switching activity are added in an incremental manner so that learned information from the first stage can be reused in the second stage to improve the efficiency. First results have shown the potential of this approach.

So far, the approach considers only off-path inputs of the propagation paths. Future work is the extension of the concept to the off-path inputs of the activation path. Furthermore, the approach will be evaluated with other measurements, e.g. weighted switching activity.

References

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Simultaneous Reduction of Test Data and Switching Activity for Transition Delay Tests

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1 Introduction

Test technologies for integrated circuits are mainly based on massive parallel scan tests [1], because their high compaction rates are essential for keeping test costs low. However, power consumption is one point which is not addressed by most of these architectures [1,2]. Too much power consumption may result in thermal stress for the device and increased voltage drops on VDD / GND rails, which implies higher signal delays. And thus good devices could fail during delay testing.
In the following a technique is described, which simultaneously reduces the capture power during Launch-Off-Capture-based delay testing and provides further test data compaction. The first functional cycle ("launch") of this scheme sets up all relevant gates and generates the second vector. The second functional cycle ("capture") provokes the desired transitions and stores the relevant circuit behaviour within scan cells. Afterwards this test response is shifted-out, and the new first vector is shifted-in. Typically, the critical power consumption regarding transition delay testing belongs to the capture cycle, because this cycle works with a full-speed clock in contrast to the slow shift and launch cycles. Power consumption in CMOS consists of a dynamic and a static part. Dynamic power consumption in CMOS is proportional to transistor switching events. Weighted switching activity (WSA) metrics was proposed in [3] and is hereafter used as synonym for power consumption.

2 The Concept

Several modifications are needed to reduce the WSA for the capture cycle for a given test pattern. First, test pattern relaxation [4] has to be executed to get a pattern ($P_X=P_0...P_{n-1}$) with a high percentage of unspecified bits (X). This is essential for high compaction rates. Afterwards, these X bits are replaced by 0 or 1 with respect to the power-aware compaction technique to get the new low-power pattern P_{new}. Alternating run-length encoding was chosen as compaction technique, because it can reduce switching activity during scan mode [2] and it is easy to calculate. In general, a good measure for the compaction rate of alternating run-length encoding is the number of transitions ($trans_{Pnew}$) within the pattern P_{new} – a lower value means a better compaction.
Earlier publications for capture power reductions [5,6] used the observation that the correlation between WSA of a cycle and the Hamming distance of the flip flop states at the beginning and at the end of this cycle is high. Accordingly, the Hamming distance ($hamming_{LC}$) between flip flop states before ($L=L_0\ldots L_{n-1}$) and after capture cycle ($C=C_0\ldots C_{n-1}$) is an estimation for power consumption within capture cycle.
In the next step, estimations for compaction and power consumption are put together to make a cost function.

$$cost = weight_1 \cdot trans_{P_{new}} + weight_2 \cdot hamming_{LC}$$

If the cost function would only consist of the first part, then minimisation process would be very easy: compute adjacent filling for the pattern. But the second part is much more computational-intensive, because L and C are functional-dependent on P_{new}: $L:=f(P_{new})$ and $C:=f(L)=f(f(P_{new}))$. Accordingly, it should be hardly possible to calculate the exact minimum in the general case. In the following, a heuristic approach is proposed for creating a pattern P_{new} with low costs step-by-step from the relaxed pattern P_x by using a greedy algorithm.

2.1 Greedy Algorithm

At the beginning, the algorithm calculates the cost of the pattern P_x and stores P_x based on its cost and the number of unspecified bits into a two-dimensional data structure. Afterwards, the main program loop starts. It takes the currently best intermediate pattern and generates from this one two new patterns by replacing the next unspecified bit with 0 and for the second pattern with 1. Based on their costs (→ event-driven circuit simulation) these patterns are also stored in the data structure and replace the old pattern. The second dimension is needed, if there are several patterns generated with the same cost. The algorithm prefers the pattern with the least number of unspecified bits, because the "way" to the fully specified pattern P_{new} is shorter. The algorithm ends when the best intermediate pattern has no unspecified bits. This pattern becomes P_{new}. The remaining patterns are deleted. The number of intermediate pattern is at least twice the number of unspecified bits within the pattern. Therefore, a fast circuit simulation tool is needed to calculate the associated costs.

2.2 Event-driven Circuit Simulation

Early prototypes showed that, on the average, the chosen consecutive "best" intermediate patterns differ only by a few positions. In event-driven simulation, the circuit to be simulated is unrolled over time (t). Gate values for the necessary clock cycles have their own memory and can not be overwritten by later cycles of this simulation. This implies that every flip flop has three memories: For the pattern (time t_0), for the launch response (time t_1), and for the capture response (time t_2). Gates of combinational logic need only two memories: For the launch cycle (t_0 to t_1) and for the capture cycle (t_1 to t_2). The small difference between the last pattern and the current pattern leads in this event-driven simulation only to a few events (gate value toggles) in the unrolled circuit.

3 Results and Conclusions

Results are shown using ISCAS'89 and ITC'99 benchmark circuits. Fully specified test sets for transition delay faults were generated by a non-power-aware ATPG program and then relaxed [4]. All measurements were done on an Intel Xeon E5420 (2.5 GHz, 8 GB RAM) based system. At the moment, the whole program is single threaded. In table 1 the key numbers of these circuits and their relaxed test sets are given, together with compaction and computation time information.

Table 1: Key numbers of the used ISCAS'89 and ITC'99 circuits; compaction rates, and computation times

				MT Fill.	Proposed 8/2 w1=0.8 / w2=0.2			Prop. 2/8
Name	#Gates	#Pat.	% X	Rat.	Rat.	Time	T./Pat.	Rat.
S13207	11112	564	94%	4,6	3,6	5s	9 ms	1,9
S15850	12509	350	90%	2,7	2,4	3s	9 ms	1,4
S35932	24258	96	83%	2,2	2	2s	21 ms	1,4
S38417	29148	525	89%	3,8	3,2	15s	29 ms	2,2
S38584	26174	771	94%	4,2	3,3	36s	47 ms	2,0
B18	81515	5061	98%	13,9	11,6	940s	185 ms	8,4
B19	239422	7034	98%	20,5	15,7	5368s	763 ms	11,4
Avg.	60591	2057	92%	7,4	6,0	910s	152 ms	4,1

MT Filling (col. 5) was chosen as reference (best case) for the compaction rate with alternating run-length encoding [2]. For maximising the compaction rates (col. 5, 6 and 9), the code words for the run-lengths were optimally chosen (Huffman code). In table 1 (and also in table 2) are measurements for two different "strategies" of the proposed algorithm quoted: "8/2" and "2/8". These names describe the weightings within the cost function: "8/2" means weight1=0.8 and weight2=0.2 (2/8 → weight1=0.2 and weight2=0.8). That means strategy 8/2 optimises (more) for compaction and 2/8 optimises for power consumption. In col. 7 are the computation times of the greedy algorithm and the necessary circuit simulations shown. Because of the exponential character of the described greedy algorithm, the upper limit of entries per cost (second dimension) was set to 1. Limits of up to 10 would also be applicable, but there is a strong disproportion between rise of the computation time (up to 50) and compaction and power consumption improvements (few percents). Normally, other possible strategies needs about the same efforts (within 20% difference). It seems that the time per pattern (col. 8) rise with the square of the number of unspecified bits per pattern. Table 2 shows the level of switching activity (WSA) during capture cycles. Some of these values are much higher than the typical WSA level during functional mode. In this table, random fill values are used as references. Preferred Fill [5] and the derived Preferred Fill with Adjacent Fill [6] are very fast power-reduction techniques, which do not directly address compaction. I implemented these algorithms straightforward from [5, 6]. The numbers regarding power-reductions are not comparable with the references because of the complete different pattern sets. The last row ("Gain") shows the relative average improvement over random fill.

Table 2: Comparison of diff. power reduction techniques

	Rand. Fill		Pref. Fill		PF+AF		Prop. 8/2		Prop. 2/8	
	Avg	Peak	Avg	Peak	Avg	Peak	Avg	Peak	Avg	Peak
S13207	25%	33%	17%	30%	22%	32%	15%	30%	12%	29%
S15850	24%	32%	16%	28%	20%	28%	16%	28%	12%	24%
S35932	39%	44%	30%	41%	32%	42%	32%	41%	26%	39%
S38417	26%	32%	22%	31%	21%	30%	16%	28%	15%	27%
S38584	25%	39%	21%	38%	23%	39%	16%	36%	14%	33%
B18	10%	17%	7%	15%	8%	17%	7%	20%	5%	16%
B19	9%	15%	7%	15%	8%	15%	5%	16%	4%	13%
Gain	n/a	n/a	24%	6%	16%	5%	34%	4%	48%	14%

It could be summarised that compaction is successfully addressed with the new technique; something about 80 ("8/2") percent from the optimum value (MT filling) could be reached. Reductions of the average power consumption during capture cycle reach nearly 50 ("2/8") percent. The peak power consumption however, stays on a high level. The possible reasons are: a) weak correlation between Hamming distance and WSA metrics; b) low ratio of unspecified bits within a dedicated pattern; c) greedy algorithm "decided wrong"; d) even the relaxed test pattern is "power hungry". Possible solutions: a) could be solved by using WSA metrics directly for the optimisation; b) split pattern; c) different strategy or different parameters; d) create a new pattern based on power-aware ATPG [7]. Nevertheless, the proposed solution brings test set compaction and power consumption together. Depending on the general conditions (maximum allowed power consumption) the weightings should be carefully chosen.

References

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Delay Modeling for Power Noise-Aware Design and Test in 65nm FPGAs

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I. Introduction

THERE is a continuously increasing demand for lower power consumption and higher operating frequencies in digital systems. In addition, external or operation-induced disturbances may significantly affect circuit functionality or performance. These facts give rise to many challenging issues in the design and test of nanometer circuits. This work focuses on the effect of power supply disturbances on the propagation delays of digital circuits implemented in Field Programmable Gate Arrays (FPGAs), which are becoming the preferred choice of implementation, and even deployment in mass production quantities, in an increasing number of digital applications [1].

It has been recently shown that propagation delay variation models allow to efficiently supporting the design and test of low-power nanometer digital circuits [2]. Based on these models, design techniques have been proposed to increase the robustness of digital circuits to power supply disturbances [3][4]. The models have been extensively validated, mainly by simulation, in technologies down to 130nm.

Currently, FPGA devices fabricated in 65nm technologies are readily available. Due to their industrial significance, it is very interesting to model their behavior in the presence of power supply variations, in order to allow the aforementioned design and test techniques (targeting delay faults) to be implemented. Advantage can be taken of their reconfiguration capabilities to carry out extensive experimentation for modeling purposes. This work addresses the derivation of propagation delay variation models for two of the main components of such devices (i.e., lookup tables and interconnects). Results obtained in actual devices through electrical measurements are presented, demonstrating the validity of the models.

II. Propagation Delay Models for 65nm FPGAs

In order to deal with power supply variations using the target design and test techniques, it is necessary to accurately model path delays, which can be derived from gate delay models. The use of delay variation models (instead of absolute delay models) significantly reduces the computational load required to estimate delays. The gate-level expression that relates propagation delay variations (Δt_{pd}) with power supply voltage variations (ΔV_{DD}) is [6]:

$$\Delta t_{pd}(\Delta V_{DD}) = \psi' \cdot \frac{(1+\Delta V_{DD})(1-\alpha)^2}{(1+\Delta V_{DD}-\alpha)^2} - 1 \quad (1)$$

where Ψ' is empirically derived and $\alpha \approx V_{th0}/V_{DDnom}$ (empirical fitting around this value greatly improves accuracy).

Path delay variation (ΔT_{pd}) models can be obtained as the weighted summation of the Δt_{pd} of the gates in the path [7]:

$$\Delta T_{pd} = \Delta t_{pd_I} \cdot \sum_{i=1}^{n} p_i \cdot \left(1 + \varepsilon_i + k_i \cdot (1+\varepsilon_{i-1}) \cdot \frac{t_{pd0_{i-1}}}{t_{pd0_i}}\right) \quad (2)$$

where Δt_{pdI} models the propagation delay variation of the fastest transition of a reference inverter, ε_i compute the deviation of gate delay variations of logic gates relatives to Δt_{pdI}, p_i represent the contribution of each gate to the overall path delay in nominal operating conditions and k_i model the effect of slow inputs on gate delays.

The basic block diagram of an FPGA is shown in Fig. 1. It mainly consist of arrays of custom logic blocks (LBs) surrounded by a perimeter of I/O blocks, all of which can be assembled arbitrarily [5] by means of interconnect matrices (IM). In order to apply the models, it has to be taken into account that, in the target FPGAs (the most widely used), logic functions are implemented using SRAM-based lookup tables (LUTs), located inside the logic blocks. Therefore, the term t_{pdI} in Eq. (2) refers in this case to the behavior of a reference LUT. Logic paths consist of chains of logic blocks and interconnects.

A 65nm Cyclone III FPGA from Altera has been used to carry out electrical measurements in the experiments described below. In order to characterize the behavior of LUTs, logic blocks located close to I/O blocks have been used, to have balanced interconnect delays. The results obtained for the fastest output transition of the LUT are depicted in Fig. 2, where crosses represent maximum and minimum measured delays, and circles joined by the line represent the model obtained according to Eq. (1). In this experiment, the power supply voltage varies from its nominal value (1.2V) down to 0.8V. For lower values, functional collapse occurs. I/O blocks are supplied from a different source, so their behavior is not affected by the depletion of the supply voltage of the core.

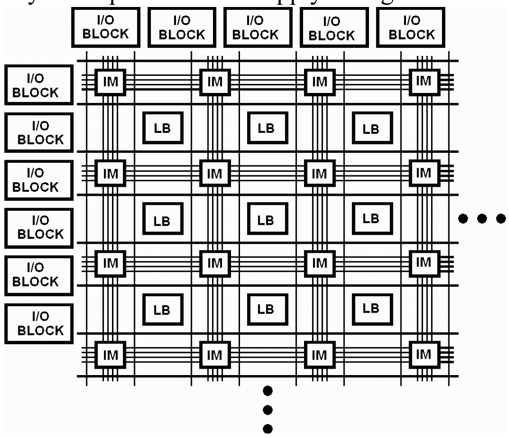

Fig. 1. FPGA concept.

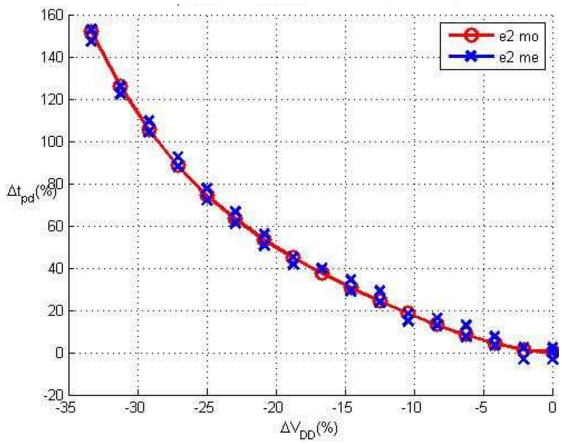

Fig. 2. Delay variations vs. power supply voltage variations in LUTs.

In order to obtain a model for interconnect delay variations, the previous experiment is repeated, but using an I/O block located far away from the logic block. Interconnect delays are estimated as the difference between the results of both experiments. The corresponding model is shown in Fig. 3.

A third experiment has been carried out to validate the path delay model defined by Eq. (2). In this case, two logic blocks located in the inner part of the device have been used. One interconnect connects both blocks, and another two connect each one of them to I/O blocks. The corresponding results are shown in Fig. 4.

The maximum error of the models for all experiments is below 5%, and the average value is below 3%.

These results point to the suitability of the models to be applied in FPGAs. The next steps of the work will be:

1) To carry out additional experiments for characterizing the behavior of other resources of the devices (e.g., flip-flops).

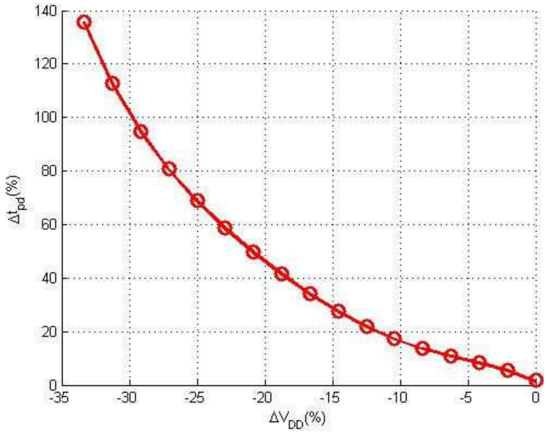

Fig. 3. Delay variations vs. power supply voltage variations in interconnects.

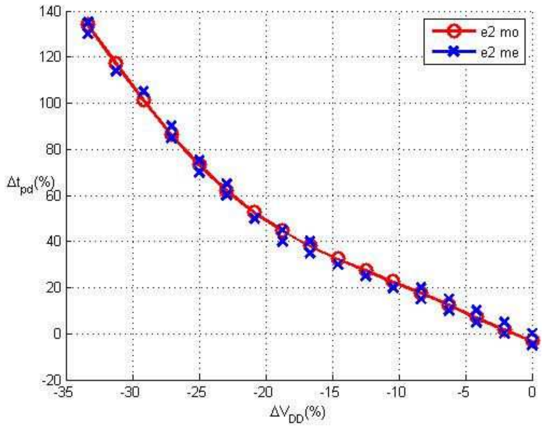

Fig. 4. Delay variations vs. power supply voltage variations in a path.

2) To extensively characterize resources located in different areas of the devices, to evaluate the effect of process variations.

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Test Sequences with Reduced and Increased Switching Activity
Extended Abstract

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1. Introduction

Scan-based tests are commonly used since the computational effort for producing a scan-based test set is manageable, and the tests achieve high fault coverage. The scan operation at the beginning of a scan-based test brings the circuit into a known state, from which target faults can be detected. The scan-in state may or may not be one that the circuit can enter during functional operation, also called a reachable state. It was shown in [1]-[2] that scan-based tests for delay faults, where the scan-in state is an unreachable state, can lead to overtesting, or unnecessary yield loss, where good chips may fail a delay test. In [1], overtesting is related to the detection of faults that do not affect the correct functional operation of the circuit. In [2], overtesting is related to the creation of peak switching activity that is higher than the peak switching activity during functional operation. When the resulting current demands cannot be met, a good chip may fail a test. The possibility that scan-based tests will result in overtesting motivated the development of functional [3]-[4] and pseudo-functional [5]-[6] scan-based tests. Functional scan-based tests use only reachable states as scan-in states. Thus, they guarantee that the circuit will traverse only reachable states during the functional clock cycles of the test. It also motivated the development of procedures for generating scan-based test sets with low switching activity, for example, [2] and [7]-[12].

A functional test sequence is applied to the circuit in its functional mode of operation, without using scan. Functional test sequences are used as manufacturing tests for speed binning. They were also shown to detect unique defects that scan-based tests do not detect [13]. Functional test sequences avoid overtesting by completely avoiding non-functional operation conditions. In particular, a fault that does not affect the correct functional operation of the circuit cannot be detected by a functional test sequence. In addition, both the peak and the average switching activity obtained during the application of a functional test sequence are guaranteed not to exceed those possible during functional operation. In this regard, functional test sequences have an advantage over functional scan-based tests since they do not include any scan operations that imply non-functional operation or observation of fault effects that cannot be observed during functional operation.

Due to the advantages of functional test sequences, it is beneficial to explore functional test sequences with increased switching activity as a way to maximize defect detection. A functional test sequence with a higher switching activity exercises more circuit lines, and is thus likely to activate and detect more defects or exhibit more reliability issues. Since the switching activity is guaranteed not to exceed that during functional operation, increasing the switching activity of a functional test sequence will not result in overtesting due to high current demands. Any failure that occurs due to the higher switching activity can also occur during functional operation and indicates that the circuit is faulty.

Functional test sequences with decreased switching activity are also important for applications where power dissipation during test application must be limited.

Motivated by these observations, we consider the generation of functional test sequences with reduced and increased switching activity. Similar issues were considered with respect to functional scan-based tests in [14]. As stated earlier, functional test sequences have an advantage over functional scan-based tests in avoiding overtesting since they do not include any scan operations.

2. Procedures

We developed a procedure that uses subsequences of a given test sequence to produce two new test sequences. Both sequences achieve the same fault coverage as the given sequence. Compared to the given test sequence, one of the new test sequences has decreased average switching activity, and one has increased average switching activity. A subsequence $T(l,u)$ of a test sequence T is characterized by two parameters: l is the length of the subsequence, and u is the time unit where the subsequence starts. For a test sequence T of length L we consider $1 \le l \le L$ and $0 \le u \le L-l$.

Every subsequence is associated with an average switching activity computed by a simulation process that applies the subsequence several times starting from a synchronizing sequence. To construct a new test sequence with reduced average switching activity, the subsequences are considered from the one with the lowest to the one with the highest switching activity. Every subsequence is used for extending the new test sequence being constructed, until the new test sequence detects all the faults detected by the given test sequence. Due to the order by which the subsequences are considered, subsequences with lower switching activity are given a higher preference for inclusion in the new test sequence. As a result, the new test sequence, denoted by T_{incr_swa}, has reduced switching activity compared to the given sequence. The subscript *incr_swa* refers to the order by which subsequences are considered, which is by increasing switching activity.

A similar process is used for constructing a test sequence with increased switching activity, except that the subsequences are considered from the one with the highest to the one with the lowest switching activity, until the new test sequence detects all the target faults. In this case, subsequences with higher switching activity are given a higher preference for inclusion in the new test sequence. As a result, the new test sequence, denoted by T_{decr_swa}, has increased switching activity compared to the given sequence T.

By using subsequences of the given test sequence, the computational effort of constructing the new test sequences is limited. Specifically, the procedure for constructing the new test sequences requires only logic and fault simulation.

We also developed a static test compaction process based on the omission of test vectors that are not necessary for detecting target faults. The process uses the switching activity created by each test vector to determine the order by which test vectors will be considered for omission from the test sequence. For reduced average switching activity we consider test vectors for omission from high to low switching activity. For increased average switching activity we consider test vectors for omission from low to high switching activity. We denote the compacted test sequences obtained from T_{incr_swa} and T_{decr_swa} by $T_{incr\_swa\_comp}$ and $T_{decr\_swa\_comp}$, respectively.

3. Experimental results

Next, we present experimental results of the procedures developed. We consider single stuck-at faults as the target fault model.

For the given test sequence T we consider a test sequence that was generated by a sequential test generation procedure and achieves the highest known stuck-at fault coverage. The test sequence T is compacted by static test compaction to reduce its length without reducing its fault coverage. All the test sequences obtained from T achieve the same fault coverage.

In Table 1 we show preliminary results for several circuits. We report on four test sequences: T (row *orig*), T_{incr_swa} (row *incr_swa* column *test gen*), $T_{incr\_swa\_comp}$ (row *incr_swa* column *static comp*), T_{decr_swa} (row *decr_swa* column *test gen*) and $T_{decr\_swa\_comp}$ (row *decr_swa* column *static comp*). For every test sequence we show the length (subcolumn *len*) and the average switching activity (subcolumn *swa*). For test sequences produced by using test subsequences we also show (under subcolumn *max*) the maximum length of a subsequence used before all the target faults were detected.

Table 1: New test sequences

		test gen			static comp	
circuit	type	len	swa	max	len	swa
s382	orig	516	70.39	-	-	-
s382	incr_swa	2481	38.78	98	2408	38.17
s382	decr_swa	818	76.77	115	785	77.53
s526	orig	1006	97.00	-	-	-
s526	incr_swa	2738	80.67	126	1441	71.29
s526	decr_swa	2693	113.80	96	2078	113.87
s820	orig	491	270.81	-	-	-
s820	incr_swa	645	219.56	38	415	219.55
s820	decr_swa	854	293.72	273	400	294.00
s1196	orig	238	364.56	-	-	-
s1196	incr_swa	326	280.92	46	265	280.54
s1196	decr_swa	317	433.61	70	249	433.90
b07	orig	380	120.61	-	-	-
b07	incr_swa	351	99.73	170	287	99.56
b07	decr_swa	373	157.52	78	248	158.21
b08	orig	415	72.03	-	-	-
b08	incr_swa	627	52.68	29	622	52.67
b08	decr_swa	534	74.15	331	399	74.16
b11	orig	554	221.45	-	-	-
b11	incr_swa	2025	163.03	68	1326	163.02
b11	decr_swa	1064	260.11	45	870	260.18

From Table 1 and considering additional circuits (not included due to limited space), all the subsequences used are shorter than T. This indicates that subsequences are effective in detecting target faults.

T_{incr_swa} and T_{decr_swa} are longer than T. The increased length allows us to control their switching activity. As a result, T_{incr_swa} always has the lowest average switching activity, and T_{decr_swa} always has the highest average switching activity.

Static test compaction reduces the length of T_{incr_swa} without increasing its switching activity. In most cases, the switching activity of T_{incr_swa} is reduced further by compaction. The compacted test sequence is longer than T in most cases. This indicates that, in order to maintain a low average switching activity, a longer test sequence is necessary.

Static test compaction also reduces the length of T_{decr_swa} without reducing its switching activity. In most cases, the switching activity of T_{decr_swa} is increased further by compaction. The length of the compacted test sequence is sometimes lower than that of T.

A test length lower than that of T is possible when T_{decr_swa} is considered since the static test compaction process used for T is different, and does not use the switching activity to decide on the order by which the test vectors will be considered. This result also points to the use of the switching activity as a static test compaction heuristic, which leads to short test sequences.

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Trade-off between Power Dissipation and Delay Fault Coverage For LOS and LOC Testing Schemes

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Abstract

Power dissipation and delay fault coverage have always been a trade-off that becomes an actual issue for at-speed test scheme. In this paper, we list the sources of power dissipation and delay fault models that may affect circuits. After, we propose a comparison between two different at-speed scan testing schemes, namely Launch-Off-Shift (LOS) and Launch-Off-Capture (LOC). For this purpose, we operate a formal characterization of the two scan test schemes through their application in benchmark circuits.

Keywords: test power dissipation, delay fault coverage, LOS, LOC, at-speed test.

1. Introduction

Nowadays electronics products present various issues that become more important with CMOS technology scaling. High operation speed, and so high frequency, is a mandatory request. On the other hand, power consumption is one of the most significant constraints due to large diffusion of portable equipments. These needs influence not only the design of devices, but also the choice of appropriate test schemes that have to deal between production yield and test quality and cost.

Test power has been demonstrated to be significantly higher than normal operation (functional) power. The increment of power consumption during test is due to multiple sources [1]. First of all, the absence of correlation between consecutive test vectors leads to higher switching activity and more power dissipation. DFT circuitries like scan chains are intensively used during test and not in the functional mode. For test time and test data reduction, concurrent test, compression and compaction are often used, and they are power consuming. In general, *at-speed* scan test schemes lead to power consumption 3 or 4 times higher than the functional patterns [2], causing side phenomena like voltage droop and IR-drop.

Concerning delay faults, they are classified in two main categories: the transition delay faults and the path delay faults. Both of them target slow-to-rise and slow-to-fall faults. In particular, the transition delay fault model treats slow transitions of a particular circuit node that is propagated to primary outputs. In addition to localized delays, the path delay fault model deals with the delay accumulated along a particular path between input and output nodes.

In order to detect delay faults, two efficient scan test schemes are currently used: *Launch-off-Shift (LOS)* and *Launch-off-Capture (LOC)* delay test schemes. The main goal of this study is to compare the performance between LOS and LOC testing schemes in terms of delay fault coverage and power dissipation.

2. Scan Delay Testing

Delay fault testing requires a two-vector test <V1, V2>, where the vector V1 is used to initialize the nodes of the circuit under test (CUT), and the test vector V2 produces transitions in those nodes, at speed frequency. The response of CUT internal nodes to V2 is captured by the scan chains. The comparison between the observed values and expected ones gives the test response.

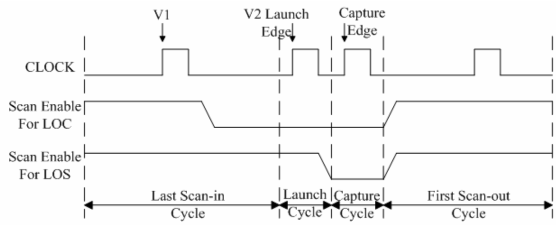

Figure 1: Waveforms of LOC and LOS testing schemes

The typical waveforms of clock signal and Scan Enable signals for LOS and LOC schemes are given in Figure 1. Test vector V1 is shifted into the scan chains at slow speed, while launch and capture cycles are applied at speed.

In the LOS test scheme, the scan enable signal (SEN) remains at '1' (=shift mode), and the test vector V2 is obtained by one bit shifting of vector V1. Transitions are launched and propagated in the CUT. During the capture cycle, the SEN signal is switched from 1 to 0 (=functional mode), and then the response to V2 is captured. It has been reported in the literature that operation of the LOS scheme allows high coverage of delay faults, but the SEN signal needs to be switched at speed. In the LOC scheme, after the test vector V1 is shifted into the scan chain, the SEN signal has the advantage to have a large time window to be switched from 1 to 0. However, as test vector V2 is the response of the CUT to V1 during the launch cycle, the complexity of test vector generation is more complex than in the LOS testing scheme. Moreover, this operation strategy leads to a lower delay fault coverage compared to LOS testing.

Summarizing the above mentioned features, the main advantage of LOS compared to LOC is the better delay fault coverage, and this point has been shown to be crucial for efficient performance validation of today circuits. On the other hand, some components of power consumption, especially *launch power*, are more relevant for LOS test scheme than for LOC [3]. This situation may lead to severe issues in terms of IR-drop and Ldi/dt noises. The properties of LOS and LOC are summarized in Table 1.

	LOS	LOC
Delay Faulty Coverage	Better	Good
Application Testing Time	Short	Long
Max. Frequency	Comparable	Comparable
Complexity of ATPG	Easy	Complicated
Implementation	Expensive	Easy
Power Consumption	Higher	High
Improving Methods	Very Few	More

Table 1: Comparison table of LOC and LOS tests

In industrial circuits, LOC test schemes are widely used since long time, while LOS schemes started to be employed only recently, despite the higher delay fault coverage. The minor use of LOS schemes is mainly due to the difficult implementation of the at-speed SEN signal.
In order to alleviate this problem, a first solution to allow the use of a slow SEN signal during LOS has been proposed in [4]. This solution is based on the use of a low-overhead control logic which is inserted in the scan cell. A dedicated signal is generated from SEN and clock signals. This signal enables the scan cell instead of SEN. Consequently, the SEN signal can be switched from 1 to 0 at a slow speed, like in LOC test scheme. V2 is launched in shift mode by the asynchronous signal, and then the test response is captured as LOC testing schemes. In this way, high fault coverage and easily implementation are achieved for LOS test scheme. Another solution used in industry is discussed in [3] and is based on clustering the flip-flops into groups by a function enable signal, and for each group a test enable control is employed. This method allows a certain power reduction since not all of the scan flip-flops are active during test. The authors of [3] report a power reduction of nearly 20% of peak switching activity. On the other hand, this method does not assure the maximum fault coverage.

3. Testing and Test Power

Because LOC has been used in industry for many years, most of solutions proposed so far to reduce power consumption during at-speed test application are based on this (LOC) scheme. Only the study reported in [3] addresses the problem of how to reduce power consumption during LOS test application. Although comparing the LOC and LOS testing scheme in terms of power consumption (considering the use of a slow SEN signal), the authors do not provide a comprehensive and quantitative comparison between LOC and LOS including both power consumption and delay fault coverage measurements. In order to supplement this study and show the possible tradeoff that can be done between power dissipation and delay fault coverage for LOS and LOC testing schemes, a deeper and quantitative analysis is proposed in this paper.

4. Experiments

Although several studies cover the LOS and LOC test schemes in detail, to the best of our knowledge, no quantitative study has been proposed with experimental comparison between LOS and LOC schemes that detail their coverage of delay faults and power consumption. For this purpose, we intend to produce meaningful results. A commercial ATPG (Automatic Patter Generation) tool will be used to generate test patterns for LOS and LOC testing schemes. The ISCAS and ITC benchmark circuits combining both combinational parts and sequential parts will be used for experiments purpose. The whole simulations will be done with Synopsys TetraMax and PowerMill tools.

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