

Publication List
Alex Yakovlev

Authored Monographs :

1. J. Cortadella, M. Kishinevsky, A. Kondratyev, L. Lavagno and A. Yakovlev. Logic Synthesis of Asynchronous Controllers and Interfaces, Springer Series in Advanced Microelectronics, vol. 8, Springer, 2002, ISBN-3-540-43152-7.

Edited Monographs:

1. J. Cortadella, A. Yakovlev and G. Rozenberg (Eds.) Concurrency and Hardware Design (Advances in Petri Nets), Lecture Notes in Computer Science, vol. 2549, ISBN-3-540-00199-9, Springer-Verlag, 2002.
2. A. Yakovlev and R. Nouta (Eds.) Asynchronous Interfaces: Tools, techniques, and Implementations (AINT'2000), TU Delft, The Netherlands, July 2000, ISBN 90-5326-037-4, 158pp.
3. A. Yakovlev, L. Gomes and L. Lavagno (Eds.) Hardware Design and Petri Nets. Kluwer Academic Publishers, Boston, ISBN 0-7923-7791-5, March 2000, 344 pp

Journal papers (refereed):

1. D. Shang, F. Burns, A. Bystrov, A. Koelmans, D. Sokolov and A. Yakovlev. High-security asynchronous circuit implementation of AES, IEE Proceedings, Computers and Digital Techniques, vol.153, No.2, March 2006, pp. 71-77.
2. V. Khomenko, M. Koutny and A. Yakovlev. Logic Synthesis for Asynchronous Circuits Based on STG Unfoldings and Incremental SAT, Fundamenta Informaticae, Volume 70, Issue 1-2, pp 49-73, IOS Press, 2006.
3. F. Xia, F. Hao, I. Clark, A. Yakovlev, and E. G. Chester. Buffered Asynchronous Communication Mechanisms. Fundamenta Informaticae, Volume 70, Issue 1-2, pp 155-170, IOS Press, 2006
4. D. Sokolov, J. Murphy, A. Bystrov and A. Yakovlev, Design and Analysis of Dual-Rail Circuits for Security Applications, IEEE Transactions on Computers, Vol. 54, No.4, pp. 449-460, April 2005.
5. D. Sokolov and A. Yakovlev, Clock-less circuits and system synthesis, IEE Proceedings, Computers and Digital Techniques, vol.152, No.3, May 2005, pp. 298-316.
6. F. Burns, D. Shang, A.M. Koelmans and A. Yakovlev. Scheduling and allocation using closeness tables, IEE Proceedings, Computers and Digital Techniques, Vol. 151, No.5, September 2004, pp.332-340.
7. A. Yakovlev, S. Furber, R. Krenz, A. Bystrov. Design and Analysis of a Self-timed Duplex Communication System, IEEE Transactions on Computers, Vol. 53, No.7, pp. 798-814, July 2004.
8. D. Shang, F. Burns, A. Koelmans, A. Yakovlev, F. Xia. Asynchronous system synthesis based on direct mapping using VHDL and Petri nets, IEE Proceedings,

- Computers and Digital Techniques, Vol. 151, No.3, May 2004, pp. 209-220
(Premium Award of IEE CDT, 2005)
9. V. Khomenko, M. Koutny, and A. Yakovlev: Detecting State Coding Conflicts in STG Unfoldings Using SAT. Special Issue on Best Papers from ICACSD'2003, IOS Press, Fundamenta Informaticae 62(2) (2004) 1-21.
 10. A. Madalinski, A. Bystrov, V. Khomenko and A. Yakovlev. Visualisation and resolution of encoding conflicts in asynchronous circuit design, IEE Proc. CDT, vol. 150, No.5, Sept. 2003, pp. 285-293 (Special issue of Best papers at DATE'2003).
 11. D.J. Kinniment, O.V. Maevsky, A. Bystrov, G. Russell, A.V. Yakovlev. On-chip structures for timing measurement and test, Microprocessors and Microsystems, Vol. 27, No. 9 (October 2003), pp. 473-483.
 12. H. Saito, A. Kondratyev, J. Cortadella, L. Lavagno, T. Nanya and A. Yakovlev, Design of asynchronous controllers with delay insensitive interface, IEICE Transactions on Fundamentals of Electronics Communications and Computer Sciences, Vol. E85-A(12): 2577-2585, December 2002.
 13. F. Xia, A.V. Yakovlev, I.G. Clark and D. Shang. Data communication in systems with heterogeneous timing, IEEE Micro, vol. 22, No. 6, pp. 58-69, Nov./Dec. 2002.
 14. A.M. Abas, A.Bystrov, D.J. Kinniment, O.V. Maevsky, G. Russell, and A.V. Yakovlev. Time difference amplifier, Electronics Letters, vol. 38, no. 23, pp. 1437-1438, 7 Nov. 2002.
 15. D.J.Kinniment, A. Bystrov, A.V. Yakovlev. Synchronization Circuit Performance, IEEE Journal of Solid-State Circuits, vol. 37, no. 2, Feb. 2002, pp. 202-209.
 16. J. Cortadella, M.Kishinevsky, S.M. Burns, K.S. Stevens, A. Kondratyev, L. Lavagno, A. Taubin, A. Yakovlev, Lazy Transition Systems and Asynchronous Circuit Synthesis with Relative Timing Assumptions. IEEE Trans. of CAD, Vol. 21, No. 2, Feb. 2002, pages 109-130.
 17. A. Burns, A.J. Wellings, F. Burns, A.M. Koelmans, M. Koutny, A. Romanovsky, A. Yakovlev. Modelling and Verification of an Atomic Action protocol implemented in ADA, Int. J. of Comp. Systems & Eng., vol. 16 (3): 173-182, May 2001.
 18. A.Burns, A.J.Wellings, A.M.Koelmans, M.Koutny, A.Romanovsky, A.Yakovlev. On Developing and Verifying Design Abstractions for Reliable Concurrent Programming in Ada. Ada Letters, v. XXI, no. 1, March 2001, pp. 48-55.
 19. D. J. Kinniment, A.V. Yakovlev, and B. Gao. Synchronous and Asynchronous A-D Conversion, IEEE Transactions on VLSI systems, Vol. 8 No. 2 Apr. 2000, pp. 217-219.
 20. F. Burns, A. Koelmans and A. Yakovlev. WCET Analysis of Superscalar Processors Using Simulation With Coloured Petri Nets, Real-Time Systems, The International Journal of Time-Critical Computing Systems, Volume 18, Issue 2/3, May 2000, Kluwer Academic Publishers, pp. 275-288.
 21. D.J. Kinniment, A.V. Yakovlev. Low power, low noise micropipelined flash A-D converter, IEE Proc. Circuits, Devices Systems, vol. 146, no.5, October 1999, pp 263-267.

22. J. Cortadella, M. Kishinevsky, A. Kondratyev, L. Lavagno, E. Pastor, and A. Yakovlev. Decomposition and technology mapping of speed-independent circuits using boolean relations. *IEEE Trans. of CAD*, Vol. 18, No. 9, Sep. 1999, pp. 1221-1236.
23. L. Lloyd, K. Heron, A. Yakovlev, and A.M. Koelmans. Asynchronous microprocessors: from high level model to FPGA implementation. *Journal of Systems Architecture* vol. 45 (1999), pp. 975-1000, Elsevier.
24. A. Bystrov and A. Yakovlev. Ordered arbiters. *Electronics Letters*, 27th May 1999, Vol. 35, No. 11, pp. 877-879.
25. F.B. Burns, A.M. Koelmans, A.V. Yakovlev. Analysing superscalar processor architectures with coloured Petri nets. *Int. Journal on Software Tools for Technology Transfer*, Vol.2, No.2, December 1998, Springer, pp. 182-191.
26. A. Yakovlev, D.J. Kinniment, F. Xia and A.M. Koelmans. A FIFO buffer with non-blocking interface. *IEEE Computer Society TCVLSI Technical Bulletin*, Fall 1998, pp. 11-14.
27. A. Kondratyev, J. Cortadella, M. Kishinevsky, L. Lavagno, and A. Yakovlev. Logic decomposition of speed-independent circuits (invited and refereed paper), *Proceedings of IEEE*, vol. 87, no.2, pp. 347-362, Feb. 1999.
28. A. Kondratyev and M. Kishinevsky and A. Yakovlev. Hazard-free implementation of speed-independent circuits, *IEEE Trans. on CAD*, vol. 17, no. 9, pp. 749-771, Sept. 1998.
29. J. Cortadella, M. Kishinevsky, L. Lavagno and A. Yakovlev, Deriving Petri Nets from Finite Transition Systems, *IEEE Transactions on Computers*, Vol. 47, Number 8, pages 859-882, Aug. 1998.
30. I.G. Clark, F. Xia, A.V. Yakovlev and A.C. Davies. Petri net models of latch metastability, *Electronics Letters*, 2nd April 1998, Vol. 34, No.7, pp. 635-636.
31. J. Cortadella, M. Kishinevsky, A. Kondratyev, L. Lavagno and A. Yakovlev, A region-based theory for state assignment in speed-independent circuits, *IEEE Trans. on CAD*, vol. 16, no. 8, August 1997, pp. 793-812.
32. A. Yakovlev. Designing Control Logic for Counterflow Pipeline Processor Using Petri nets, *Formal Methods in Systems Design (Kluwer)*, Vol. 12, No.1 (January 1998), pp. 39-71.
33. A. Semenov, A.M. Koelmans, L. Lloyd and A. Yakovlev. Designing an asynchronous processor using Petri nets, *IEEE Micro*, Vol. 17, No. 2 (March/April 1997), pp. 54-64.
34. J. Cortadella, M. Kishinevsky, A. Kondratyev, L. Lavagno and A. Yakovlev, Petrify: a tool for manipulating concurrent specifications and synthesis of asynchronous controllers, *IEICE Trans. Inf. & Syst.*, Vol. E80-D, No.3, March 1997, pp. 315-325.
35. A. Yakovlev, A.M. Koelmans, A. Semenov and D.J.Kinniment, Modelling, Analysis and Synthesis of Asynchronous Control Circuits Using Petri Nets, *INTEGRATION: the VLSI Journal*, Vol. 21 (1996), pp. 143-170.
36. A. Yakovlev, L. Lavagno and A. Sangiovanni-Vincentelli. A unified signal transition graph model for asynchronous control circuit synthesis. *Formal Methods in System Design (Kluwer)*, Vol. 9, No. 3, Nov. 1996, pp. 139-188.

37. A. Yakovlev, M. Kishinevsky, A. Kondratyev, L. Lavagno and M. Pietkiewicz-Koutny. On the Models for Asynchronous Circuit Behaviour with OR Causality. *Formal Methods in Systems Design* (Kluwer), Vol. 9, No. 3, Nov. 1996, pp. 189-234.
38. A. Yakovlev, A. Koelmans, and L. Lavagno. High level modelling and design of asynchronous interface logic, *IEEE Design and Test of Computers*, Spring 1995, pp. 32-40.
39. A. Yakovlev, A. Petrov, and L. Lavagno. A Low Latency Asynchronous Arbitration Circuit, *IEEE Trans. on VLSI Systems*, vol. 2, No. 3, Sept. 1994, pp. 372-377.
40. A.V. Yakovlev. Structural technique for fault-masking in asynchronous interfaces. *IEE Proceedings E (Computers and Digital Techniques)*, Vol. 140, No.2, March 1993, pp. 81-91.
41. L.Ya. Rosenblum, A.V. Yakovlev, and V.B. Yakovlev. A look at concurrency semantics through "lattice glasses". *Bulletin of the EATCS (European Association for Theoretical Computer Science)*, v37, 1989, pp. 175-180.
42. A. Yakovlev. Designing Self-Timed Systems, *VLSI SYSTEMS DESIGN*, Vol. VI, No. 9, September 1985, pp. 70-90.
43. Yu.G. Karpov, L.Ya. Rosenblum, A.V. Yakovlev, and V.N. Zakharov. Control of asynchronous processes in systolic arrays, *Soviet Journal of Computer Sciences* (translated from Russian, J. Wiley), vol.27, No.2, (1989).
44. V.I. Varshavsky, V.B. Marakhovsky, L.Ya. Rosenblum, A.V. Yakovlev, Yu.S. Tatarinov, and V.Ya. Volodarskii. Structural organisation and information interchange protocols for a fault-tolerant self-synchronous ring baseband channel, *Automatic Control and Computer Science* (translated from Russian, Allerton Press), vol.22, No.4, pp.44-51 (1988).
45. V.I. Varshavsky, V.B. Marakhovsky, L.Ya. Rosenblum, A.V. Yakovlev, Yu.S. Tatarinov, and V.Ya. Volodarskii. Hardware implementation of protocols for a fault-tolerant self-synchronous ring channel, *ibid.*, vol.22, No.6, pp. 59-67 (1988).
46. V.I. Varshavsky, V.B. Marakhovsky, L.Ya. Rosenblum, A.V. Yakovlev, Yu.S. Tatarinov, and V.Ya. Volodarskii. Algorithmic and structural organisation of test and recovery facilities in a self-synchronous ring, *ibid.*, vol.23, No.1, pp.53-58 (1989).
47. V.I. Varshavsky, V.B. Marakhovsky, L.Ya. Rosenblum, and A.V. Yakovlev. From specification to hardware implementation of physical layer protocols, *ibid.*, vol. 21, No.5, pp.59-65 (1987).
48. V.I. Varshavsky, V.B. Marakhovsky, L.Ya. Rosenblum, A.V. Yakovlev, and Yu. S. Tatarinov. Towards fault-tolerant hardware implementation of physical layer network protocols, *ibid.*, vol.20, No.6, pp.71-76 (1986).
49. V.I. Varshavsky, V.B. Marakhovsky, L.Ya. Rosenblum, and A.V. Yakovlev. Principles of self-timing and interface models in VLSI systems, *ibid.*, vol. 19, No.3, pp.72-78 (1985).
50. V.I. Varshavsky, V.B. Marakhovsky, L.Ya. Rosenblum, and A.V. Yakovlev. Implementation and analysis of the TRIMOSBUS self-clocking interface, *ibid.*, vol.19, No.4, pp.80-87 (1985).

Conference papers (refereed):

1. Yuan Chen, Fei Xia, Alex Yakovlev, Virtual Self-timed Blocks for Systems-On-Chip, Proc. ISCAS 2006, May, Kos, Greece, pp. 1969-1972.
2. D. Koppad, D. Sokolov, A. Bystrov, A. Yakovlev, Online testing by protocol decomposition, Proc. IOLTS, July 2006.
3. D. Shang, A. Yakovlev, F. Burns, F. Xian, A. Bystrov, Low-cost online testing of asynchronous handshakes, Proc. European Test Symposium, Southampton, May 2006, IEEE CS Press, pp. 225-230.
4. C. D'Alessandro, D. Shang, A. Bystrov, A. Yakovlev and O. Maevsky. Multi-rail phase-encoding for NoC, Proc. of Int. Symp. Advanced Research in Asynchronous Systems and Circuits (ASYNC'06), March 2006, Grenoble, IEEE CS Press, pp. 107-116.
5. S. Dasgupta, D. Potop-Butucaru, B. Caillaud, A. Yakovlev. Moving from Weakly Endochronous Systems to Delay-Insensitive Circuits, Proceedings of the Second Workshop on Globally Asynchronous, Locally Synchronous Design (FMGALS 2005), Electronic Notes in Theoretical Computer Science, Vol. 146, No.2, January 2006, pp 81-103
6. J. Zhou, D.J. Kinniment, G. Russell and A. Yakovlev, A Robust Synchronizer Circuit, Proceedings of the IEEE Computer Society Annual Symposium on VLSI (ISVLSI'06), Karlsruhe, Germany, March 2006, pp. 442-443.
7. C. D'Alessandro, D. Shang, A. Bystrov, and A. Yakovlev. PSK Signalling on NoC Buses, PATMOS 2005, Leuven, September 2005, LNCS 3728, ISBN 3-540-29013-3, Springer, pp. 286-296
8. J. Murphy, A. Yakovlev, Power-balanced Asynchronous Logic, Proc. 17th European Conference on Circuit Theory and Design (ECCTD), 29 August – 2 September 2005.
9. J. Murphy, A. Bystrov and A. Yakovlev, Self-Checking Circuits for Security Applications, 11th Annual International Mixed-Signals Testing Workshop (IMSTW'05), Cannes, France, June 2005, pp. 278-285.
10. D. Shang, A. Bystrov, A. Yakovlev and D. Koppad, On-line Testing of Globally Asynchronous Circuits, Proc. 11th International Online Testing Symposium (IOLTS'05), St. Raphael, France, July 2005, IEEE CS Press, pp. 135-140.
11. J. Murphy, A. Bystrov and A. Yakovlev, Power-balanced Self Checking Circuits for Cryptographic Chips, Proc. 11th International Online Testing Symposium (IOLTS'05), St. Raphael, France, July 2005, IEEE CS Press, pp. 157-162.
12. J. Cortadella, K. Gorgonio, F. Xia, and A. Yakovlev, Automating Synthesis of Asynchronous Communication Mechanisms, Proc. Int. Conf. on Application of Concurrency to System Design (ACSD'05), St. Malo, France, June 2005, IEEE CS Press, pp. 166-175.
13. H. K. Ramakrishnan, S. Chattopadhyay, A. Yakovlev, S. Dlay, A. G. O'Neill, Design of strained silicon inverters for future VLSI applications, 3rd International Conference on materials for Advanced Technologies (ICMAT 2005), Singapore, 2005.

14. S. Dasgupta and A. Yakovlev, Modelling and verification of globally asynchronous and locally synchronous ring architectures, DATE 2005, Munich, March 2005.
15. D. Koppad, A. Bystrov and A. Yakovlev, Off-line testing of asynchronous circuits, 18th Int. Conf. on VLSI Design, IEEE CS Press, Kolkata, Jan. 3-7, 2005, pp. 730-735
16. D. Shang, F. Burns, A. Bystrov, A. Koelmans, D.Sokolov and A.Yakovlev. A low and balanced power implementation of the AES security mechanisms using self-timed circuits, PATMOS 2004, Santorini, September 2004, LNCS 3254, pp. 471-480.
17. D.J.Kinniment and A.V.Yakovlev. Low latency synchronisation through speculation, PATMOS 2004, Santorini, September 2004, LNCS 3254, Springer, pp. 278-288.
18. F. Hao, F. Xia, E.G. Chester, A. Yakovlev and I. G. Clark. MATLAB Models of ACMs in Control Systems, 1st International Conference on Informatics in Control, Automation and Robotics (ICINCO-2004), Setubal, Portugal, 25-28 August 2004, INSTICC Press, vol.3, pp. 54-61.
19. D. Sokolov, J.Murphy, A.Bystrov and A. Yakovlev. Improving the security of dual-rail circuits, Proc. CHES 2004, M. Joye and J.-J. Quisquater (Eds), August 2004, LNCS 3156, Springer, pp. 282-297.
20. G.-Y. Luo, F. Xia, I. G. Clark, A. M. Koelmans, A. V. Yakovlev. Simulating Heterogeneously Timed Networks in Network Simulator NS, 4th International Symposium on Communicating Systems, Networks and Digital Signal Processing (CSNDSP 2004), University of Newcastle upon Tyne, UK, July 2004.
21. D. Shang, F. Burns, A. Koelmans and A. Yakovlev. A Balanced Power Implementation of the AES Security Algorithm Using Self-Timed Circuits, in the Technical Track Proceedings of the 2nd International Conference of Applied Cryptography and Network Security (ACNS 2004), pp. 84-93, June 8-11, 2004, Yellow Mountain, P.R. China.
22. M. Renaudin and A. Yakovlev, From Hardware Processes to Asynchronous Circuits via Petri Nets: an Application to Arbiter Design, Proc. Workshop on Token Based Computing (ToBaCo2004), satellite to 25th Int. Conf. on Appl. and Theory of Petri nets, Bologna, Italy, 22 June 2004, pp. 59-66.
23. V. Khomenko, M. Koutny and A. Yakovlev, Logic synthesis for asynchronous circuits based on Petri net unfoldings and incremental SAT, Proc. Fourth Int. Conf. Applications of Concurrency to System Design (ACSD 2004), Edited by M. Kishinevsky and Ph. Darondeau, Hamilton, Ontario, Canada, 16-18 June 2004, IEEE Press, pp. 16-25. (Best paper award of ACSD 2004.)
24. F. Xia, F. Hao, I. Clark, A.Yakovlev and E.G. Chester, Buffered asynchronous communication mechanisms, Proc. Fourth Int. Conf. Applications of Concurrency to System Design (ACSD 2004), Edited by M. Kishinevsky and Ph. Darondeau, Hamilton, Ontario, Canada, 16-18 June 2004, IEEE Press, pp. 36-45.
25. D. Koppad, A. Bystrov and A. Yakovlev. Algorithm for Testing Asynchronous circuits, 16th IFIP International Conference on Testing of Communicating Systems (TestCom 2004), St Anne's College, Oxford, UK, 17-19 March 2004.

26. F. Burns, D. Shang, A. Koelmans and A. Yakovlev. An Asynchronous Synthesis Toolset Using Verilog, Proc. Design and Test Europe (DATE'04), Paris, Feb. 2004, IEEE CS Press pp.724-725.
27. V. Khomenko, M. Koutny and A. Yakovlev. Detecting state encoding conflicts in STG unfoldings using SAT, Proc. of ACS'D 2003, Guimaraes, Portugal, June 2003, IEEE CS Press, pp. 51-60.
28. A. Bystrov, D. Sokolov, and A. Yakovlev. Low latency control structures with slack, Proc. of Int. Symp. on Advanced Research in Asynchronous Systems and Circuits (ASYNC'03), May 2003, Vancouver, IEEE CS Press, pp. 164-173.
29. N. Starodoubtsev, S. Bystrov, and A. Yakovlev. Monotonic circuits with complete acknowledgement, Proc. of ASYNC'03, Vancouver, IEEE CS Press, pp. 98-108.
30. A. Madalinski, A. Bystrov, V. Khomenko and A. Yakovlev. Visualization and resolution of coding conflicts in asynchronous circuit design, Proc. DATE 2003, Munich, March 2003, IEEE CS Press, pp. 926-931.
31. D. Sokolov, A. Bystrov and A. Yakovlev. STG optimisation in the direct mapping of asynchronous circuits, Proc. DATE 2003, Munich, March 2003, pp. 932-937.
32. D. Sokolov, A. Bystrov, A. Yakovlev, Tools for STG Optimisation in the Direct Mapping of Asynchronous Circuits, Second UK ACM SIGDA Workshop on Electronic Design Automation, Bournemouth, 16-17 September 2002.
33. F. Burns, D. Shang, A. Koelmans, A. Yakovlev, Using Petri Nets for Asynchronous Data Path and Controller Synthesis, Second ACM SIGDA UK Workshop on Electronic Design Automation, Bournemouth, 16-17 September 2002.
34. F. Xia, A. Yakovlev, I. Clark and D. Shang. Data Communication in Systems with Heterogeneous Timing, Proc. 4th Euromicro Conference on Massively Parallel Computing Systems, Ischia, Italy, 9-12 April 2002.
(<http://www.mpcs.org/MPCS02/Papers/4/Paper.pdf>)
35. V. Varshavsky, A. Yakovlev, V. Marakhovsky and I. Levin, Self-Timing, Self-Checking and Self-Recovery, Proc. 4th Euromicro Conference on Massively Parallel Computing Systems, Ischia, Italy, 9-12 April 2002.
(<http://www.mpcs.org/MPCS02/Papers/8/Paper.pdf>)
36. A. Madalinski, A. Bystrov, A. Yakovlev, Visualisation of Coding Conflicts in Asynchronous Circuit Design, IEEE/ACM 11th International Workshop on Logic and Synthesis, New Orleans, June 2002, IEEE Computer Society and ACM SIGDA, pp. 155-160.
37. A. Bystrov, A. Yakovlev, Synthesis of Asynchronous Circuits with Predictable Latency, IEEE/ACM 11th International Workshop on Logic and Synthesis, New Orleans, June 2002, IEEE Computer Society and ACM SIGDA, pp. 239-243.
38. D. Shang, F. Xia and A. Yakovlev, Asynchronous Circuit Synthesis via Direct Translation, Proc. ISCAS'02, Scottsdale, Arizona, May 2002, IEEE, Volume III, pp. 369-372.
39. O. Maevsky, D.J. Kinniment, A. Yakovlev, A. Bystrov. Analysis of the oscillation problem in tri-flops, Proc. ISCAS'02, Scottsdale, Arizona, May 2002, IEEE, volume I, pp.381-384.

40. V. Khomenko, M. Koutny and A. Yakovlev. Detecting state coding conflicts in STGs using integer programming, Proc. DATE'02, Paris, March 2002, IEEE CS Press, pp. 338-345.
41. A. Bystrov, M. Koutny and A. Yakovlev. Visualization of partial order models in VLSI design flow, Proc. DATE'02, Paris, March 2002, IEEE CS Press, pp. 1089-1090.
42. A. Bystrov and A. Yakovlev. Asynchronous Circuit Synthesis by Direct Mapping: Interfacing to Environment, Proc ASYNC'02, Manchester, April 2002, IEEE CS Press, 127-136.
43. D.J. Kinniment, O. Maevsky, A. Bystrov, G. Russell and A. Yakovlev, On-chip Structures for Timing Measurements and Test, Proc ASYNC'02, Manchester, April 2002, IEEE CS Press, pp. 190-197
44. D. Shang, F. Xia and A. Yakovlev. Testing a Self-Timed Asynchronous Communication Mechanism (ACM) VLSI Chip, Proc. IEEE Workshop on Design and Diagnostics of Electronic Circuits and Systems, Gyor, Hungary, 18-20 April, 2001, pp. 53-56.
45. A. Yakovlev, F. Xia and D. Shang. Synthesis and implementation of a signal-type asynchronous data communication mechanism. In Proc. International Symposium on Advanced Research in Asynchronous Circuits and Systems (ASYNC'01), Salt Lake City, pages 127-136. IEEE Computer Society Press, March 2001.
46. A. Yakovlev, F. Xia. Towards synthesis of asynchronous communication algorithms, Int. Workshop on Synthesis of Concurrent Systems, ICATPN'01 and ICACSD'01, Newcastle upon Tyne, June 2001. (Published in: Synthesis and Control of Discrete Event Systems (Eds. B. Caillaud, P. Darondeau, L. Lavagno and X. Xie), Kluwer Academic Publishers, ISBN-0-7923-7639-0, January 2002, pp. 57-75.)
47. N. Starodoubtsev, A. Bystrov, and A. Yakovlev. Semi-modular latch chains for asynchronous circuit design. Proc. 10th Int. Workshop on Power and Timing Modelling, Optimization and Simulation (PATMOS'2000), Goetingen, Germany, Sept. 2000, D. Soudris, P. Pirsch, E. Barke (Eds), LNCS 1918, Springer, pp. 168-177.
48. A. Madalinski, A. Bystrov and A. Yakovlev. Statistical Fairness of Ordered Arbiters, 16th Annual Performance Engineering Workshop UKPEW2000, July 2000, University of Durham, pp. 165-176.
49. S. DeLong, F. Xia, and A. Yakovlev. An implementation of a three-slot asynchronous communication mechanism using self-timed circuits. Proc. of 1st Int. Workshop on Asynchronous Interfaces (AINT'2000), Delft University of Technology, July 2000, ISBN 90-5326037-4, pp. 37-44.
50. A. Burns, A.J. Wellings, F. Burns, A.M. Koelmans, M. Koutny, A. Romanovsky, A. Yakovlev. Towards Modelling and Verification of Concurrent Ada Programs Using Petri Nets, Proc. Workshop Software Engineering and Petri Nets, 21st Int. Conf. App. Theory of Petri Nets, Aarhus, Denmark, June 2000, pp. 115-134, Technical Report DAIMI PB - 548, Dept. of Computer Science, Univ. of Aarhus, ISSN 0105-8517.
51. J. Cortadella, M. Kishinevsky, A. Kondratyev, L. Lavagno and A. Yakovlev, Hardware and Petri Nets: Application to Asynchronous Circuit Design,

- Application and Theory of Petri Nets 2000, Lecture Notes in Computer Science vol. 1825, pp. 1-15, Springer Verlag, June 2000.
52. D. Shang, F. Xia, and A. Yakovlev. A self-timed asynchronous data communication mechanism, Proc. 1st Annual Postgrad Symp. on Convergence of Telecommunications, Networking and Broadcasting (PGNET2000), Liverpool, John Moores University, EPSRC, pp. 170-176.
 53. A. Bystrov, D. Kinniment, and A. Yakovlev. Priority Arbiters. Proc. Sixth Int. Symp. on Advanced Research in Asynchronous Circuits and Systems (ASYNC2000), April 2000, Eilat, Israel, IEEE Computer Society Press, pp. 128-137.
 54. F. Xia, A. Yakovlev, D. Shang, A. Bystrov, A. Koelmans, and D. Kinniment. Asynchronous Communication Mechanisms using Self-timed Circuits. Proc. Sixth Int. Symp. on Advanced Research in Asynchronous Circuits and Systems (ASYNC2000), April 2000, Eilat, Israel, IEEE Computer Society Press, pp. 150-159.
 55. H. Saito, A. Kondratyev, J. Cortadella, L. Lavagno, A. Yakovlev. What is the cost of delay-insensitivity? Proc. IEEE/ACM Int. Conf. on CAD (ICCAD'99), San Jose, Nov. 1999, IEEE Comp. Soc. Press.
 56. H. Saito, A. Kondratyev, J. Cortadella, L. Lavagno, A. Yakovlev. Proceedings of the ICATPN'99 Workshop on Hardware Design and Petri Nets (HWPN'99), June 21, 1999, Williamsburg, VA, pp. 169-189.
 57. A. Kondratyev, J. Cortadella, M. Kishinevsky, L. Lavagno, A. Yakovlev. Automatic synthesis and optimization of partially specified asynchronous systems. Proc of 36th ACM Design Automation Conference (DAC'99), New Orleans, LA, pp. 110-114.
 58. A. Kondratyev, J. Cortadella, M. Kishinevsky, L. Lavagno, A. Taubin, A. Yakovlev. Lazy Transition Systems: Application to Timing Optimization of Asynchronous Circuits. Proc. IEEE/ACM Int. Conference on CAD (ICCAD'98), November 1998, San Jose, IEEE Comp Soc. Press, pp. 324-331.
 59. I. Mitrani, A. Yakovlev. Tree Arbiter with Nearest-Neighbour Scheduling. Proc. of the 13th International Symposium on Computer and Information Sciences (ISCIS'98), 26-28 October, Belek-Anatlya, Turkey. In: Advances in Computer and Information Sciences'98 (Eds. U. Gudukbay, T. Dayar, A. GURSOY, E. GELENBE) Concurrent Systems Engineering Series Vol. 53, pp. 83-92, ISBN 90-5199-405-2 (IOS Press).
 60. J. Mirkowski and A. Yakovlev. A Petri net model for embedded systems. Workshop on Design and Diagnostics of Electronic Circuits and Systems, Szczyrk, September 2-4, 1998, pp. 313-321, ISBN 83-908409-6-0.
 61. W. Vogler, A. Semenov and A. Yakovlev. Unfolding and Finite Prefix for Nets with Read Arcs. Proceedings of CONCUR'98, Nice, France, Sept. 1998, LNCS No. 1466, pp. 501-516.
 62. L. Lloyd, A. V. Yakovlev, E. Pastor, A.M. Koelmans. Estimations of power consumption in asynchronous logic as derived from Graph Based Circuit Representations. International Workshop on Power and Timing Modeling, Optimization and Simulation (PATMOS'98), Technical University of Denmark - October 7-9, 1998, pp. 367-376, A.M. Trullemans-Anckaert, J. Sparsoe (eds).

63. L. Lloyd, K. Heron, A. M. Koelmans, A.V. Yakovlev. Rapid design of asynchronous logic using reconfigurable architectures. Int. Conference on Microelectronics and Packaging (ICMP'98), Curitiba, Parana, Brazil, 12-14 August 1998.
64. F. Burns, A. Yakovlev and A. Koelmans. Modelling of superscalar processor architectures with Design/CPN. Proc. Workshop on Practical Use of Coloured Petri Nets and Design/CPN. Aarhus (Ed. by K. Jensen), Denmark, 10-12 June 1998, DAIMI TR PB-532, May 1998, pp. 15-30.
65. J. Cortadella, M. Kishinevsky, A. Kondratyev, L. Lavagno, and A. Yakovlev Automatic handshake expansion and reshuffling using concurrency reduction, Proceedings of the ICATPN'98 Workshop on Hardware Design and Petri Nets (HWPN'98), June 23, 1998, Lisbon, pp. 86-110.
66. A.Kondratyev, J. Cortadella, M. Kishinevsky, L. Lavagno, A.Taubin and A. Yakovlev. Identifying state coding conflicts in asynchronous system specifications using Petri net unfoldings, Proceedings of Int. Conf. on Appl. of Concurrency to System Design (ACSD'98), March 1998, Aizu-Wakamatsu, Japan, IEEE Computer Society Press, pp. 152-163.
67. D.J. Kinniment, B. Gao, A. Yakovlev, F. Xia. Towards asynchronous A-D conversion, Proc. 4th Int. Symp. on Advanced Research in Asynchronous Circuits and Systems, March-April 1998, San Diego, CA, IEEE Computer Society Press, pp. 206-215.
68. J. Cortadella, M. Kishinevsky, A. Kondratyev, L. Lavagno, E. Pastor and A. Yakovlev. Decomposition and technology mapping of speed-independent circuits using boolean relations, Proc. IEEE/ACM Int. Conference on CAD (ICCAD'97), November 1997, IEEE Computer Society Press.
69. I. Mitrani, A. Yakovlev. Tree Arbiter with Nearest-Neighbour Scheduling. Proc. 13th UK Workshop on Performance Engineering of Computer and Telecommunication Systems, Ilkley, July 1997, pp. 29/1-29/15 (to be published by Edinburgh University Press).
70. M. Kishinevsky, J. Cortadella, A.Kondratyev, L. Lavagno, A.Taubin and A. Yakovlev. Coupling asynchrony and interrupts: place chart nets and their synthesis, Proc. Int. Conference on Application and Theory of Petri Nets (ed. R. Valette), Toulouse, June 1997, Lecture Notes in Computer Science, Vol. 1248, Springer, Berlin, 1997, pp. 328-347.
71. A. Semenov, A. Yakovlev, E. Pastor, M. Pena, J. Cortadella, and L. Lavagno Partial order approach to synthesis of speed-independent circuits. Proc. 3rd Int. Symp. on Advanced Research in Asynchronous Circuits and Systems, Eindhoven, Holland, April 1997, IEEE Comp. Soc. Press, pp. 254-265.
72. J. Cortadella, M. Kishinevsky, A. Kondratyev, L. Lavagno and A. Yakovlev. Technology mapping for speed-independent circuits: decomposition and resynthesis. Proc. 3rd Int. Symp. on Advanced Research in Asynchronous Circuits and Systems, Eindhoven, Holland, April 1997, pp. 240-253.
73. J. Cortadella, M. Kishinevsky, A. Kondratyev, L. Lavagno and A. Yakovlev. Technology mapping of speed-independent circuits based on combinational decomposition and resynthesis, Proc. EDTC'97, Paris, March 1997, IEEE Comp. Soc. Press, pp. 98-105.

74. A. Semenov, A. Yakovlev, E. Pastor, M. Pena, and J. Cortadella, Synthesis of Speed-independent circuits from STG-unfolding segment, Proc. 34th ACM/IEEE Design Automation Conference (DAC'97), Anaheim, CA, June 1997, pp. 16-21.
75. J. Cortadella, Kondratyev, A., Kishinevsky, M., Lavagno. L. and A. Yakovlev, Petrify: a tool for manipulating concurrent specifications and synthesis of asynchronous controllers. Proc. 11th Conference on Design of Integrated Circuits and Systems (DCIS'96), Barcelona, Nov. 1996, pp.205-210.
76. V. Varshavsky, V. Marakhovsky and A. Yakovlev. Towards Self-Checking and Self-Recovery in Self-Timed Embedded Systems. Proc. IEEE International Workshop On Embedded Fault-Tolerant Systems, Dallas, Texas, September 1996.
77. J. Cortadella, A. Kondratyev, M. Kishinevsky, L. Lavagno and A. Yakovlev, Complete state encoding based on theory of regions, Proc. 2nd Int. Symp. on Advanced Research in Asynchronous Circuits and Systems, Aizu, Japan, March 1996, pp. 36-47.
78. A.Semenov and A. Yakovlev, Verification of asynchronous circuits based on Time Petri Net unfolding, Proc. 33rd ACM/IEEE Design Automation Conference (DAC'96), Las Vegas, June 1996, pp. 59-63.
79. J. Cortadella, Kondratyev, A., Kishinevsky, M., Lavagno. L. and A. Yakovlev, Methodology and tools for complete state coding in STG-based synthesis of asynchronous circuits, Proc. 33rd ACM/IEEE Design Automation Conference (DAC'96), Las Vegas, June 1996, pp. 63-66.
80. N.Starodoubtsev, A. Yakovlev and S. Petrov, Use of VHDL-based environment for interactive synthesis of asynchronous circuits. Proceedings VHDL Forum in Europe Spring'96 Working Conference, Dresden, Germany, May 1996, pp. 21-33.
81. A.Yakovlev, A.Semenov, A.M.Koelmans and D.J.Kinniment. Petri nets and asynchronous circuit design, Digest of IEE Colloquium on Design and Test of Asynchronous Systems, IEE, London, Ref. No. 1996/040, pp. 8/1-8/6.
82. J. Cortadella, M. Kishinevsky, L. Lavagno and A. Yakovlev. Synthesizing Petri nets from state-based models. Proc. ICCAD'95, November 1995, San Jose, CA, IEEE Comp. Soc. Press, Nov. 1995, pp. 164-171.
83. A.Semenov and A. Yakovlev, Verification of asynchronous circuits based on timed Petri net unfolding, Proc. of the Int. Workshop on Timing Issues in the Specification and Synthesis of Digital Systems (TAU'95), Seattle, Nov. 1995, pp. 199-210.
84. A. Kondratyev, M. Kishinevsky and A. Yakovlev. On hazard-free implementation of speed-independent circuits. Proc. Asia and South Pacific Design Automation Conference (ASP-DAC'95), Chiba, Japan, August-September 1995, pp. 241-248.
85. A. Semenov and A. Yakovlev. Combining partial orders and symbolic traversal for efficient verification of asynchronous circuits. Proc. IFIP Int. Conference on Computer Hardware Description Languages, (CHDL'95),Chiba, Japan, August-September 1995, pp. 567-573.
86. A. Yakovlev, V. Varshavsky, V. Marakhovsky and A. Semenov, Designing an asynchronous pipeline token ring interface, Proc. of 2nd Working Conference on Asynchronous Design Methodologies, London, May 1995, IEEE Comp. Society Press, N.Y., 1995, pp. 32-41.

87. A. Kondratyev, J. Cortadella, M. Kishinevsky, E. Pastor, O. Roig, and A. Yakovlev. Checking Signal Transition Graph Implementability by Symbolic BDD Traversal, European Design and Test Conference, Paris, March 1995, IEEE Comp. Society Press, N.Y., pp. 325-332.
88. J. Cortadella, L. Lavagno, P. Vanbekbergen, and A. Yakovlev. Designing Asynchronous Circuits from Behavioural Specifications with Internal Conflicts, Proc. Int. Symp. on Advanced Research in Asynchronous Circuits and Systems (ASYNC'94), Salt Lake City, Nov. 1994, IEEE Comp. Society Press, N.Y., pp. 106-115.
89. A. Yakovlev, M. Kishinevsky, A. Kondratyev, and L. Lavagno. OR causality: modelling and hardware implementation, Proc. Int. Conference on Application and Theory of Petri Nets (ed. R. Valette), Zaragoza, June 1994, Lecture Notes in Computer Science, vol. 815, Springer, Berlin, 1994, pp. 568-587.
90. A. Kondratyev, M. Kishinevsky, B. Lin, P. Vanbekbergen, and A. Yakovlev. Simple-gate implementation of speed-independent circuits, Proc. IEEE Design Automation Conference, DAC'94, San Diego, June 1994, IEEE Comp. Society Press, N.Y., pp. 56-62.
91. A. Kondratyev, M. Kishinevsky, B. Lin, P. Vanbekbergen, and A. Yakovlev. On the conditions for gate-level speed-independence of asynchronous circuits, Proc. ACM Int. Workshop on Timing Issues in the Specification and Synthesis of Digital Systems (TAU'93), Sept. 1993, Malente, Germany.
92. A. Yakovlev, A. Petrov, and L. Rosenblum. Synthesis of asynchronous control circuits from symbolic signal transition graphs, Asynchronous Design Methodologies (Ed. S. Furber, M. Edwards), IFIP Transactions A-28, North-Holland, 1993 (Proc. IFIP 10.5 Working Conf., Manchester, March-April 1993), pp. 71-85.
93. A.V. Yakovlev. Synthesis of hazard-free asynchronous circuits from generalised signal-transition graphs, Proc. 6th Int. Conf. VLSI Design (VLSI DESIGN'93), Bombay, India, January 1993, IEEE Comp. Society Press, N.Y., 1993, pp. 21-24.
94. G. Pulkkis, A. Yakovlev, and A. Petrov. Interfacing transputers to analog environments in real-time systems, Proc. 3rd Nordic Transputer Conference, Copenhagen, May 1993, pp. 96-99.
95. A. Yakovlev, L. Lavagno, and A. Sangiovanni-Vincentelli. A unified signal transition graph model for asynchronous control circuit synthesis. Proc. Int. Conf. on CAD (ICCAD'92), Santa Clara, CA, November 1992, IEEE Comp. Society Press, N.Y., pp. 104-111.
96. A.V. Yakovlev. On limitations and extensions of signal transition graph model for designing asynchronous control circuits. Proc. Int. Conf. on Computer Design (ICCD'92), Cambridge, MA, October 1992, IEEE Comp. Society Press, N.Y., pp. 396-400.
97. A.V. Yakovlev. A structural technique for fault-protection in asynchronous interfaces. Proc. Int. Symp. on Fault-Tolerant Computing, (FTCS'92) Boston, MA, July 1992, IEEE Comp. Society Press, N.Y., pp. 288-296.
98. A.V. Yakovlev and A.I. Petrov. A process event knowledge model for industrial expertise, Industrial Applications of Artificial Intelligence (Ed. J.L. Alty, L.I.

- Mikulich), IFIP, North-Holland, 1991 (Proc. IFIP TC5/WG5.3 Int. Conference on AI in CIM, Leningrad, USSR, April 1990), PP. 115-120.
99. A.V. Yakovlev and A.I. Petrov. On the simulation of asynchronous logical control, Problem Solving by Simulation (Ed. A. Javor), Proc. IMACS European Simulation Meeting, Esztergom, Hungary, August 1990, pp. 9-10.
 100. A.V. Yakovlev and A. Petrov. Petri nets and parallel bus controller design. Proc. of 11th Int. Conf. on Applications and Theory of Petri Nets, Paris, France, June 1990, pp. 244-263.
 101. L.Ya. Rosenblum and A.V. Yakovlev. Analysing semantics of concurrent hardware specifications. Proc. Int. Conf. on Parallel Processing (ICPP89), Pennstate University Press, University Park, PA, July 1989, pp. 211-218, Vol.3.
 102. A.Yu. Kondratyev, L.Ya. Rosenblum, and A.V. Yakovlev, Signal graphs: a model for designing concurrent logic. Proc. Int. Conf. on Parallel Processing (ICPP), Pennstate University Press, University park, PA, July 1988, pp. 51-54, Vol.1.
 103. L.Ya. Rosenblum and A.V. Yakovlev. Signal graphs: from self-timed to timed ones, Proc. of the Int. Workshop on Timed Petri Nets, Torino, Italy, July 1985, IEEE Computer Society Press, NY, 1985, pp. 199-207.

Conference Presentations (not formally refereed):

1. C. D'Alessandro, D. Shang, A. Bystrov, A. Yakovlev and O. Maevsky. Multiple-rail phase-encoding for NoCs, DATE 2006 Friday Workshops, Workshop on Future Interconnects and Networks on Chip, Munich, March 2006, Poster session.
2. J.Zhou, D. Kinniment, G. Russell and A. Yakovlev. Design of fast and reliable synchronizers for NOCs, DATE 2006 Friday Workshops, Workshop on Future Interconnects and Networks on Chip, Munich, March 2006, Poster session.
3. C. A'Alessandro, K. Gardiner, D.J. Kinniment, and A. Yakovlev. On-chip subpicosecond phase alignment, Proc. 2nd UK Embedded PhD Forum, Birmingham, October 2005.
4. D. Sokolov, A. Bystrov, A. Yakovlev. Design for low-power and high-security based on timing diversity, Proc. 2nd UK Embedded PhD Forum, Birmingham, October 2005.
5. A. Madalinski, C. D'Alessandro, P. Wang and A. Yakovlev, Latency aware Conflict Resolution in Asynchronous Control Logic Synthesis, 17th UK Asynchronous Forum, Southampton, September 2005.
6. C. D'Alessandro, D. Shang, A. Bystrov, A. Yakovlev and O. Maevsky, Multiple-Rail Phase-Encoding for NoC, 17th UK Asynchronous Forum, Southampton, September 2005.
7. K. Heron, G. Russell, D.J. Kinniment and A. Yakovlev, Time Amplifiers for On-Chip Interval Measurement, 17th UK Asynchronous Forum, Southampton, September 2005.
8. Y. Chen, F. Xia and A. Yakovlev, The Design of STEP Processor, 17th UK Asynchronous Forum, Southampton, September 2005.
9. D. Koppad, A. Bystrov and A. Yakovlev, On-line Monitoring of Asynchronous Interfaces, 17th UK Asynchronous Forum, Southampton, September 2005.

10. J.P. Murphy, D. Sokolov, A. Bystrov and A. Yakovlev, Resisting Side Channel Attacks Using Dual Spacer Dual Rail, 16th UK Asynchronous Forum, Manchester, September 2004.
11. Y. Zhou and A. Yakovlev. Design of an Asynchronous Sequence Generator with Dynamically Loadable Count Ratio, 16th UK Asynchronous Forum, Manchester, September 2004.
12. Guang-Yeu Luo, Ian G. Clark, Fei Xia, Albert M. Koelmans, Alex V. Yakovlev. Simulating Hets in NS for developing an ACM transport protocol for Networks-on-Chip, PREP 2004, Poster presentation, University of Hertfordshire, 5-7 April 2004.
13. A. Bystrov, D. Koppad, A. Yakovlev, On-line testing of asynchronous circuits, Workshop of ACiD-WG Working Group, Turku, Finland, June 2004.
14. J. Cortadella and A. Yakovlev, Ten Years of Petrifying: where are we now? (Invited talk), Workshop of ACiD-WG Working Group, Turku, Finland, June 2004.
15. A. Yakovlev, A. Bystrov, D. Sokolov, J. Murphy, V. Varshavsky and V. Marakhovsky, Phase-difference based logic: principle and applications, Workshop of ACiD-WG Working Group, Turku, Finland, June 2004.
16. D.Koppad, A.Bystrov and A.Yakovlev, Algorithm for testing asynchronous circuits, Proc. 15th UK Asynchronous Forum, Cambridge Jan. 2004.
17. F.Hao, F.Xia, I.G.Clark, A.Yakovlev and E.G.Chester, RR-BB algorithm models in Matlab. Proc. 15th UK Asynchronous Forum, Cambridge Jan. 2004.
18. G.-Y.Luo, I.G.Clark, F.Xia, A.M.Koelmans and A.Yakovlev, Simulating heterogeneous timing networks in network simulator NS, Proc. 15th UK Asynchronous Forum, Cambridge Jan. 2004.
19. G.-Y.Luo, I.G.Clark, F.Xia, A.M.Koelmans and A.Yakovlev, Experiments with adding security to synchronous netlists, Proc. 15th UK Asynchronous Forum, Cambridge Jan. 2004.
20. A.Bystrov, D. Sokolov, A.Yakovlev and A. Koelmans, Balancing Power Signature in Secure Systems, Proc. 14th UK Asynchronous Forum, Newcastle upon Tyne, 30 June-1 July 2003.
21. D. Koppad, A. Bystrov and A. Yakovlev, Testing in the Direct Mapping Domain, Proc. 14th UK Asynchronous Forum, Newcastle upon Tyne, 30 June-1 July 2003.
22. D.Shang, F.Burns, A.M.Koelmans and A.Yakovlev, An Asynchronous DMA System Design Based on Direct Mapping Using VHDL and Petri Nets, Proc. 13th UK Asynchronous Forum, Cambridge, Dec. 2002.
23. F.Hao, A.Yakovlev, E.G.Chester, F.Xia, I.G.Clark and D.Shang, Implementation of a Three-Slot Signal ACM, Proc. 13th UK Asynchronous Forum, Cambridge, Dec. 2002.
24. A.Bystrov, D.Sokolov and A.Yakovlev, Low-Latency Control Structures with Slack, Proc. 13th UK Asynchronous Forum, Cambridge, Dec. 2002.
25. A. Yakovlev. Is the Die Cast for the Token Game? (invited paper) Proc. of 23rd International Conference on Applications and Theory of Petri nets (ICATPN 2002), Adelaide, Australia, June 2002, LNCS 2360, Springer, pp. 70-79.

26. F. Burns, D. Shang, A. Koelmans and A. Yakovlev, Synthesis of Asynchronous Data Paths and Controllers using Petri Nets, Proc. 12th UK Asynchronous Forum, London, 17-18 June 2002.
27. D. Sokolov, A. Bystrov and A. Yakovlev, Tools for STG Optimisation in the Direct Mapping of Asynchronous Circuits, Proc. 12th UK Asynchronous Forum, London, 17-18 June 2002.
28. A. Madalinski, A. Bystrov and A. Yakovlev, Visualisation of Coding Conflicts in Asynchronous Circuit Design, Proc. 12th UK Asynchronous Forum, London, 17-18 June 2002.
29. A. Yakovlev, F. Burns, A. Bystrov, A. Koelmans, R. Krenz, D. Shang. Behavioural synthesis of asynchronous controllers: a case study with a self-timed communication channel, Proc. Second ACiD-WG Workshop of the European Commission's Fifth Framework Programme, Munich, Jan. 2002.
30. D.J. Kinniment, O.V. Maevsky, A. Bystrov, G. Russell, A.V. Yakovlev. On-chip test for timing conditions, Proc. Second ACiD-WG Workshop of the European Commission's Fifth Framework Programme, Munich, Jan. 2002.
31. J. Cortadella, J. Garside and A. Yakovlev. Tutorial: Logic Design of Asynchronous Circuits, ASPDAC/VLSI Design 2002, Bangalore, Jan. 2002.
32. A. Bystrov and A. Yakovlev, Synthesis of Asynchronous Circuits with Predictable Latency, 11th Async UK Forum, Cambridge, Dec. 2001
33. F. Burns, D. Shang, A. Koelmans and A. Yakovlev, Translating from Asynchronous FSM Specifications in VHDL to Petri Nets, 11th Async UK Forum, Cambridge, Dec. 2001.
34. D. Shang, F. Xia and A. Yakovlev, Asynchronous Circuit Synthesis via Direct Translation, 11th Async UK Forum, Cambridge, Dec. 2001
35. O. Maevsky, A. Bystrov, D.J. Kinniment and A. Yakovlev, Analysis of Logic Gate Q-Flop resolver, 10th UK Async Forum, Edinburgh, July 2001.
36. A. Bystrov, A. Yakovlev and M. Koutny, Visualisation of Partial Order Models in VLSI Design Flow, 10th UK Async Forum, Edinburgh, July 2001.
37. D. Kinniment, A. Bystrov and A. Yakovlev, Synchronisation circuit performance, Proc. First ACiD-WG Workshop of the European Commission's Fifth Framework Programme, Neuchatel, Feb. 2001.
38. A. Yakovlev, F. Xia and I. Clark, Hets: towards harmonising time and power in systems on chip, Proc. First ACiD-WG Workshop of the European Commission's Fifth Framework Programme, Neuchatel, Feb. 2001.
39. I. Clark, F. Xia and A. Yakovlev, Modelling and analysis of asynchronous communication mechanisms, Proc. First ACiD-WG Workshop of the European Commission's Fifth Framework Programme, Neuchatel, Feb. 2001.
40. A. Yakovlev. Tutorial: Specifying Controllers using Petri Nets, 9th Asynchronous UK Forum, Cambridge, Dec. 2000.
41. D. Shang, F. Xia and A. Yakovlev. Testing a Self-Timed Asynchronous Communication Mechanism (ACM) VLSI Chip, 9th Asynchronous UK Forum, Cambridge, Dec. 2000.
42. N. Stardoubtsev and A. Yakovlev. Isochronic Fork-Free Asynchronous Circuits, 9th Asynchronous UK Forum, Cambridge, Dec. 2000.

43. J. Cortadella, L. Lavagno, A. Yakovlev. Hardware Design and Petri nets, Advanced Tutorial on Hardware Design and Petri Nets, 21st Int. Conf. App. Theory of Petri Nets, Aarhus, Denmark, June 2000.
44. A. Bystrov and A. Yakovlev. Dynamic Priority Arbiter with FIFO, Proc. 8th Asynchronous UK Forum, South Bank University, London, June 2000.
45. A. Yakovlev. Towards Modelling and Verification of Concurrent Ada Programs Using Petri Nets, BAT/PORTA Workshop 18th to 19th May 2000, University of Newcastle.
46. I. Blunno, A. Bystrov, J. Carmona, J. Cortadella, L. Lavagno and A. Yakovlev. Direct synthesis of large-scale asynchronous controllers using a Petri-net based approach. Proc. of the Fourth FP4 ACiD-WG workshop, Grenoble, January 2000.
47. A. Bystrov, A. Yakovlev. Fast four-phase tree FIFO. Proc. 7th UK Asynchronous Forum, University of Newcastle upon Tyne, 20-21 December 1999.
48. F. Xia, A. Yakovlev, I. Clark. Testing the data freshness properties of asynchronous communication mechanisms. Proc. 7th UK Asynchronous Forum, University of Newcastle upon Tyne, 20-21 December 1999.
49. A. Madalinski, F. Xia and A. Yakovlev Studying the data loss and data re-reading behaviour of a four-slot asynchronous communication mechanism using stochastic Petri nets techniques. Proc. 7th UK Asynchronous Forum, University of Newcastle upon Tyne, 20-21 December 1999.
50. A. Bystrov, D. Shang, F. Xia, A. Yakovlev. Self-timed and speed independent latch circuits, Proc. 6th UK Asynchronous Forum, University of Manchester, 12-13th July 1999.
51. F. Xia, D. Shang, A. Yakovlev, A. Koelmans. An Asynchronous Communication Mechanism using self-timed circuits, Proc. 6th UK Asynchronous Forum, University of Manchester, 12-13th July 1999.
52. A. Bystrov and A. Yakovlev. Revisiting the problem of fair arbitration. Proc. of 5th UK Asynchronous Forum, Computer Laboratory, University of Cambridge, December 1998.
53. A. Yakovlev, D.J. Kinniment, F. Xia and A.M. Koelmans. A FIFO buffer with non-blocking interface. Proc. of 5th UK Asynchronous Forum, Computer Laboratory, University of Cambridge, December 1998.
54. E. Pastor, A. Yakovlev and J. Cortadella. Hierarchical communicating nets for the symbolic analysis of coordinated systems. Proc. of the Special Interest Workshop on Exploitation of STG-based Design Technology, St.Petersburg, 6-7 July 1998.
55. L. Lloyd, A. Yakovlev, E. Pastor, A. Koelmans, Estimations of Power Consumption in Asynchronous Logic, 4th UK Async Forum, Imperial College, London, 13-14- July 1998.
56. F. Burns, A. Yakovlev, and A. Koelmans. Modelling Superscalar Processor Architectures with Coloured Petri Nets, Proc. ACiD-WG Workshop "Specification Models and Languages and Technology Effects on Asynchronous Design", Torino, Italy, January 1988.
57. J. Cortadella, M. Kishinevsky, A. Kondratyev, L. Lavagno, and A. Yakovlev. Automatic Handshake Expansion and Reshuffling, Proc. ACiD-WG Workshop "Specification Models and Languages and Technology Effects on Asynchronous Design", Torino, Italy, January 1988.

58. J. Cortadella, M. Kishinevsky, A. Kondratyev, L. Lavagno, A. Taubin and A. Yakovlev. Timing-Based Optimization, Proc. ACiD-WG Workshop "Specification Models and Languages and Technology Effects on Asynchronous Design", Torino, Italy, January 1988.
59. F.Xia, I.G. Clark, A.V. Yakovlev and A.C. Davies. Petri net models of metastable operations in latch circuits. Proc. 3rd UK Forum on Asynchronous Systems, Department of Computer Science, Edinburgh University, December 1997.
60. F. Burns, A. Yakovlev and A. Koelmans. On the modelling of superscalar processor architectures with coloured Petri nets. Proc. 3rd UK Forum on Asynchronous Systems, Department of Computer Science, Edinburgh University, December 1997.
61. D.J. Kinniment, A. Yakovlev, B. Gao. Metastable behaviour and system performance. Proc. 2nd UK Forum on Asynchronous Systems, Department of Computing Science, University of Newcastle upon Tyne, July 1997.
62. A. Semenov and A. Yakovlev. Partial order approach to design, verification and synthesis of asynchronous circuits, Proc. First UK Asynchronous Forum, Edinburgh, December 1996, pp. 47-50.
63. A. Yakovlev, Solving ACiD-WG design problems with Petri net based methods. Proc. ESPRIT ACiD-WG Workshop on Asynchronous Circuit Design, Groningen, Sept. 9-10, 1996, TR CSN9602, Computer Science Notes Series, University of Groningen.
64. J. Cortadella, Kondratyev, A., Kishinevsky, M., Lavagno. L. and A. Yakovlev, Petrify: a tool for synthesis of Petri nets and asynchronous circuits. Proc. ESPRIT ACiD-WG Workshop on Asynchronous Circuit Design, Groningen, Sept. 9-10, 1996, TR CSN9602, Computer Science Notes Series, University of Groningen.
65. A.M. Koelmans, L. Lloyd, A. Semenov and A. Yakovlev. PNIT: a framework for the design of (a)synchronous circuits using Petri nets. Proc. ESPRIT ACiD-WG Workshop on Asynchronous Circuit Design, Groningen, Sept. 9-10, 1996, TR CSN9602, Computer Science Notes Series, University of Groningen.
66. A. Semenov, A. Yakovlev, E. Pastor, M. Pena and J. Cortadella, Synthesis of speed-independent circuits from STG-unfolding segment. Proc. ESPRIT ACiD-WG Workshop on Asynchronous Circuit Design, Groningen, Sept. 9-10, 1996, TR CSN9602, Computer Science Notes Series, University of Groningen.
67. A. Yakovlev. Designing arbiters using Petri nets. Proceedings of the 1995 Israel Workshop on Asynchronous VLSI, Nof Genossar, Israel, March 1995, VLSI Systems Research Center, Technion, Haifa, Israel, pp. 178-201.
68. A. Semenov and A. Yakovlev. Verification using Petri net models. Proceedings of the 1995 Israel Workshop on Asynchronous VLSI, Nof Genossar, Israel, March 1995, VLSI Systems Research Center, Technion, Haifa, Israel, pp. 281-287.
69. A.V. Yakovlev and A.M. Koelmans. Structural Techniques for fault-tolerant asynchronous controllers. Proc. ACiD-WG/EXACT Workshop on Asynchronous Controllers and Interfacing, IMEC, Leuven, Belgium, September 1992.

Chapters in Books (not listed in Conferences):

1. D. Sokolov and A. Yakovlev, Clock-less circuits and system synthesis, Chapter 16 in B. Al-Hashimi (Ed.), System On Chip: Next Generation Electronics, IEE Circuits Devices and Systems Book Series, 2006, pp. 541-586, ISBN: 0-86341-552-0 & 978-086341
2. J. Carmona, J.Cortadella, V. Khomenko and A.Yakovlev. Synthesis of Asynchronous Hardware from Petri Nets, Lectures on Concurrency and Petri Nets: Advances in Petri Nets, Lecture Notes in Computer Science, Volume 3098 / 2004, Publisher: Springer-Verlag Heidelberg, ISSN: 0302-9743, ISBN: 3-540-22261-8, pp 345-401
3. A.V. Yakovlev. Clockless Computing or Learning How to Play “Soft Time” in “Hard Space”, Special Issue of Izvestia SPEEI, Series “Informatics, Control and Computer Technologies” (dedicated to the 70th anniversary of Professor V.I. Timokhin), pp. 55-64
4. A.V. Yakovlev and A.M. Koelmans. Petri nets and Digital Hardware Design Lectures on Petri Nets II: Applications. Advances in Petri Nets, Lecture Notes in Computer Science, vol. 1492, Springer-Verlag, 1998, pp. 154-236.

Technical Reports:

1. A. Madalinski, V. Khomenko, and A. Yakovlev, Interactive Resolution of Encoding Conflicts in Asynchronous Circuits Based on STG Unfoldings, Tech Report Series CS-TR-944, School of Computing Science, University of Newcastle upon Tyne, February 2006.
2. D. Sokolov, A. Bystrov, and A. Yakovlev, Direct mapping of low-latency asynchronous controllers from STGs, NCL-EECE-MSD-TR-2006-110, Microelectronic System Design Group, School of EECE, University of Newcastle upon Tyne, January 2006.
3. A. Mokhov, D. Sokolov, and A. Yakovlev, Completion Detection Optimisation, NCL-EECE-MSD-TR-2005-109, Microelectronic System Design Group, School of EECE, University of Newcastle upon Tyne, October 2005
4. C. Hoggins, C. D’Alessandro, D.J. Kinniment, and A. Yakovlev, Securing On-chip Operations against Timing Attacks, NCL-EECE-MSD-TR-2005-108, Microelectronic System Design Group, School of EECE, University of Newcastle upon Tyne, September 2005.
5. D. Shang, A. Yakovlev, A. Koelmans, D. Sokolov, A. Bystrov, Dual-Rail with Alternating-Spacer Security Latch Design, NCL-EECE-MSD-TR-2005-107, Microelectronic System Design Group, School of EECE, University of Newcastle upon Tyne, September 2005.
6. C. D’Alessandro, D. Shang, A. Bystrov, A. Yakovlev, O. Maevsky, Phase-encoded transmission for NoC, NCL-EECE-MSD-TR-2005-106, Microelectronic System Design Group, School of EECE, University of Newcastle upon Tyne, May 2005.
7. Yuan Chen, Fei Xia, Alex Yakovlev, Modeling Asynchronous ANNs for Energy Efficient Implementation, NCL-EECE-MSD-TR-2004-105, Microelectronic System Design Group, School of EECE, University of Newcastle upon Tyne, May 2005.

8. D. Shang, A. Bystrov, A. Yakovlev, Asynchronous, Checker designs for monitoring Handshake Interfaces D. Koppad, NCL-EECE-MSD-TR-2005-104, Microelectronic System Design Group, School of EECE, University of Newcastle upon Tyne, March 2005.
9. H. Simpson, E. Campbell, F. Xia, I. Clark, A. Yakovlev, D. Shang, Further discussions on the classification and high-level models of ACMs, NCL-EECE-MSD-TR-2004-102, Microelectronic System Design Group, School of EECE, University of Newcastle upon Tyne, June 2004.
10. D. Sokolov, J. Murphy, A. Bystrov, A. Yakovlev, Improving the security of dual-rail circuits, NCL-EECE-MSD-TR-2004-101, Microelectronic System Design Group, School of EECE, University of Newcastle upon Tyne, April 2004.
11. H. Simpson, E. Campbell, F. Xia, I. Clark, A. Yakovlev, D. Shang, Further discussions on the classification and high-level models of ACMs, NCL-EECE-MSD-TR-2004-102, Microelectronic System Design Group, School of EECE, University of Newcastle upon Tyne, June 2004.
12. V. Khomenko, M. Koutny and A. Yakovlev. Logic Synthesis Avoiding State Space Explosion, CS-TR: 813, School of Computing Science, University of Newcastle, Aug 2003.
13. V. Khomenko, M. Koutny and A. Yakovlev. Detecting State Coding Conflicts in STG Unfoldings Using SAT, CS-TR: 778, Department of Computing Science, University of Newcastle, Sep 2002.
14. A. Madalinski, A. Bystrov and A. Yakovlev. ICU: A tool for Identifying State Coding Conflicts using STG unfoldings, CS-TR: 773, Department of Computing Science, University of Newcastle, Dec 2002.
15. A. Madalinski, A. Bystrov and A. Yakovlev. Visualisation of Coding Conflicts in Asynchronous Circuit Design, CS-TR: 768, Department of Computing Science, University of Newcastle, Apr 2002.
16. A. Yakovlev, S.B. Furber and R. Krenz, Design, Analysis and Implementation of a Self-Timed Duplex Communication System, CS-TR: 761, Department of Computing Science, University of Newcastle, 2002.
17. A. Bystrov, A. Yakovlev, Synthesis of Asynchronous Circuits with Predictable Latency, CS-TR-754, Department of Computing Science, University of Newcastle, 2001.
18. D.J. Kinniment, O.V. Maevsky, A. Bystrov, G. Russell and A. Yakovlev, On-Chip structures for Timing Measurement and Test, CS-TR: 750, Department of Computing Science, University of Newcastle, 2001.
19. D. Shang, F. Xia and A. Yakovlev, Asynchronous circuit synthesis via direct translation, CS-TR-748, Department of Computing Science, University of Newcastle, 2001.
20. O. Maevsky, D.J. Kinniment, A. Yakovlev and A. Bystrov, Analysis of the oscillation problem in tri-flops, CS-TR-747, Department of Computing Science, University of Newcastle, 2001.
21. A. Bystrov, M. Koutny and A. Yakovlev. Visualisation of Partial Order Models in VLSI Design Flow, CS-TR-744, Department of Computing Science, University of Newcastle, 2001.

22. A. Bystrov, A. Yakovlev, Asynchronous Circuit Synthesis by Direct Mapping: Interfacing to Environment, CS-TR-743, Department of Computing Science, University of Newcastle, 2001.
23. V. Khomenko, M. Koutny and A. Yakovlev, Detecting State Coding Conflicts in STGs Using Integer Programming, CS-TR-736, Department of Computing Science, University of Newcastle, 2001.
24. A. Yakovlev, F. Xia and D. Shang, Synthesis of a signal-type asynchronous data communication mechanism and its hardware implementation, CS-TR-720, Department of Computing Science, University of Newcastle, 2000.
25. A. Madalinski, F. Xia and A. Yakovlev, Relative data freshness of asynchronous communication mechanisms, CS-TR-709, Department of Computing Science, University of Newcastle, 2000.
26. A. Burns, A.J. Wellings, A.M. Koelmans, M. Koutny, A. Romanovsky and A. Yakovlev. On Developing and Verifying Design Abstractions for Reliable Concurrent Programming in Ada, CS-TR-706, Dept. of CS, Newcastle University.
27. A. Madalinski, A. Bystrov and A. Yakovlev, Statistical Fairness of Ordered Arbiters, CS-TR-703, Department of Computing Science, University of Newcastle, 2000.
28. A. Burns, A.J. Wellings, F. Burns, A.M. Koelmans, M. Koutny, A. Romanovsky and A. Yakovlev. Towards Modelling and Verification of Concurrent Ada Programs Using Petri Nets. CS-TR-700, Dept. of CS, Newcastle University.
29. A. Bystrov, D.J. Kinniment and A. Yakovlev, Priority Arbiters, CS-TR-687, Department of Computing Science, University of Newcastle, 2000.
30. F. Xia, A. Yakovlev, A. Bystrov, A.M. Koelmans, D.J. Kinniment and D. Shang, An asynchronous communication mechanism using self-timed circuits, CS-TR-686, Department of Computing Science, University of Newcastle, 2000.
31. A. Yakovlev, D. J. Kinniment, and F. Xia. A FIFO Buffer with Real-Time Interface, TR. no. 649, Department of Computing Science, University of Newcastle upon Tyne, August 1998.
32. L. Lloyd, A. Yakovlev, E. Pastor and A.M. Koelmans. Estimations of Power Consumption in Asynchronous Logic as Derived from Graph Based Circuit Representations, CS-TR: 643, Department of Computing Science, University of Newcastle upon Tyne, 1998.
33. W. Vogler, A. Semenov and A. Yakovlev. Unfolding and Finite Prefix for Nets with Read Arcs. TR. no. 634, Department of Computing Science, University of Newcastle upon Tyne, February 1998.
34. F. Xia, I.G. Clark, A.V. Yakovlev and A.C. Davies. Petri net models of metastable operations in latch circuits. TR. no. 627, Department of Computing Science, University of Newcastle upon Tyne, January 1998.
35. F. Xia and A. Yakovlev. Overview of modelling and analysis techniques for arbiters and related circuits, TR. no. 626, Department of Computing Science, University of Newcastle upon Tyne, January 1998.
36. D. J. Kinniment, B. Gao, A. V. Yakovlev and F. Xia. Towards Asynchronous A-D Conversion, TR. no. 615, Department of Computing Science, University of Newcastle upon Tyne, 1997.

37. A. Kondratyev, J. Cortadella, M. Kishinevsky, L. Lavagno, A. Taubin and A. Yakovlev. Identifying State Coding Conflicts in Asynchronous System Specifications Using Petri Net Unfoldings, TR. no. 614, Department of Computing Science, University of Newcastle upon Tyne, 1997.
38. L. Lloyd, K. Heron, A.M. Koelmans and A. Yakovlev. Asynchronous Microprocessors: From High Level Model to FPGA Implementation, TR. no. 610, Department of Computing Science, University of Newcastle upon Tyne, 1997.
39. D J Kinniment, A V Yakovlev and B Gao. Metastable Behaviour in Arbiter Circuits, TR. no. 604, Department of Computing Science, University of Newcastle upon Tyne, December 1997.
40. J. Cortadella, M. Kishinevsky, A. Kondratyev, L. Lavagno, E. Pastor, A. Taubin and A. Yakovlev. Decomposition and Technology Mapping of Speed-Independent Circuits Using Boolean Relations, Technical Report UPC-DAC-1997-20, May 1997.
41. L. Lloyd, A. Yakovlev and A.M. Koelmans. A 2-Phase Asynchronous Event Driven Buffer with Completion Decetion Signalling, TR. no. 573, Department of Computing Science, University of Newcastle upon Tyne,1997.
42. A. Semenov and A. Yakovlev. Contextual Net Unfolding and Asynchronous System Verification. TR. no. 572, Department of Computing Science, University of Newcastle upon Tyne, December 1997.
43. M. Kishinevsky, J. Cortadella, A.Kondratyev, L. Lavagno and A. Yakovlev. Technology mapping for speed-independent circuits. Technical Report 96-2-005, Department of Computer Hardware, The University of Aizu, December 1996.
44. M. Kishinevsky, J. Cortadella, A.Kondratyev, L. Lavagno and A. Yakovlev. Synthesis of General Petri nets. Technical Report 96-2-004, Department of Computer Hardware, The University of Aizu, November 1996.
45. M. Kishinevsky, J. Cortadella, A.Kondratyev, L. Lavagno, A.Taubin and A. Yakovlev. Place chart nets and their synthesis. Technical Report 96-2-003, Department of Computer Hardware, The University of Aizu, November 1996.
46. J. Cortadella, M. Kishinevsky, L. Lavagno and A. Yakovlev. Deriving Petri nets from finite transition systems. Universitat Politecnica de Catalunya, Tech. Rep. UPC-DAC-96-19, June 1996.
47. A. Semenov, A. Yakovlev, E. Pastor, M. Pena, J. Cortadella, and L. Lavagno Partial order approach to synthesis of speed-independent circuits. TR. no. 566, Department of Computing Science, University of Newcastle upon Tyne, October 1996.
48. A. Semenov, A. Yakovlev, E. Pastor, M. Pena, and J. Cortadella, Synthesis of Speed-independent circuits from STG-unfolding segment , TR. no. 565, Department of Computing Science, University of Newcastle upon Tyne, October 1996.
49. I. Mitrani, A. Yakovlev. Tree Arbiter with Nearest-Neighbour Scheduling. TR. no. 563, Department of Computing Science, University of Newcastle upon Tyne, October 1996.
50. C. Carrion and A. Yakovlev. Design and Evaluation of two Asynchronous Token Ring Adapters. TR. no. 562, Department of Computing Science, University of Newcastle upon Tyne, October 1996.

51. J. Cortadella, Kishinevsky, M., Kondratyev, A., Lavagno, L. and A. Yakovlev. Petrify: a tool for manipulating concurrent specifications and synthesis of asynchronous circuits, TR, Departament d'Arquitectura de Computadors, Universitat Politecnica de Catalunya, April 1996.
52. J. Cortadella, Kishinevsky, M., Kondratyev, A., Lavagno, L. and A. Yakovlev. Coupling technology mapping, logic optimization and state encoding for speed-independent circuits. TR UPC-DAC-96-13, Departament d'Arquitectura de Computadors, Universitat Politecnica de Catalunya, May 1996.
53. N. Starodoubtsev, A. Yakovlev and S. Petrov, Synthesis of asynchronous circuits in VHDL-based environment, TR. no. 540, Department of Computing Science, University of Newcastle upon Tyne, November 1995.
54. A. Semenov, A.M. Koelmans, L. Lloyd and A. Yakovlev, Designing an Asynchronous Processor using Petri Nets, TR. no. 539, Department of Computing Science, University of Newcastle upon Tyne, November 1995.
55. A.M. Koelmans, D.J. Kinniment, Y. Xu and A. Yakovlev, PNIF: An Interchange format for system specification with coloured Petri nets, TR. no. 538, Department of Computing Science, University of Newcastle upon Tyne, November 1995.
56. K.S. Low and A. Yakovlev, Token Ring Arbiters: an exercise in asynchronous logic design with Petri nets, TR. no. 537, Department of Computing Science, University of Newcastle upon Tyne, November 1995.
57. M. Pietkiewicz-Koutny and A. Yakovlev, Non-pure nets and their transition systems, TR. no. 528, Department of Computing Science, University of Newcastle upon Tyne, September 1995.
58. J. Cortadella, M. Kishinevsky, A. Kondratyev, L. Lavagno and A. Yakovlev, A region-based theory for state assignment in asynchronous circuits, Department of Computer Hardware, The University of Aizu, Technical Report 95-2-006, October 1995.
59. A. Yakovlev, Designing Control Logic for Counterflow Pipeline Processor Using Petri nets, TR. no. 522, Department of Computing Science, University of Newcastle upon Tyne, May 1995.
60. A. Semenov, A. Yakovlev and N. Anisimov. Specification and Verification of a Self-Timed Token Ring Protocol. TR. no. 516, Department of Computing Science, University of Newcastle upon Tyne, May 1995.
61. J. Cortadella, M. Kishinevsky, L. Lavagno and A. Yakovlev. Synthesizing Petri nets from state-based models, Universitat Politecnica de Catalunya, Tech. Rep. UPC-DAC-95-09, April 1995.
62. A. Yakovlev, A.M. Koelmans, A. Semenov and D.J. Kinniment, Modelling, Analysis and Synthesis of Asynchronous Control Circuits Using Petri Nets, TR. no. 514, Department of Computing Science, University of Newcastle upon Tyne, April 1995.
63. A. Semenov and A. Yakovlev. Combining partial orders and symbolic traversal for efficient verification of asynchronous circuits. TR Series No. 501, February 1994.
64. A. Kondratyev, M. Kishinevsky and A. Yakovlev. Monotonous cover transformations for speed-independent implementation of asynchronous circuits.

- Department of Computer Hardware, The University of Aizu, Technical Report 94-2-002, June 1994.
65. J. Cortadella, L. Lavagno, P. Vanbekbergen and A. Yakovlev. Designing Asynchronous Circuits from Behavioural Specifications with Internal Conflicts, Universitat Politecnica de Catalunya, UPC/DAC Technical Report No. RR 94/08.
 66. A. Semenov and A. Yakovlev. Event-Based Framework for Verifying High-Level Models of Asynchronous Circuits, Department of Computing Science. TR Series No. 487, May 1994.
 67. A. Yakovlev, M. Kishinevsky, A. Kondratyev and L. Lavagno. On the Models for Asynchronous Circuit Behaviour with OR Causality. Department of Computing Science. TR Series No. 463, Nov. 1993.
 68. A. Yakovlev, A.M. Kolemans and L. Lavagno. High Level Modeling and Design of Asynchronous Interface Logic, Department of Computing Science. TR Series No. 460, Nov. 1993.
 69. A. Yakovlev, A. Petrov and L. Lavagno. High Speed Asynchronous Arbiter. Department of Computing Science. TR Series No. 427, May 1993.
 70. A.V. Yakovlev and A.I. Petrov, Symbolic Signal Transition Graphs and Asynchronous Circuit Design. Computing Lab. TR Series No.395, September 1992.
 71. A.V. Yakovlev, L. Lavagno, and A. Sangiovanni-Vincentelli. A Unified Signal Transition Graph Model for Asynchronous Control Circuit Synthesis, Electronics Research Laboratory, U.C. at Berkeley, Techn. Memo. No. UCB/ERL M92/78, 20 July 1992.
 72. A.V. Yakovlev. Synthesis of hazard-free asynchronous circuits from generalised signal-transition graphs. Computing Lab. TR Series No.377, April 1992.
 73. A.V. Yakovlev. On limitations and extensions of signal transition graph model for designing asynchronous control circuits. Computing Lab. TR Series No.374, February 1992.
 74. A.V. Yakovlev. A structural technique for fault-protection in asynchronous interfaces. Computing Lab. TR Series No.362, November 1991.
 75. A.M. Koelmans, A.V. Yakovlev and D.J. Kinniment. System-level Design Based on Transformational Synthesis: Problems and Options, University of Newcastle upon Tyne, Computing Laboratory TR Series No. 371, January 1992.
 76. A.V. Yakovlev. Analysing concurrent systems through lattices, The Polytechnic of Wales Computer Studies TR CS-91-9, 1991.
 77. A.V. Yakovlev. Relation-based approach to analysing semantics of asynchronous hardware specifications, University of Newcastle upon Tyne Computing Laboratory, Tech. Report Series, No. 286, Nov. 1989.
 78. A. Yakovlev. Concurrency models for designing interface logic in distributed systems, University of Newcastle upon Tyne, Computing Laboratory, Tech. Report Series, No. 285, Nov. 1989.

Other Edited Conference Proceedings:

1. J. Cortadella and A. Yakovlev, Proc. Workshop on Token Based Computing (ToBaCo2004), satellite to 25th Int. Conf. on Appl. and Theory of Petri nets, Bologna, Italy, 22 June 2004.
2. A. Yakovlev and L. Lavagno (Eds.) Proceedings of the ICATPN'99 Workshop on Hardware Design and Petri Nets (HWPN'99), June 21, 1999, Williamsburg.
3. A. Yakovlev (Ed.) Proc. of the Special Interest Workshop on Exploitation of STG-based Design Technology, St.Petersburg, 6-7 July 1998.
4. A. Yakovlev and L. Gomes (Eds.) Proceedings of the ICATPN'98 Workshop on Hardware Design and Petri Nets (HWPN'98), June 23, 1998, Lisbon.
5. S. Furber and A. Yakovlev (Eds.) Proc. 2nd UK Asynchronous Forum, Department of Computing Science, University of Newcastle upon Tyne, July 1997.
6. M.B. Josephs and A. Yakovlev (Eds.) Handouts of the Third ACiD-WG Workshop Newcastle upon Tyne, January 18-19, 1999 Technical Report Series no. 670, Computing Science, University of Newcastle upon Tyne, April 1999.

Patents:

1. Asynchronous serial register, V.I. Varshavsky, V.B. Marakhovsky, L.Ya. Rosenblum, A.V. Yakovlev, USSR Patent 1136216, Bulletin of Inventions, 1985, No. 3.
2. A device for interfacing a receiver with a data bus, V.I. Varshavsky, V.B. Marakhovsky, O.V. Maevsky, L.Ya. Rosenblum, V.I. Timokhin, A.V. Yakovlev, USSR Patent 1241248, Bulletin of Inventions, 1986, No. 24.
3. A device for synchronising modules of a computer system, L.Ya. Rosenblum, O.A. Fedorova, I.V. Yatsenko, A.V. Yakovlev, USSR Patent 1442985, Bulletin of Inventions, 1988, No. 45.

Publications in Russian:

Over 40 papers in Russian, among which journal articles, conference papers, articles in special collections, technical reports.

Translated Books (from Russian):

1. Concurrent Hardware. The Theory and Practice of Self-Timed Design (by M. Kishinevsky et al.), J. Wiley and Sons, 1993. 368pp, ISBN:0-471-93536-0.
2. Self-Timed Control of Concurrent Processes (by V. Varshavsky et al.), Kluwer Academic Publishers, 1990, ISBN:0792305256

Contribution to Standards Specification:

IEEE Standard Backplane Bus Specification for Multiprocessor Architectures: FUTUREBUS, ANSI/IEEE Std 896.1-1987.

Reviews published in ACM Computing Reviews:

Vol.28 (1987) No. 8705-0385, 8709-0759
Vol.29 (1988) No. 8805-0302, 8808-0559, 8811-0848
Vol.30 (1989) No. 8905-0302, 8907-0419, 8910-0726
Vol.31 (1990) No. 9002-0109, 9010-0772
Vol.32 (1991) No. 9104-0261
Vol.33 (1992) No. 9208-0580, 9209-0693, 9211-0880
Vol.34 (1993) No. 9305-0310, 9310-0775, 9312-0927
Vol.35 (1994) No. 9407-0389, 9410-0670

More than 200 short reviews (in Russian) in Soviet Review
Journal "Computing Sciences"