CURRICULUM VITAE

ALEXANDRE YAKOVLEV

Personal information:

Education and Degrees:

1979-1982 *Ph.D. in Computer Science*, Dept. of Computing Science, St. Petersburg Electrical Engineering Institute (SPEEI), Russia. Thesis: "Design and Implementation of Asynchronous Interface Protocols"
1973-1979 *M.Sc. in Computer Engineering (with distinction)*, Dept. of Computer Engineering, SPEEI, Dissertation: "Software Design for Microprocessor-based Logical Control"
1971-1973 *Certificate of Maturity* (grades: 75% "excellent" and 25% "good"), High school No. 38 (with emphasis on mathematics and physics), St. Petersburg, Russia.

Professional Training:

1992-93 Staff development courses at Newcastle: Introductory Course for Academic Staff (Lecturing and Explaining), Course Design and Evaluation, Research Management/Funding.
1990 Two-week School on Formal Methods for VLSI Design, Techn. Univ. of Denmark.
1984-85 Postdoctoral research fellowship, Univ. of Newcastle upon Tyne, Computing Laboratory.
1982-83 Staff development course on teaching methods, SPEEI, St. Petersburg, Russia.

Full-Time Appointments:

Aug. 1997 - present: *Reader in Computing Systems Design*; **Sep. 1991 - Jul. 1997:** *Lecturer in Computing Science*; Dept. of Computing Science, Univ. of Newcastle upon Tyne
Oct. 1990 - Aug. 1991: *Senior Lecturer in Comp. Studies*; Dept. of Computer Studies, Univ. of Glamorgan
Jan. 1988 - Sep. 1990 *Associate Professor in Computing Science, Deputy Head of Dept. of Computing Science*; **Nov. 1982 - Dec. 1987:** *Assistant Professor*; **Nov. 1979 - Oct. 1982:** *PhD student and Part-Time Research Assistant*; **Apr. 1979 - Oct. 1979:** *Computer Engineer and Part-Time Research Assistant*; Dept. of Computing Science, SPEEI, Russia **Oct. 1977 - Mar. 1979:** *Graduate Student and Part-Time Research Assistant*; Dept. of Computer Eng., SPEEI, Russia

Summary of Research Grants Obtained:

EPSRC grants:

- GR/M94366, £173,000, 1/01/2000-31/12/2002, Model visualisation for asynchronous circuit design (MOVIE), Principal Investigator, with A.M.Koelmans, M. Koutny and D.J.Kinniment.
- GR/M94359, £5,700, 15/01/2000-14/01/2002, Visiting fellowship, Behavioural refinements for asynchronous circuit synthesis (BREACH), Sole Investigator.
- GR/L93775, £162,000, 1/04/97-31/03/2001, Asynchronous communication mechanisms for real-time systems (COMFORT), Principal Investigator, with A.M.Koelmans and D.J.Kinniment.
- GR/L28098, £126,000, 1/04/97 - 31/03/2000, Time-predictable hardware platforms (TIMBRE), Principal Investigator, with A.M.Koelmans.
- GR/K70175, £120,000, 1/10/96-29/02/2000, Hazard-free arbiter design (HADES), Principal Investigator, with D.J.Kinniment and G.Russell.
- GR/L24038, £6,000, 1/01/97-31/06/98, Visiting fellowships, Asynchronous circuit synthesis and testing (ASTI), Sole Investigator.
- GR/J52327, £115,000, 1/12/93 - 1/6/97, Automated synthesis of parallel synchronous and asynchronous controllers (ASAP), Co-investigator, with D.J.Kinniment (as PI) and A.M.Koelmans.
- GR/J72486 and GR/J78334, £5,000, 1/07/94-1/01/96, Visiting fellowships, Automated synthesis of asynchronous control circuits, Principal Investigator, with D.J.Kinniment

Other grants:

EU Framework-4: (1) Nr. 214949, £17,000, 1/05/96-30/04/2000; Working Group on asynchronous circuit design (ACiD-WG) (involves eight UK and EU universities and two companies), Principal Investigator with A.M. Koelmans. (2) Nr.20072, £340,000, 15/12/95 - 14/12/98; LTR project on design for validation (DeVa), Co-investigator , with B.Randell, R.Stroud, A.M. Koelmans et al.
Industry: Acorn Networks Inc, $10,000, 1/10/99-31/05/2000, Research studentship, Sole Investigator.
British Council: (1) BC-Germany, £4,300, 1/05/98-31/03/2000, Joint ARC project (with Brandenburg Tech. Univ. at Cottbus, Germany) on dependable embedded system design with Petri Nets (DENT), Principal

Investigator, with A.M.Koelmans, F. Burns and F. Alamsyah. (2) BC-Spain, £4,500, 1/05/98-30/04/99 and 1/05/96-30/04/97, two joint Acciones Integradas projects (with Polytech. Univ. of Catalonia, Spain) on CAD tools for synthesis of asynchronous circuits, Principal Investigator , with A.M.Koelmans, L. Lloyd and A. Semenov. (3) BC-Italy/CNR, £1,000, 27/03/94 -18/04/94, research visit to Politechnic of Turin Dept of Electronics, Sole Investigator.
Leverhulme Trust: Fellowship (for Dr. E. Pastor from UPC, Barcelona), £17,200, 26/01/98-25/10/98, Synthesis methods for timed asynchronous circuits, Sole Investigator.
NATO/Royal Society: (1) Visiting Fellowship (for Dr. J. Mirkowski from TU of Zielona Gora, Poland), £12,300, 5/09/97-4/09/98, Development of formal models for hardware/software co-design, Sole Investigator. (2) Joint Project (with SPEEI, Russia), £25,000, 1/04/93 - 1/08/95, Testing of digital circuits, Co-investigator , with G. Russell and D.J. Kinniment. (3) Visiting fellowship (for Prof. A.R.Taubin from Univ. of Aizu, Japan), £1,000, 1/09/93 - 1/10/93; Sole Investigator.
Nuffield Foundation: Two Undegraduate Research Bursaries, £2,000 1/07/96-1/09/96 and 1/07/94-1/09/94, Sole Investigator.
Newcastle Univ. Research Committee: PhD Research Studentship on design of reliable interfaces and controllers, £31,400, 1/10/93 - 1/09/96, Sole Investigator.

Publications

Most Important Articles:

1(*). A.V. Yakovlev and A.M. Koelmans. Petri nets and Digital Hardware Design Lectures on Petri Nets II: Applications. Advances in Petri Nets, *Lecture Notes in Computer Science (LNCS)*, vol. 1492, Springer-Verlag, 1998, pp. 154-236
2. A. Kondratyev, J. Cortadella, M. Kishinevsky, L. Lavagno, and A. Yakovlev. Logic decomposition of speed-independent circuits. *Proceedings of IEEE*, vol. 87, no. 2, pp. 347-362, Feb. 1999
3. J. Cortadella, M. Kishinevsky, L. Lavagno and A. Yakovlev. Deriving Petri Nets from Finite Transition Systems, *IEEE Transactions on Computers*, vol. 47, no. 8, pp. 859-882, Aug. 1998
4(*). A. Yakovlev. Designing Control Logic for Counterflow Pipeline Processor Using Petri nets, *Formal Methods in Systems Design*, vol. 12, no. 1, pp. 39-71, Kluwer AP, Jan. 1998.
5. J. Cortadella, M. Kishinevsky, A. Kondratyev, L. Lavagno and A. Yakovlev. A region-based theory for state assignment in speed-independent circuits, *IEEE Trans. on CAD*, vol. 16, no. 8, pp. 793-812, Aug. 1997
6(*). A. Yakovlev, L. Lavagno, and A. Sangiovanni-Vincentelli. A unified signal transition graph model for asynchronous control circuit synthesis. *Formal Methods in System Design*, vol. 9, no. 3, pp. 139-188, Kluwer AP, Nov. 1996
7. A. Yakovlev, M. Kishinevsky, A. Kondratyev, L. Lavagno and M. Pietkiewicz-Koutny. On the Models for Asynchronous Circuit Behaviour with OR Causality. *Formal Methods in Systems Design*, vol. 9, no. 3, pp. 189-234, Kluwer AP, Nov. 1996
8. A. Yakovlev, A.M. Koelmans, A. Semenov, and D.J.Kinniment, Modelling, Analysis and Synthesis of Asynchronous Control Circuits Using Petri Nets, *Integration: the VLSI journal*, vol. 21, pp. 143-170, Elsevier, 1996
9. A. Yakovlev, A.M. Koelmans, and L. Lavagno. High level modelling and design of asynchronous interface logic, *IEEE Design and Test of Computers*, Spring 1995, pp. 32-40
10(*). L. Rosenblum and A. Yakovlev. Signal graphs: from self-timed to timed ones, *Proc. of the Int. Workshop on Timed Petri Nets*, Torino, Italy, July 1985, IEEE Comp. Soc. Press, 1985, pp. 199-207.

Other Publications over the last five years:

Journal Articles:

11. J. Cortadella, M. Kishinevsky, A. Kondratyev, L. Lavagno, E. Pastor, and A. Yakovlev. Decomposition and technology mapping of speed-independent circuits using boolean relations. *IEEE Trans. on CAD*, Vol. 18, No. 9, Sep. 1999, pp. 1221-1236
12. L. Lloyd, K. Heron, A. Yakovlev, and A.M. Koelmans. Asynchronous microprocessors: from high level model to FPGA implementation. *J. of Syst. Arch.* , vol. 45 (1999), pp. 975-1000, Elsevier
13. A. Bystrov and A. Yakovlev. Ordered arbiters. *Electronics Letters*, 27th May 1999, Vol. 35, No. 11, pp. 877-879
14. F.B. Burns, A.M. Koelmans, and A.V. Yakovlev. Analysing superscalar processor architectures with coloured Petri nets. *Int. Journal on Software Tools for Technology Transfer*, Vol.2, No.2, December 1998, Springer, pp. 182-191
15. A. Yakovlev, D.J. Kinniment, F. Xia and A.M. Koelmans. A FIFO buffer with non-blocking interface. *IEEE Computer Society TCVLSI Technical Bulletin*, Fall 1998, pp. 11-14
16. A. Kondratyev and M. Kishinevsky and A. Yakovlev. Hazard-free implementation of speed-independent circuits, *IEEE Trans. on CAD*, vol. 17, no. 9, pp. 749-771, Sept. 1998

17. I.G. Clark, F. Xia, A.V. Yakovlev and A.C. Davies, Petri net models of latch metastability, *Electronics Letters*, 2nd April 1998, Vol. 34, No.7, pp. 635-636
18. A. Semenov, A.M. Koelmans, L. Lloyd and A. Yakovlev. Designing an asynchronous processor using Petri nets, *IEEE Micro*, Vol. 17, No. 2 (March/April 1997), pp. 54-64
19. J. Cortadella, M. Kishinevsky, A. Kondratyev, L. Lavagno and A. Yakovlev, Petrify: a tool for manipulating concurrent specifications and synthesis of asynchronous controllers, *IEICE Trans. Inf. & Syst.*, Vol. E80-D, No.3, March 1997, pp. 315-325.
20. Yakovlev, A., Petrov, A., Lavagno, L. A Low Latency Asynchronous Arbitration Circuit, *IEEE Trans. on VLSI Systems*, vol. 2, No. 3, Sept. 1994, pp. 372-377

Conference Papers:

21. H. Saito, A. Kondratyev, J. Cortadella, L. Lavagno, A. Yakovlev. What is the cost of delay-insensitivity? *Proc. of ICATPN'99 Workshop on Hardware Design and Petri Nets (HWPN'99)*, June 1999, Williamsburg, VA, pp. 169-189
22. A. Kondratyev, J. Cortadella, M. Kishinevsky, L. Lavagno, A. Yakovlev. Automatic synthesis and optimization of partially specified asynchronous systems. *Proc. of 36th ACM Design Automation Conference (DAC'99)*, June 1999, New Orleans, LA, pp. 110-114
23. A. Kondratyev, J. Cortadella, M. Kishinevsky, L. Lavagno, A. Taubin, and A. Yakovlev. Lazy Transition Systems: Application to Timing Optimization of Asynchronous Circuits. *Proc. IEEE/ACM Int. Conference on CAD (ICCAD'98)*, November 1998, San Jose, IEEE Comp Soc. Press, pp. 324-331
24. I. Mitrani and A. Yakovlev. Tree Arbiter with Nearest-Neighbour Scheduling. Proc. of the 13th Int. Symp. on Comp. and Inf. Sci. (ISCIS'98), Oct. 1998, Belek-Anatlya, Turkey. In: Adv. in Comp. and Inf. Sci. (Eds. U. Gudukbay, T. Dayar, A. Gursoy, E. Gelenbe) Concurrent Systems Engineering Series Vol. 53, pp. 83-92, (IOS Press)
25. J. Mirkowski and A. Yakovlev. A Petri net model for embedded systems. *Proc. Workshop on Design and Diagnostics of Electronic Circuits and Systems*, Szczyrk, September 2-4, 1998, pp. 313-321
26. W. Vogler, A. Semenov and A. Yakovlev. Unfolding and Finite Prefix for Nets with Read Arcs. *Proceedings of CONCUR'98*, Nice, France, Sept. 1998, LNCS, vol. 1466, Springer pp. 501-516
27. L. Lloyd, A. V. Yakovlev, E. Pastor, A.M. Koelmans Estimations of power consumption in asynchronous logic as derived from Graph Based Circuit Representations. *Proc. of PATMOS'98*, Techn. Univ. of Denmark, Oct. 1998, pp. 367-376
28. L. Lloyd, K. Heron, A. M. Koelmans, A.V. Yakovlev. Rapid design of asynchronous logic using reconfigurable architectures. *Proc. Int. Conf. on Microelectronics and Packaging (ICMP'98)*, Curitiba, Parana, Brazil, 12-14 August 1998
29. F. Burns, A. Yakovlev and A. Koelmans. Modelling of superscalar processor architectures with Design/CPN, *Proc. Workshop on Practical Use of Coloured Petri Nets and Design/CPN*, Aarhus (Ed. by K. Jensen), Denmark, 10-12 June 1998, DAIMI TR PB-532, pp. 15-30
30. J. Cortadella, M. Kishinevsky, A. Kondratyev, L. Lavagno, and A. Yakovlev Automatic handshake expansion and reshuffling using concurrency reduction, *Proc. of the ICATPN'98 Workshop on Hardware Design and Petri Nets (HWPN'98)*, June 23, 1998, Lisbon, pp. 86-110
31. A.Kondratyev, J. Cortadella, M. Kishinevsky, L. Lavagno, A.Taubin and A. Yakovlev. Identifying state coding conflicts in asynchronous system specifications using Petri net unfoldings, *Proc. of Int. Conf. on Appl. of Concurrency to System Design (CSD'98)*, March 1998, Aizu-Wakamatsu, Japan, IEEE Comp. Soc. Press, pp. 152-163
32. D.J. Kinniment, B. Gao, A. Yakovlev, F. Xia. Towards asynchronous A-D conversion, *Proc. 4th Int. Symp. on Adv. Res. in Asynchronous Circuits and Systems (Async'98)*, March-April 1998, San Diego, CA, IEEE Comp. Soc. Press, pp. 206-215
33. J. Cortadella, M. Kishinevsky, A. Kondratyev, L. Lavagno, E. Pastor and A. Yakovlev. Decomposition and technology mapping of speed-independent circuits using boolean relations, *Proc. IEEE/ACM Int. Conf. on CAD (ICCAD'97)*, November 1997, IEEE Comp. Soc. Press
34. I. Mitrani and A. Yakovlev. Tree Arbiter with Nearest-Neighbour Scheduling. *Proc. 13th UK Workshop on Performance Engineering of Computer and Telecommunication Systems*, Ilkley, July 1997, pp. 29/1-29/15
35. M. Kishinevsky, J. Cortadella, A.Kondratyev, L. Lavagno, A.Taubin and A. Yakovlev. Coupling asynchrony and interrupts: place chart nets and their synthesis, *Proc. Int. Conf. on Appl. and Theory of Petri Nets*, Toulouse, June 1997, LNCS, vol. 1248, Springer, 1997, pp. 328-347
36. A. Semenov, A. Yakovlev, E. Pastor, M. Pena, J. Cortadella, and L. Lavagno Partial order approach to synthesis of speed-independent circuits. *Proc. 3rd Int. Symp. on Adv. Res. in Async. Circuits and Systems (Async'97)*, Eindhoven, Holland, April 1997, IEEE Comp. Soc. Press, pp. 254-265
37. J. Cortadella, M. Kishinevsky, A. Kondratyev, L. Lavagno and A. Yakovlev. Technology mapping for speed-independent circuits: decomposition and resynthesis. *Proc. 3rd Int. Symp. on Advanced Research in*

Asynchronous Circuits and Systems (Async'97), Eindhoven, Holland, April 1997, pp. 240-253
38. J. Cortadella, M. Kishinevsky, A. Kondratyev, L. Lavagno and A. Yakovlev, Technology mapping of speed-independent circuits based on combinational decomposition and resynthesis, *Proc. European Conf. on Design and Testing (EDTC'97)*, Paris, March 1997, IEEE Comp. Soc. Press, pp. 98-105
39. A. Semenov, A. Yakovlev, E. Pastor, M. Pena, and J. Cortadella, Synthesis of Speed-independent circuits from STG-unfolding segment *Proc. 34th ACM/IEEE Design Automation Conference (DAC'97)*, Anaheim, CA, June 1997, pp. 16-21
40. J. Cortadella, Kondratyev, A., Kishinevsky, M., Lavagno. L. and A. Yakovlev, Petrify: a tool for manipulating concurrent specifications and synthesis of asynchronous controllers. *Proc. 11th Conference on Design of Integrated Circuits and Systems*, Barcelona, Nov. 1996
41. A. Yakovlev. Solving ACiD-WG design problems with Petri net based methods. *Proc. ESPRIT ACiD-WG Workshop on Asynchronous Circuit Design*, Groningen, Sept. 9-10, 1996, TR CSN9602, Computer Science Notes Series, University of Groningen.
42. V. Varshavsky, V. Marakhovsky and A. Yakovlev. Towards Self-Checking and Self-Recovery in Self-Timed Embedded Systems. *Proc. IEEE Int. Workshop On Embedded Fault-Tolerant Systems*, Dallas, Texas, September 1996
43. J. Cortadella, Kondratyev, A., Kishinevsky, M., Lavagno. L. and A. Yakovlev, Complete state encoding based on theory of regions, *Proc. 2nd Int. Symp. on Advanced Research in Asynchronous Circuits and Systems*, Aizu, Japan, March 1996, IEEE Comp. Soc. Press, NY, 1996, pp. 36-47
44. A. Semenov and A. Yakovlev, Verification of asynchronous circuits based on Time Petri Net unfolding, *Proc. 33rd Design Automation Conference (DAC'96)*, Las Vegas, June 1996, pp. 59-63
45. J. Cortadella, Kondratyev, A., Kishinevsky, M., Lavagno. L. and A. Yakovlev. Methodology and tools for complete state coding in STG-based synthesis of asynchronous circuits, *Proc. DAC'96*, Las Vegas, June 1996, pp. 63-66
46. N.Starodoubtsev, A. Yakovlev and S. Petrov, Use of VHDL-based environment for interactive synthesis of asynchronous circuits. *Proc. VHDL Forum in Europe Spring'96 Working Conference*, Dresden, Germany, May 1996, Shaker Verlag, Aachen, pp. 21-33
47. A.Yakovlev, A.Semenov, A.M.Koelmans and D.J.Kinniment, Petri nets and asynchronous circuit design, *Digest of IEE Colloquium on Design and Test of Asynchronous Systems*, IEE, London, Ref. No. 1996/040, pp. 8/1-8/6
48. J. Cortadella, M. Kishinevsky, L. Lavagno and A. Yakovlev, Synthesizing Petri nets from state-based models. *Proc. Int. Conf. on CAD (ICCAD'95)*, Nov. 1995, San Jose, CA, IEEE Comp. Soc. Press, Nov. 1995, pp. 164-171
49. A.Semenov and A. Yakovlev, Verification of asynchronous circuits based on timed Petri net unfolding, *Proc. of the Int. Workshop on Timing Issues in the Spec. and Synth. of Digital Systems (TAU'95)*, Seattle, Nov. 1995, pp.199-210
50. A. Kondratyev, M. Kishinevsky and A. Yakovlev, On hazard-free implementation of speed-independent circuits. *Proc. Asia and South Pacific Design Automation Conference (ASP-DAC'95)*, Chiba, Japan, August-September 1995, pp. 241-248.
51. A. Semenov and A. Yakovlev. Combining partial orders and symbolic traversal for efficient verification of asynchronous circuits. *Proc. IFIP Int. Conf. on Computer Hardware Description Languages*, (CHDL'95),Chiba, Japan, August-September 1995, pp. 567-573.
52. A. Yakovlev, V.Varshavsky, V. Marakhovsky and A.Semenov, Designing an asynchronous pipeline token ring interface, *Proc. of 2nd Working Conference on Asynchronous Design Methdologies*, London, May 1995, IEEE Comp. Soc. Press, N.Y., 1995, pp. 32-41.
53. A. Kondratyev, Cortadella, J., Kishinevsky, M., Pastor, E., Roig, O., and A. Yakovlev. Checking Signal Transition Graph Implementability by Symbolic BDD Traversal, *Proc. European Design and Test Conference (EDTC'95)*, Paris, March 1995, IEEE Comp. Society Press, N.Y., pp. 325-332. (
54. A. Yakovlev, Designing arbiters using Petri nets. *Proc. 1995 Israel Workshop on Asynchronous VLSI*, Nof Genossar, Israel, March 1995, VLSI Systems Research Center, Technion, Haifa, Israel, pp. 178-201.

All other publications in the last five years:

Edited Conf. Proc.	Conf. Papers	Tech. Reports
4	17	27

All other publications in English:

Transl. Books	Journ. papers	Conf. papers	Book Contrib.	Tech. Reports	ACM CR Reviews
2	11	16	2	16	23

Publications in Russian:

Journ. papers	Conf. papers	USSR Patents	Tech. Reports	Book Chapters	Teaching Guides
12	7	3	12	4	4

Particular Achievements in Research:

Since I got my PhD degree my research work has been mainly focused on: generally, proving the advantages of asynchronous design techniques for constructing digital VLSI systems, and more specifically, demonstrating the crucial role of formal models of concurrency, such as Petri nets, in designing asynchronous systems that are reliable (free from hazards) and efficient (in terms of speed, power consumption and size). These twenty years of research, on my own and in collaboration with colleagues and co-authors from Newcastle University (D. Kinniment, A. Koelmans, L. Lloyd, I. Mitrani, A. Semenov, et al.), St. Petersburg EEI (V. Markhovsky, A. Petrov, L. Rosenblum, V. Varshavsky, et al.) and other universities and industry worldwide (J. Cortadella, M. Kishinevsky, M. Kondratyev, L. Lavagno, E. Pastor, A. Taubin, W. Vogler, et al.) have led to significant results in reaching these two goals. These results are subdivided into the following four main categories:

Formal Models of Asynchronous Behaviour:

(1) During the 80s, on the basis of the formalism of Petri nets, together with L. Rosenblum, I developed the model of *Signal Transition Graphs* or STGs (independently, a similar model was proposed at M.I.T. by T.A. Chu) [ref. 10(*)], on which I worked later with L. Lavagno, et al. [6(*)]. This model has found wide-spread use and led to further investigations by many researchers and asynchronous designers around the world in the last decade (publications in IEEE journals, and conf's such as ASYNC, ICCD, ICCAD, DAC, EDAC, EDTC). Furthermore, a large community of asynchronous system designers in the UK and abroad (e.g., the designers of the first industrial-strength asynchronous microprocessor Amulet at the University of Manchester, and research designers at Intel Labs in Hillsboro, Oregon) are using STGs for synthesis and analysis of their circuits.
(2) Our original STG model [10(*)] was defined for *both untimed and timed cases*, thus not only enabling the design of circuits with unbounded delays (pessimistic, speed-independent, case) but also circuits with timing constraints (allowing optimisation for speed and area at the cost of being more optimistic about delays). The latter aspect has also led to a variety of investigations in the asynchronous community, including the concepts of "Lazy" Transition Systems [23] and Relative Timing that is now being actively used at Intel Corp.
(3) From 1990 to 1995, I developed the *concept of causality* in asynchronous hardware behaviour; in particular, I investigated OR-causality, a concurrency paradigm implemented within the new Petri net extension called Causal Logic Nets [7]. The original "binary version" of the STG model has also been extended to multi-valued or symbolic STGs [my paper at IPIF Async. Conf. Manchester, 1993]. This work has resulted in wider research in this area in the last two years (e.g., at University of Keiserslautern).

Asynchronous Circuit Synthesis:

(4) Between 1990 and 1997, I developed a *Petri net based methodology* for synthesis of asynchronous control circuits [1(*), 9]. The methodology has two-stages. The first stage, Abstract Synthesis, uses labelled Petri nets and their composition. The second stage, Logic Synthesis, uses the refinement of the nets obtained by Abstract Synthesis into Signal Transition Graphs (STGs) and synthesis of hazard-free logic circuits from STGs. In particular, I have contributed to the development of a set of new methods and algorithms supporting this methodology (with J. Cortadella, M. Kishinevsky, A. Kondratyev, L. Lavagno, E. Pastor, A. Semenov, A. Taubin): (a) methods for synthesis of speed-independent circuits *directly* from STGs, *avoiding* the full state space exploration, using *lock (coupledness) classes* (originally proposed in my PhD thesis) and *using Petri net unfoldings and approximate boolean covers* [31,36,39]; (b) a method for synthesis of *safe Petri nets with read arcs* from transition systems and a method of solving the *state encoding problem* in STG-based synthesis, both based the *theory of regions in transition systems* [3,4(*),5, 43, 45, 48]; (c) a method for the *hazard-free implementation* of speed-independent circuits, using *monotonic cover conditions* [16,50]; (d) a method for *decomposition and technology mapping* of speed-independent circuits, using *boolean factorisation and binary relations* [2, 11, 37, 38]; (e) methods for *asynchronous circuit optimisation* (for speed and area factors), and constructing *locally speed-independent (or with bounded delays) and globally delay-insensitive* circuits, using various *STG transformation* techniques (under appropriate equivalence criteria) *concurrency reduction and expansion, handshake expansion* [21, 22]. The main algorithms for this methodology have been implemented in software tools, either with my direct involvement (Petrify [19,40]) or under my supervision (PNIF, PUNT [47]).

Asynchronous Circuit Verification:

(5) Between 1994 and 1998, I have contributed to the development of automatic techniques for asynchronous circuit verification based on *partial order techniques*, such as *(time) Petri net unfoldings* [51,53,44]. Together with A. Semenov, and later with W. Vogler, new methods and algorithms for Petri net unfolding have been developed to improve the efficiency of the partial order analysis approach for k-bounded Petri nets and Petri

nets with read arcs, using the techniques based on *a (FIFO or LIFO) ordering of tokens* in nonsafe places, *representative sets* of transitions [51, TR487(1994)], *weak causality and contextual cycles* [26]. These methods have been implemented under my supervision in tool PUNT, which is currently being advanced in a PhD research work (F. Alamsyah), supported by Applied Materials. These techniques and tools have been successfuly used in a number of applications such as verifying control logic for Amulet microprocessors and checking coherence of Simpson's four-slot asynchronous communication mechanism (actively used by BAe).

Asynchronous Circuit Design:

(6) In order to prove the usefulness of formal methods, techniques and tools in practice, I have been designing (by myself and with A. Bystrov, D. Kinniment, L. Lavagno, A. Petrov, V. Varshavsky, F. Xia et al.) various types of *asynchronous control circuits* using Petri nets, STGs and related techniques. These examples include: bus controllers [PN conf (1990),10(*)] asynchronous pipeline token-ring interface [52], various arbiters [13,20,54], A/D converters [32], micropipeline circuits and processors (e.g., Sproull's Counterflow pipeline) [1(*), 4(*), 8, 12] and ESPRIT ACID-WG industrial design problems [41].
(7) Other methods supporting asynchronous circuit design include: (a) the principle of *structural fault-masking* in asynchronous interfaces and methods for self-recovery in asynchronous systems [paper at IEE Proc. (1993)]; (b) a method for *estimating power consumption* in asynchronous control circuits *based on Petri net T-invariants* (with L. Lloyd, et al.) [27]; (c) a method for *performance analysis of asynchronous arbiters* (with I. Mitrani) [24] ; (d) a method for *using VHDL in the asynchronous circuit synthesis* (with N. Starodoubtsev) [46] ; (e) a method for *self-checking and self-recovery* in self-timed systems (with V. Varshavsky and V. Marakhovsky) [42,52], (f) a method for estimating the worst-case execution time for CPU models using coloured nets (with F. Burns and A. Koelmans) [14,29].

Other Research-related Achievements:

I have formed an Asynchronous Systems Laboratory at Newcastle, which includes fifteen members (lecturers, RAs and PhDs) and has close links with industry (Intel, BAe Dynamics, Theseus Logic, Cogency Technology, Acorn Networks and other companies). I have contributed to the forming of several UK and international academic partnerships with support from EPSRC (assessment: **alpha 5, excellent**), BC, Leverhulme grants and EU ACiD-WG. The most effective is our "Petrify team", which is now supported by Intel (through our Barcelona partner), joint EPSRC project with Bristol University on parallel controller synthesis (ASAP) (assessed as **alpha 5, excellent**), joint EPSRC project COMFORT with King's College London, uncled by BAe Dynamics. I have assisted to forming an asynchronous design team at Intel Corp. that performed work on asynchronous instruction decoder RAPPID (1996-99). More recently, I have formed a EU consortium (GENESIS) to develop generic methods and algorithms for synthesis of distributed, concurrent and asynchronous systems. My other research-related achievements include:

Within the Asynchronous Design community:
(1) **worldwide:** Co-chairing the Programme Committee of the ASYNC'99 and being a member of the PC of all six ASYNC symposia.
(2) **EU:** Newcastle is a full member of the ACiD-WG (currently in Framework-4, and in the re-newal proposed for Framework-5). We have been invited to organise the third ACiD-WG workshop in Newcastle (Jan. 1999) and a number of ACiD-WG special-interest workshops and group meetings in St. Petersburg (1998) and Newcastle (1997-99).
(3) **UK:** I am a member of the steering committee of the Async UK Forum and in this capacity I advise PhD students, RAs and designers throughout the UK on asynchronous design techniques. Newcastle has been awarded the organisation the 2nd (1987) and 7th (1999) Async UK Forums.

Within the Petri Net community:
(1) I have been invited by the Steering Committee of the Int. Conf. on Appl. and Theory of Petri nets (ICATPN) to organise two workshops on Hardware Design and Petri nets with the 19th (1998) and 20th (1999) ICATPN, and an Adanced Tutorial on this topic at the 21st ICATPN (2000).
(2) I have given invited lectures on using Petri nets in hardware design, in a number of universities and companies in the UK and worldwide (Helsinki TU, TU of Denmark, IMEC Leuven, Manchester Univ., Univ. Birmingham, Univ. Augsburg, BTU Cottbus, Hewlett-Packard Res. Labs, Acorn Networks).
(3) I am the main editor of the first monograph on Hardware Design and Petri nets to appear at Kluwer AP in early 2000.