November 2008

Next Generation of Interconnect Technology for Multiprocessor SoC (NEGUS) EP/C512812/1

A.Yakovlev (Principal Investigator), A. Bystrov, A. Koelmans, D.J. Kinniment, Newcastle University

This three year project has been carried out in collaboration with the University of Southampton, Prof. Bashir Al-Hashimi, who submitted his final report in May 2008. The project has met the five objectives outlined in the proposal submission. At Newcastle it was primarily focused on the development of new signalling schemes for reliable communications (link level), associated digital logic design methods and implementations, methods

1. Key advances from this project

- (1) Novel synchronisers (more robust to PVT variations than ordinary jamb latches) and arbiters (for static and dynamic priority arbitration) as building blocks for NoCs and multiprocessor SoCs [1].
- (2) New signalling schemes for Networks on Chip based on phase difference (Phase encoding), inherently resilient to single event upsets and transient faults, including investigations into dual-rail and multi-rail, differential phase encoding, phase encoding combined with time-to-digital conversion, delayphase regeneration circuits, implementation of phase-encoding channel in a VLSI chip, including power and bandwidth analysis [3, 5, 8, 16, 18, 19, 20].
- (3) New fault-tolerant techniques to minimise the impact of cross-talk on phase encoded channels [6], techniques for analysis of the bandwidth-centric optimisation of links with crosstalk avoidance [13], and study of the impact of variability on the reliability of long on-chip interconnects with crosstalk [12]
- (4) Novel asynchronous serialised links for NoC with the same performance as synchronous link but with reduced number of wires and reduced power consumption with transistor level evaluation [14,17] and new communication links with a new NRZ protocol resilient to transient faults and reduced logic complexity compared to phase-encoded channels [8], developed in collaboration with the Southampton partners and University of Bologna.
- (5) New methods for modelling, analysis and implementation of interconnects in FPGAs, including wave-pipelined interconnects [10,11], in collaboration with Imperial College.
- (6) New methods for modelling and verifying asynchronous communication mechanisms (ACMs) using coloured Petri nets [21], new methods and algorithms for automated synthesis of ACMs [5, 22], developed in collaboration with UPC, Barcelona
- (7) New model for designing control circuits for NoC link logic (including phase encoded channels), routers and CPUs, called Conditional Partial Order Graphs (CPOGs), and associated verification and synthesis methods [9, 15, 25].

2. Research Impact

During the course of this project collaboration with companies and academia have been developed further:

- Silistix, Manchester (Dr John Bainbridge, john.bainbridge@silistix.com) expressed interest in the research on synchronisers for NoCs. They are potential user of the technology. David Kinniment is on Silistix advisory board. They are actively supporting a follow up to SYRINGE.
- MBDA, Stevenage (Mr Eric Campbell, ERCampbell@iet.org), we continued our long-standing collaboration with MBDA in the area of modelling and analysis of ACMs, and in NoCs. Eric Campbell gave an invited talk at the 3nd UK Embedded Forum organised by Newcastle in April 2007.
- UPC Barcelona, (Prof. Jordi Cortadella, jordi.cortadella@upc.edu), collaboration in automated verification and synthesis of ACMs. The work is now going on with Dr. K. Gorgonio, who is now working in the Embedded Systems and Pervasive Computing Lab in Federal University of Campina Granda, Brazil; killer@dee.ufcg.edu.br)
- Imperial College, London (Prof. Peter Cheung, p.cheung@imperial.ac.uk), collaboration on modelling and analysis of long interconnects in FPGAs, and this work is now leading to a new joint proposal on virtual reliable links for FPGAs.
- TIMA, INPG, Grenoble, France (Prof. Marc Renaudin, marc.renaudin@imag.fr) have been involved in developments of arbiter design techniques and collaboration for the book [1].
- Univ. Bologna (Prof. Luca Benini) and Politecnico di Torino (Prof. L. Lavagno), whoc made collaborative visits and with who research papers have been published, e.g. [14,17].

3. Explanation of Expenditure

Staff: The project staff requirement was 1 Senior RA full-time (Dr. F. Xia) and 1 RA part-time (Dr. D. Shang), whose time was shared with other EPSRC projects, and 1 PhD student (Mr A. Mokhov). The project also involved two PhD students C. D'Alessandro and B. Halak funded primarily from additional sources (B. Halak was partially supported with a maintenance bursary at the level of £5700 during 24 months). The project also funded a summer project for two MEng graduates Mr. R. Emery and Mr. S.Kolbeinson, who investigated aspects of the use of FPGAs for prototyping neural networks.

Overall the salaries budget has been slightly underspent (less than 0.5%).

Travel, Consumables, Exceptional: Travel budget has been overspent by 10%, this was due to the larger than planned involvement of staff and excellent opportunities for dissemination of our research internationally (e.g. presentations at several ASYNC Symposia). Consumables have been underspent by 10% due to some savings in Europractice chip fabrication. Exception items (student fees) were overspent by 10%. **Overall:** The overall budget is underspent by £313.89.

4. Further Research or Dissemination Activities

The project has been extremely successful in generating further research and dissemination. It helped to form baseline for the proposal of the project STEP awarded in 2007 (EP/E044662/1) and for a new proposal on Reliable Cell Design for Variable Processes, which has been submitted to EPSRC.

This project has been influential in paving the way to a series of international activities and events in the area of Networks on Chip, namely (i) the organisation of the highly successful Friday Workshop on Networks on Chip under DATE 2006 (A. Yakovlev acted as one of the three organisers, see http://async.org.uk/noc2006/), (ii) creation of an annual International Symposium on NoCs (A. Yakovlev is a member of the Steering Committee of the NOCS Symp.), and (iii) securing the organisation of the two IEEE International Symposia, NOCS'08 and ASYNC'08, held in Newcastle in April 2008. The 2008 event produced results of the highly rated tutorial on Metastability and Synchronisation in SoCs and NoCs by David Kinniment (see http://async.org.uk/async2008/, http://async.org.uk/nocs2008/,

http://async.org.uk/nocs2008/keynote-tutorials.html). The implementation of phase encoding circuits in VLSI chips and FPGA have been demonstrated at the ASYNC Symposia chip exhibitions, as well as presented at the ESSCIRC'08 conference. One of the useful by-products of this project has been start of a new PhD research by Robin Emery in the area of developing an on-chip communication infrastructure for neural network modelling and simulation [30,31]. Newcastle has been actively promoting the NoC research in the UK Embedded Forum (see http://async.org.uk/ukef07/).

NEGUS Publications (main 5 publications marked with *)

Books and Edited Monographs

- 1. D.J. Kinniment. Synchronization and Arbitration in Digital Systems, Wiley and Sons, 2007 (with contributions from A.Bystrov, M. Renaudin, G. Russell and A. Yakovlev).
- J. Kleijn and A. Yakovlev (Eds). Petri nets and Other Models of Concurrency – ICATPN 2007, Lecture Notes in Computer Science, vol. 4546, ISBN 978-3-540-73093-4, Springer-Verlag, 2007, 515 p.

Journal papers

- (*) C. S. D'Alessandro, D. Shang, A. Bystrov, A.V. Yakovlev and O. Maevsky. Phase-Encoding for On-Chip Signalling, IEEE Transactions on Circuits and Systems-I: Regular Papers, Vol. 55, No.2, March 2008, pp. 535-545.
- (*) K. Gorgônio, J. Cortadella, F. Xia and A. Yakovlev, Automating Synthesis of Asynchronous Communication Mechanisms, Fundamenta Informaticae, Volume 78, Issue 1, pp 75-100, IOS Press, 2007
- 5. C. D'Alessandro, A. Bystrov and A. Yakovlev, Improved Phase-Encoding Signalling, Electronics Letters, Vol. 43, No. 4, pp. 216-217 (February 2007).
- 6. (*) B. Halak and A. Yakovlev. Fault-Tolerant Techniques to Minimize the Impact of Crosstalk on Phase Encoded Communication Channels, IEEE Transactions on Computers, Vol. 57, No.4, April 2008, pp. 505-519.

Conference papers (formally refereed)

- S. Ogg, B. Al-Hashimi and A.Yakovlev, Asynchronous Transient Resilient Links for NoC, Proc. CODES + ISSS'08, October 19-24, 2008, Atlanta, Georgia, USA, ACM Press, pp. 209-214.
- 8. Crescenzo D'Alessandro, Alex Bystrov and Alex Yakovlev, Implementation of a Phase-encoding Signalling Prototype Chip, 34th European Solid-State Circuits Conference (ESSCIRC), pp. 478-481, September 2008
- A. Mokhov and A. Yakovlev, Verification of Conditional Partial Order Graphs, in: J. Billington, Z. Duan, and M. Koutny (Eds), ACSD 2008, Proc. 2008 8th Int. Conf. on Applicatioon of Concurrency to System Design, June 2008, Xi'an, China, IEEE Press, pp. 128-137.
- 10. T. Mak, C. D'Alessandro, P. Sedcole, P.Y.K. Cheung, A. Yakovlev, W. Luk, Implementation of Wave-Pipelined Interconnects in FPGAs, Proceedings of the 2nd IEEE International Symposium on Networks on Chip, Newcastle upon Tyne, UK, April 2008, pp. 213-214.
- 11. T. Mak, C. D'Alessandro, P. Sedcole, P.Y.K. Cheung, A. Yakovlev, W. Luk, Global Interconnections in FPGAs: Modelling and Performance Analysis, Proceedings of 2008 ACM International Workshop on System Level Interconnect Prediction (SLIP'08), Newcastle, April 2008, pp. 51-58.
- 12. B. Halak, S. Shedabale, H. Ramakrishnan, A. Yakovlev, G. Russell, The Impact of Variability on the Reliability of Long on-chip Interconnect in the Presence of Crosstalk, Proceedings of 2008 ACM International Workshop on System Level Interconnect Prediction (SLIP'08), Newcastle, April 2008, pp. 65-72.
- B. Halak and A. Yakovlev. Bandwidth-Centric Optimization for Area-Constrained Links with Crosstalk Avoidance Methods, Proceedings of DATE'08, Munich, March 2008, pp. 438-443.
- 14. (*) S. Ogg, E. Vialli, B. Al-Hashimi, A. Yakovlev, C. D'Alessandro, and L.Benini. Serialized Asynchronous Links for NoC, Proceedings of DATE'08, Munich, March 2008, pp. 1003-1008.
- 15. (*) A. Mokhov and A. Yakovlev. Conditional Partial Order Graphs and Dynamically Reconfigurable Control Synthesis, Proceedings of DATE'08, Munich, March 2008, pp. 1142-1147.
- 16. C. D'Alessandro, N. Minas, K. Heron, D. Kinniment and A.Yakovlev, NoC Communication Strategies using Time-to-Digital Conversion, Proc. 1st ACM/IEEE Int. Symposium on Networks on Chip, Princeton, USA, May 2007, IEEE CS Press, pp. 65-74.
- 17. S. Ogg, E. Valli, C. D'Alessandro, A. Yakovlev, B. Al-Hashimi, and L. Benini, Reducing Interconnect Cost in NoC through Serialized Asynchronous Links, Proc. 1st ACM/IEEE Int. Symposium on Networks on Chip, Princeton, USA, May 2007, IEEE CS Press, pp. 219.
- C. D'Alessandro, A. Mokhov, A. Bystrov and A. Yakovlev, Delay/Phase Regeneration Circuits, Proc. 13th IEEE Int. Symp.on Asynchronous Circuits and Systems (ASYNC'07), Berkeley, California, March 2007, IEEE CS Press, pp. 105-114.
- 19. C. D'Alessandro, D. Shang, A. Bystrov, A. Yakovlev and O. Maevsky. Multiple-rail phase-encoding for NoC, Proc. of Int. Symp. Advanced Research

in Asynchronous Systems and Circuits (ASYNC'06), March 2006, Grenoble, IEEE CS Press, pp. 107-116.

- C. D'Alessandro, D. Shang, A. Bystrov, and A. Yakovlev. PSK Signalling on NoC Buses, PATMOS 2005, Leuven, September 2005, LNCS 3728, ISBN 3-540-29013-3, Springer, pp. 286-296.
- 21. K. Gorgônio, and F. Xia. Modeling and verifying asynchronous communication mechanisms using coloured Petri nets, Proc. 8th International Conference on Application of Concurrency to System Design (ACSD 2008), Xi'an, China, 23-27 June 2008.
- 22. K. Gorgônio, J. Cortadella, and F. Xia. A compositional method for the synthesis of Asynchronous Communication Mechanisms, Proc 28th International Conference on Application and Theory of Petri Nets and Other Models of Concurrency (ATPN 2007), pp.144-163, Siedlce, Poland, 25-29 June, 2007, LNCS 4546, Springer.

Conference papers (not formally refereed)

- 23. Andrey Mokhov and Alex Yakovlev. Synthesis of multiple rail phase encoding circuits, 20th UK Asynchronous Forum, Manchester, September 2008.
- 24. Basel Halak, Alex Yakovlev, Throughput-Centric Optimisation for fixed width Links with Crosstalk Avoidance Methods, 19th UK Asynchronous Forum, London, September 2007.
- 25. Andrey Mokhov and Alex Yakovlev, Conditional Partial Order Graphs and Dynamically Recongurable Control Synthesis, 19th UK Asynchronous Forum, London, September 2007.
- 26. C. D'Alessandro, A. Bystrov, A. Yakovlev, On-chip Phase Regeneration Circuits, 18th UK Asynchronous Forum, Newcastle, September 2006.
- 27. Basel Halak and Yakovlev, Fault Tolerant Techniques to Minimise the Impact of Crosstalk on Phase Encoding Communication Channels, 18th UK Asynchronous Forum, Newcastle, September 2006.
- 28. A. Mokhov, D. Sokolov, A. Yakovlev, Completion Detection Optimisation based on Relative Timing, 18th UK Asynchronous Forum, Newcastle, September 2006.
- 29. C. D'Alessandro, D. Shang, A. Bystrov, A. Yakovlev and O. Maevsky. Multiple-rail phase-encoding for NoCs, DATE 2006 Friday Workshops, Workshop on Future Interconnects and Networks on Chip, Munich, March 2006, Poster session.
- 30. Robin Emery, Alex Yakovlev and Graeme Chester. Dense-Near/Sparse-Far Hybrid Reconfigurable Neural Network Chip, 20th UK Asynchronous Forum, Manchester, September 2008.

Other reports

 R. Emery and S. Kolbeinson. Examining the Limitations of an FPGA based Neural Network, Internal Project Report, School of EECE, Newcastle University, July 2006.

NEGUS Chip design (see also http://async.org.uk/chip-gallery.html)

NEGUS1 Phase-Encoding Demonstrator Chip. This chip contains different "flavours" of phase-encoding signalling to evaluate feasibility and performance of the scheme.

Year: 2007. Technology: UMC 0.13um through Europractice