November 2008

Synchronizer Reliability in the Next Generation of SoC with Multiple Clocks (SYRINGE)

EP/C007298/1

Alex Yakovlev (Principal Investigator), Gordon Russell, David J.Kinniment,
Newcastle University

This three year project focused on the development of measurement techniques to validate synchronizer circuits at the reliability levels required, and the design of more robust circuits which will deliver the performance necessary for future multi-billion-transistor Systems on a Chip (SoC). The project has met all three objectives outlined in the proposal submission.

1. Key advances from this project

(1) New techniques for analytical and measurement-based prediction of reliability of synchronisers with input time difference beyond 10^(-20)s [1].
(2) Novel synchronizer reliability characterisation techniques based on measurement of deep metastability, both off chip and on-chip [2,3].
(3) New designs of synchronizers robust to low supply voltages and parameter fluctuations in nanometer technologies [3, 9].
(4) New methods for time measurement, designing time-to-digital converters and their FPGA and VLSI implementation [5,6,13,15].
(5) Methods for modelling and analysis of GALS clocking schemes [7].
(6) Development of new signalling schemes for Networks on Chip based on phase difference and time-to-digital conversion [8,12].

2. Research Impact

During the course of this project collaboration with companies and academia have been developed further:

- Intel, Strategic CAD Labs, Hillsborough, USA (Mr Charles E. Dike, charles.e.dike@intel.com) acted as main partner to SYRINGE and has been involved in the evaluation of the development of new synchroniser measurement techniques and robust synchronisers. Two key journal papers [2,3] involved Mr Dike.
- Silistix, Manchester (Dr John Bainbridge, john.bainbridge@silistix.com) expressed interest in the research on synchronisers and metastability. They are potential user of the technology. David Kinniment is on Silistix advisory board. They are actively supporting a follow up to SYRINGE.
- Elastix Corp., Spain and USA (Prof. Jordi Cortadella, jordi@elastix-corp.com, and Dr. Vigyan Singal, vigyan@elastix-corp.com) have been interested in the results of this project (metastability analysis and synchronisers) with potential use in their Elastic Clock technology. An R&D project has been started with Alex Yakovlev.
- TIMA, INPG, Grenoble, France (Professor Marc Renaudin, marc.renaudin@imag.fr) have been involved in developments of arbiter design techniques and collaboration for the book [1].

3. Explanation of Expenditure

Staff: The project staff requirement was 1 Senior RA (Emeritus Prof D.J. Kinniment) and 2 PhD students. It was however possible to support three students, Zhou, Minas and Heron. Mr Heron was involved as part-time PhD student. In June 2007 he passed away. The additional research help was provided by Dr D. Shang, a senior RA, who was employed on SYRINGE for 5 months to help developing links between work on synchronisers, arbiters, NoCs and self-timed event processors (bridging with the NEGUS, EP/C512812/1) and STEP (EP/E044662/1) projects. A one-off payment of a bursary has been made to support Ms Dasgupta, whose PhD research on GALS has been very useful to SYRINGE. Overall the salaries budget has been overspent by 2%.
Travel, Consumables, Exceptional: Travel budget has been overspent by 25%, this was due to the larger than planned involvement of staff and excellent opportunities for dissemination of our research internationally (e.g. presentations at several ASYNC Symposia). Consumables have been underspent by 15% due to some savings in Europractice chip fabrication. Exception items (student fees) were underspent by 5%.
Overall: The overall budget is underspent by £463.24.

4. Further Research or Dissemination Activities

The project has been extremely successful in generating further research and dissemination. It helped to form baseline for the proposal of the project STEP awarded in 2007 (EP/E044662/1) and for a new proposal on Reliable Cell Design for Variable Processes, due to be submitted to EPSRC. This project has been influential in securing the organisation of the IEEE International Symposia, ASYNC'08 and NOCS'08, held in Newcastle in April 2008, and produced results of the highly rated tutorial on Metastability and Synchronisation in SoCs and NoCs by David Kinniment (see http://async.org.uk/async2008/, http://async.org.uk/nocs2008/, http://async.org.uk/nocs2008/keynote-tutorials.html). The implementations in VLSI chips and FPGA have been demonstrated in the above-mentioned tutorial and at the ASYNC Symposia chip exhibitions.

SYRINGE Publications (main 5 publications marked with *)

Books

1. (*) D.J. Kinniment. Synchronization and Arbitration in Digital Systems, Wiley and Sons, 2007 (with contributions from A.Bystrov, M. Renaudin, G. Russell and A. Yakovlev).

Journal papers

2. (*) D.J. Kinniment, C.E. Dike, K. Heron, G. Russell and A. Yakovlev, Measuring Deep Metastability and Its Effect on Synchronizer Performance, IEEE Transactions on VLSI Systems, vol. 15, no. 9, pp. 1028-1039, September 2007.
3. (*) J. Zhou, D.J. Kinniment, C.E. Dike, G. Russell and A.V. Yakovlev, On-chip Measurement of Deep Metastability in Synchronizers, IEEE Journal of Solid-State Circuits, vol. 43, no. 2, February 2008, pp. 550-557.

4. S. Dasgupta, D. Potop-Butucaru, B. Caillaud and A. Yakovlev. Moving from Weakly Endochronous Systems to Delay-Insensitive Circuits, Electronic Notes in Theoretical Computer Science, Vol. 146, No.2, January 2006, pp 81-103 (also presented in the Proceedings of the Second Workshop on Globally Asynchronous, Locally Synchronous Design (FMGALS 2005)).
5. M.A. Abas, G. Russell and D.J. Kinniment, Built-in time measurement circuits – a comparative design study, IET Computers and Digital Techniques 2007, vol. 1, No.2, pp. 87-97.
6. M.A. Abas, G. Russell and D.J. Kinniment, Embedded high-resolution delay measurement using time amplification, IET Computers and Digital Techniques 2007, vol. 1, No.2, pp. 77-86.
7. S. Dasgupta and A.Yakovlev. Comparative analysis of GALS clocking schemes, IET Computers and Digital Techniques, vol. 1, No.2, pp. 59-69, March 2007.
8. C. S. D'Alessandro, D. Shang, A. Bystrov, A.V. Yakovlev and O. Maevsky. Phase-Encoding for On-Chip Signalling, IEEE Transactions on Circuits and Systems-I: Regular Papers, Vol. 55, No.2, March 2008, pp. 535-545.

Conference papers (formally refereed)

9. (*) J. Zhou, D.J. Kinniment, G. Russell and A. Yakovlev, A Robust Synchronizer Circuit, Proceedings of the IEEE Computer Society Annual Symposium on VLSI (ISVLSI'06), Karlsruhe, Germany, March 2006, pp. 442-443.
10. (*) D. Kinniment, K. Heron, and G. Russell, Measuring Deep Metastbility, Proceedings of the IEEE Int Symposium on Advanced Research in Asynchronous Systems and Circuits (ASYNC'06), March 2006, Grenoble, IEEE CS Press, pp 2-11 (**Best Paper Finalist Award**).
11. S. Dasgupta and A. Yakovlev. Modeling and Performance Analysis of GALS Architectures, Proc. 2006 IEEE Int. Symposium on System-on-Chip, Tampere, November 2006, pp. 187-190.
12. C. D'Alessandro, N. Minas, K. Heron, D. Kinniment and A.Yakovlev, NoC Communication Strategies using Time-to-Digital Conversion, Proc. 1st ACM/IEEE Int. Symposium on Networks on Chip, Princeton, USA, May 2007, IEEE CS Press, pp. 65-74.
13. N. Minas, M. Marshall, G. Russell and A. Yakovlev. FPGA Implementation of an Asynchronous Processor with Both Online and Offline Testing capabilities, Proceedings of the 14th IEEE International Symposium on Asynchronous Circuits and Systems, Newcastle upon Tyne, UK, April 2008, pp. 128-137.
14. J. Zhou, D. Kinniment, G. Russell and A. Yakovlev. Adapting Synchronizers to the Effects of On Chip Variability, Proceedings of the 14th IEEE International Symposium on Asynchronous Circuits and Systems, Newcastle upon Tyne, UK, April 2008, pp. 39-47.
15. N. Minas, D.J. Kinniment, G.Russell and A. Yakovlev. High Resolution Flash Time-to-Digital Converter with Sub-Picosecond Measurement Capabilities, Proc. 2008 IEEE Int. Symposium on System-on-Chip, Tampere, Finland, November 2008, pp. 81-84.

Conference papers (not formally refereed)

16. N. Minas, D.J. Kinniment, G. Russell, A.Yakovlev, "Metastability in FPGA Devices", 18th UK Asynchronous Forum, Newcastle, September 2006.
17. Sohini Dasgupta, Alex Yakovlev, "Modeling and Performance Analysis of GALS Architectures", NCL-EECE-MSD-TR-2006-114, Microelectronic System Design Group, School of EECE, University of Newcastle upon Tyne, April 2006 (also presented in 18th UK Asynchronous Forum, Newcastle, September 2005.)
18. J.Zhou, D. Kinniment, G. Russell and A.Yakovlev. Design of fast and reliable synchronizers for NOCs, DATE 2006 Friday Workshops, Workshop on Future Interconnects and Networks on Chip, Munich, March 2006, Poster session.
19. Jun Zhou, David Kinniment, Gordon Russell, and Alex Yakovlev, On-chip Measurement of MTBF for A Robust Synchronizer, 19th UK Asynchronous Forum, London, September 2007.

SYRINGE Chip designs (see also http://async.org.uk/chip-gallery.html)

(1) SYRINGE1 chip contains a robust synchroniser which maintains the value of its metastability time constant in the event of large Vdd variations (with dynamic current control during metastability). The chip also contains an on-chip measurement circuit which extends the measurement of synchronizers into the deep metastability region.
Year: 2006. Technology: CMOS UMC 0.18um fabricated by Europractice

(2) SYRINGE2 Time-to-Digital Converter and Neuron Chip.
A High Resolution Flash Time-to-Digital Converter (TDC) was developed on a 130nm chip to investigate timing faults caused by the violation of internal timing parameters, such as clock jitter, clock skew and set-up and hold times. Results from SYRINGE2 demonstrated the possibility of measuring these timing parameters on-chip to the order of a single picosecond. The chip also contains demonstration circuits of a Leaky Integrate-and-Fire Neuron and an Asynchronous Pulse Generator for use in a biologically inspired reconfigurable neural network.
Year: 2008. Technology: UMC 0.13um through Europractice