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From low power computing to power-adaptive computing

Alex Yakovlev
Newcastle University

helped by Panagiotis Asimakopoulos and Stanislavs Golubcovs

Issues addressed in this talk

- Energy as a dynamic resource (power supply (Vdd) and consumption (Vth) variability, systems with low/bursty duty cycles, power/current spikes)
- Main focus on energy harvester based supply
- Energy flow and information flow (energy can come and go as we process data) can both affect the system behaviour
- Power adaptive computing (max power point tracking, adapting to varying Vdd, optimising duty cycles)
- System models for power adaptation (token-based, hybrid Petri nets, event-count models)
- Circuit design (AC supply, self-timed)

Messages from the ITRS Roadmap

- Non-ideal device and supply/threshold voltage scaling leads to:
  - Leakage,
  - Power management and delivery
- We're entering the 2D world of progress: "More More" (scaling factor) and "More than Moore" (functional diversification) – so scaling is not everything to battle against!
- The "More than Moore" increasingly includes non-digital aspects – RF comms, power control, passive components, sensors, actuators etc.
- Design innovations (hardware and software) will help to reduce the design costs by 50-60 times and will have increasing impact in this 2D progress

Costs of Scaling

Source: ITRS 2005	90nm	65nm	45nm
V_{TH} (V) ⇘	1X	0.85X	0.75X
I_{OFF} (nA/um) ⇧⇧	1X	~3X	~9X
Dynamic Power Density (W/cm²) ⇧	1X	1.43X	2X
Leakage Power Density (W/cm²) ⇧⇧	1X	~2.5X	~6.5X
Power Density (W/cm²) ⇧	1X	~2X	~4X
Cu Resistance (Ω) ⇧	1X	2X	4X
Interconnect RC Delay (ps) ⇧	1X	~2X	~5X
Packaging (cents/pin) ⇘	1X	0.86X	0.73X
Test (nanocents/Tx) ⇨	1X	1X	1X

To lower leakage by process one needs to give up on performance, or … do something in design

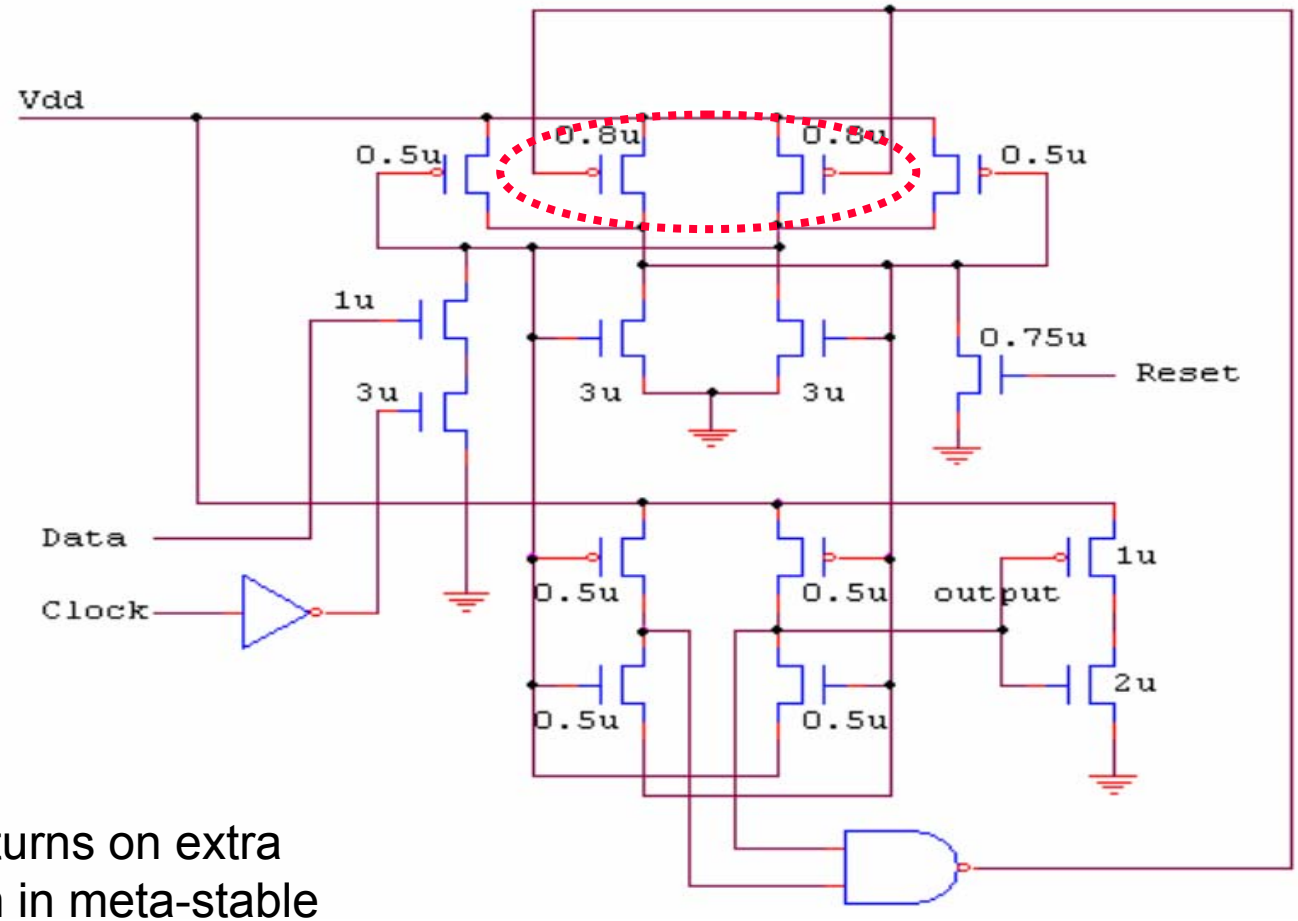
Source: Tom Williams, Synopsys

Design For Low Power

	Constant Throughput/Latency		Variable Throughput/Latency
	Design Time	Non-Active Modules	Run Time
Dynamic & Short Circuit	Logic Re-Structuring, Logic Sizing, Reduced V_{DD}, Multi-V_{DD} **2.5X**	Clock Gating **2X**	Dynamic or Adaptive Frequency & Voltage Scaling **2.5X**
Leakage	Stack Effect, Multi-V_{TH} **2X-10X**	Sleep Transistors, Multi-V_{DD}, Variable V_{TH} **10X-1000X**	Variable V_{TH} **2X-10X**

Source: J. Rabaey, UCB 2005

Robust Synchronizer (adapting performance to Vdd changes)



This circuit turns on extra power when in meta-stable state and turns off after that

Source: J.Zhou et al, Newcastle, 2007

Comparison with Jamb Latch based synchroniser

Tau (metastability time constant) vs Vdd

	Measurement Results(ps)			
Vdd(v)	Jamb latch		Robust synchronizer	
	$>10^{-14}$	$<10^{-14}$	$>10^{-14}$	$<10^{-14}$
1.8	19.44	35.55	15.27	34.92
1.7	21.75	37.29	16.53	35.76
1.6	25.64	40.93	19.38	38.25
1.5	28.77	52.36	20.29	43.07
1.4	36.22	66.17	23.75	50.36
1.35	45.43	75.35	28.51	58.19

	Simulation Results(ps)	
Vdd(v)	Jamb latch	Robust synchronizer
1.8	18.99	14.69
1.7	20.36	15.36
1.6	22.24	16.19
1.5	24.99	17.23
1.4	29.31	18.59
1.35	36.85	20.39

Portable Power Supplies

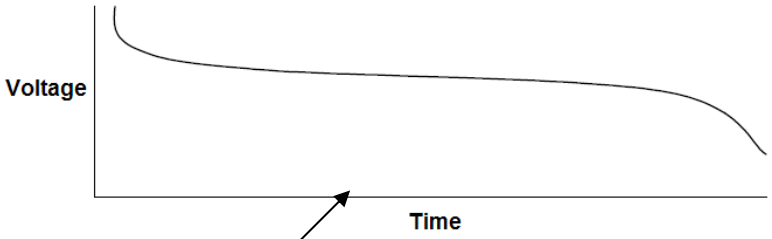
For mobile computing applications the choices of power supply are either batteries or emerging energy-harvester supplies.

Battery

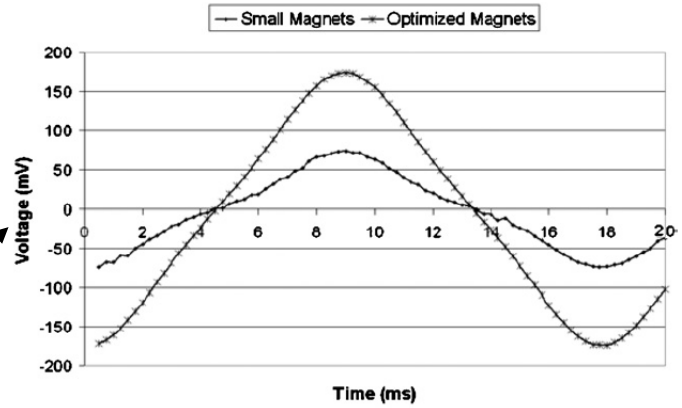
- Can supply finite energy (E) – depends on the battery capacity.
- The available power (P) can be very large.

Energy-Harvester

- Can supply infinite energy (E).
- The rate of energy production (dE/dt = P) is variable and small.



Typical Battery Discharge Curve

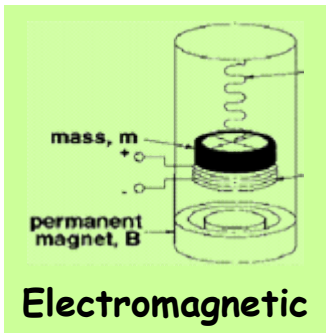


A Micro-Electromagnetic vibration harvester output voltage

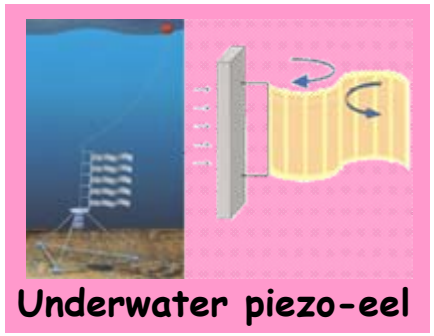
S P Beeby et al., 2007, "A micro electromagnetic generator for vibration energy harvesting", J. Micromech. Microeng. 17 (2007) 1257–1265.

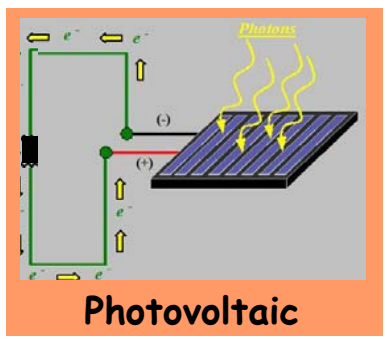
Environmental Energy Sources


Piezoelectric

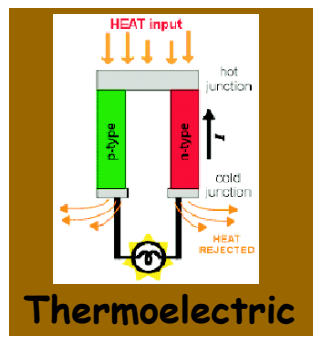


Electromagnetic


Underwater piezo-eel



Photovoltaic



Thermoelectric

Harvesting technology	Power density
Solar cells (outdoors at noon)	$15mW/cm^2$
Piezoelectric (shoe inserts)	$330\mu W/cm^3$
Vibration (small microwave oven)	$116\mu W/cm^3$
Thermoelectric (10^oC gradient)	$40\mu W/cm^3$
Acoustic noise (100dB)	$960nW/cm^3$

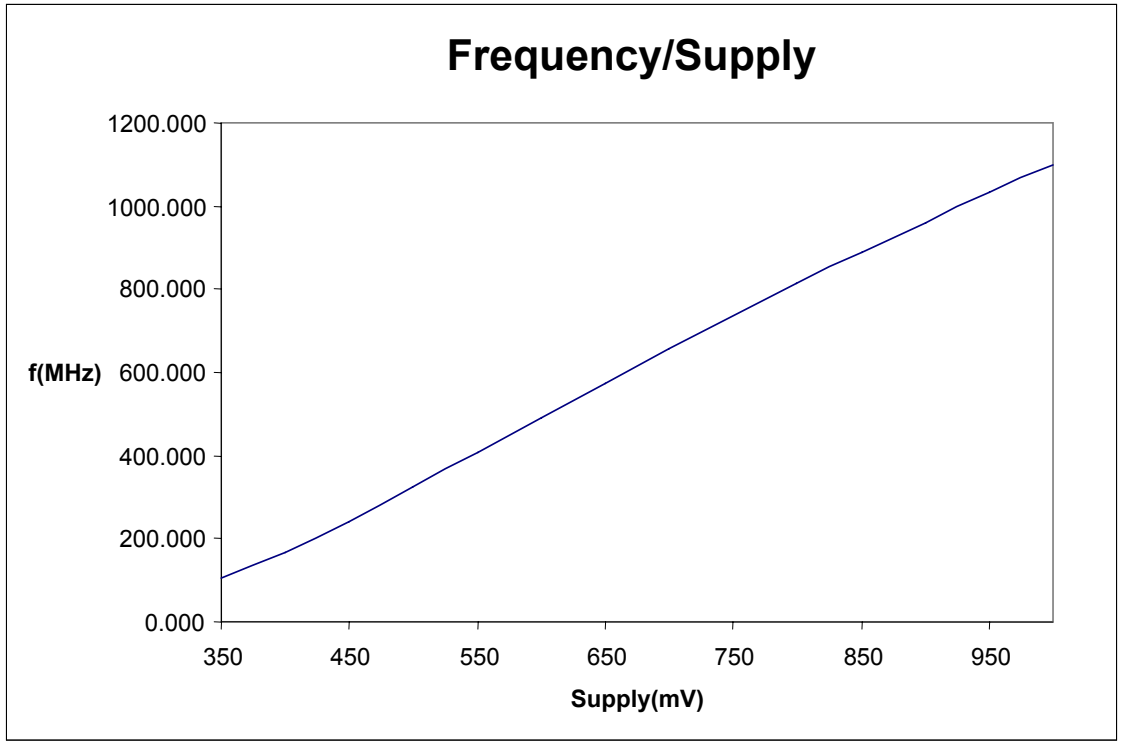
Highest power density

Source: Kansal et al, 2006

Computational circuits

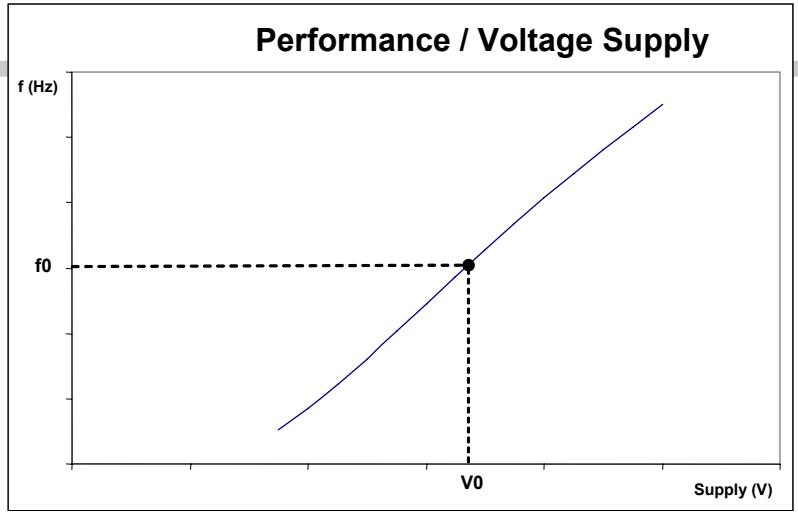
When designing computational circuits it is desirable to maximise the computational output while meeting the power supply constraints. Performance of a circuit depends on:

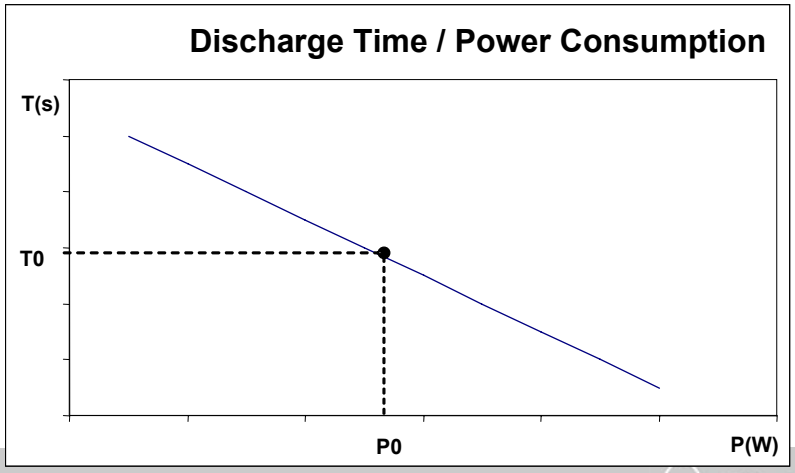
- Process technology
- Circuit architecture
- Supply voltage

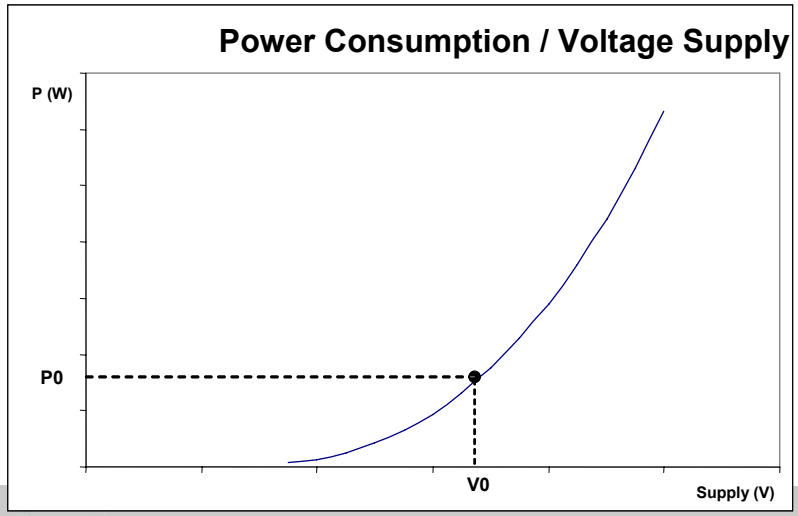


Battery Supplied Circuits

- Specifications determine the required operating time for the circuit (T0).
- Available energy E is constant so T0 determines power consumption of the circuit.
- Supply characteristics stable and pre-known.

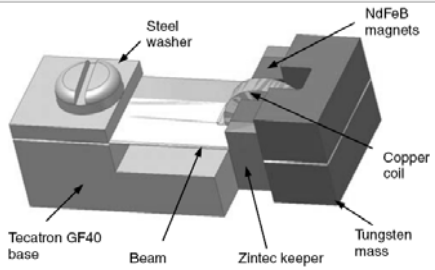




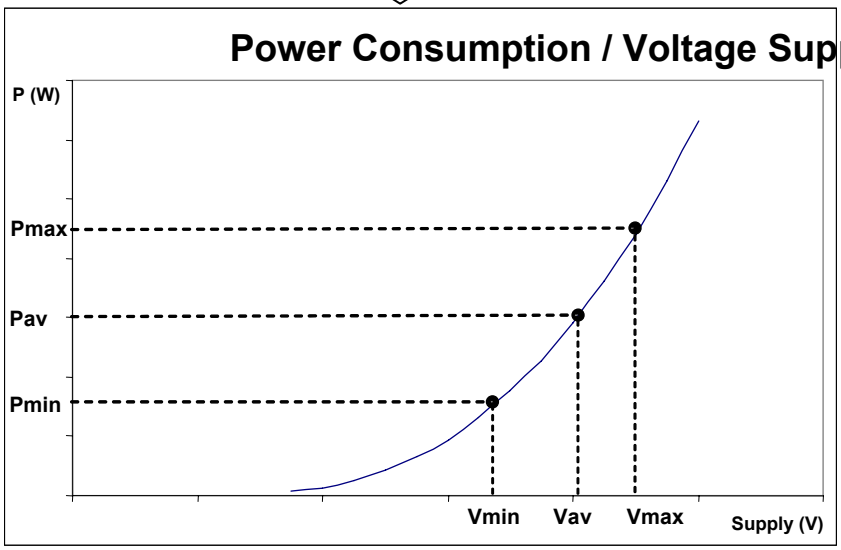


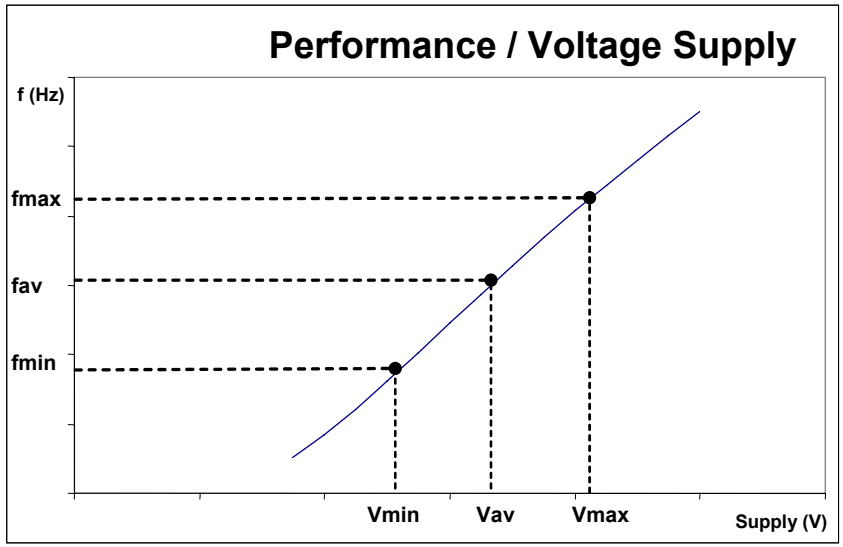
Energy-Harvester Supplied Circuits

- Specifications determine the possible output power range (Pmin, Pmax).
- Power P is variable depending on ambient conditions.
- Supply characteristics unstable and unpredictable.



S P Beeby et al., 2007, "A micro electromagnetic generator for vibration energy harvesting", J. Micromech. Microeng. 17 (2007) 1257–1265.





Circuit Designer Choices (1)

Battery Supply ⇨

- Determine from T0 the required power consumption P0.
- Design the circuit for constant P0 consumption → constant V0 supply → constant f0 performance (or apply DVS and DVFS to maximise battery life)

Energy-Harvester Supply ⇨

- Design the circuit for constant Pmin consumption → constant Vmin supply → constant fmin performance.

OR

- Track available power Paverage → change circuit consumption/performance in real-time → faverage > fmin.

Circuit Designer Choices (2)

To maximise a circuit's power utilization of a variable power output source:
- increase voltage supply of the circuit to the maximum possible value (variable voltage).
- switch on/off parts of the circuit (constant voltage).

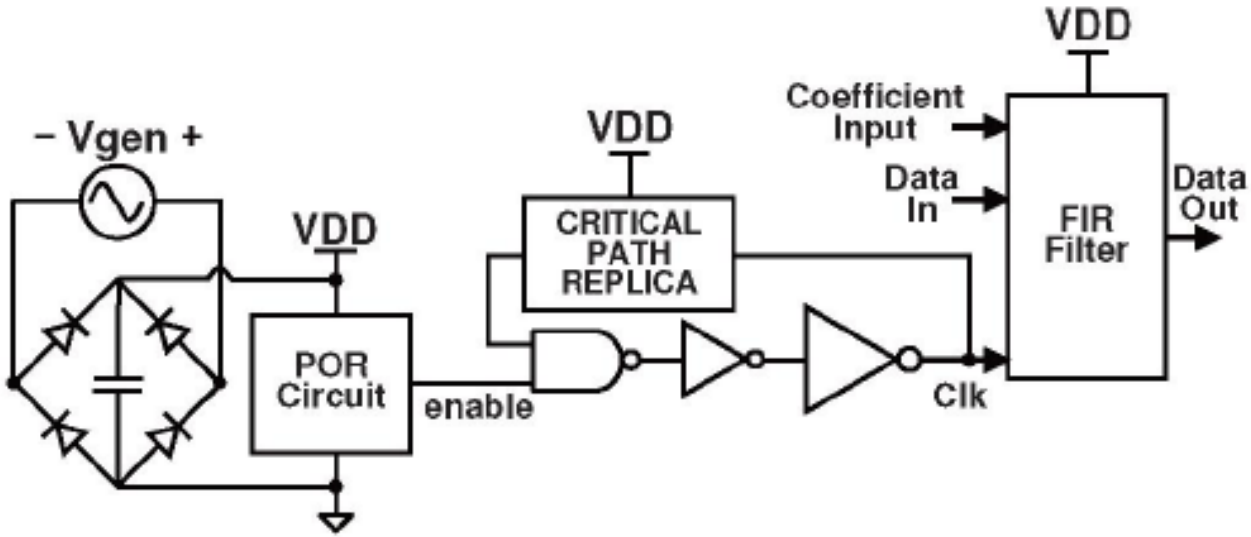
Real-time ⇦

- For both cases special controller circuits have to be developed.
- For the first case (variable voltage) self-timed circuits have an advantage → no additional circuit required to change the operating frequency.

AC supplied self-timed circuits have been demonstrated in practice.

For every power supply cycle: wake up the circuit, perform computation and shut down the circuit – hence, power-on reset needed.

AC-powered self-timed circuit

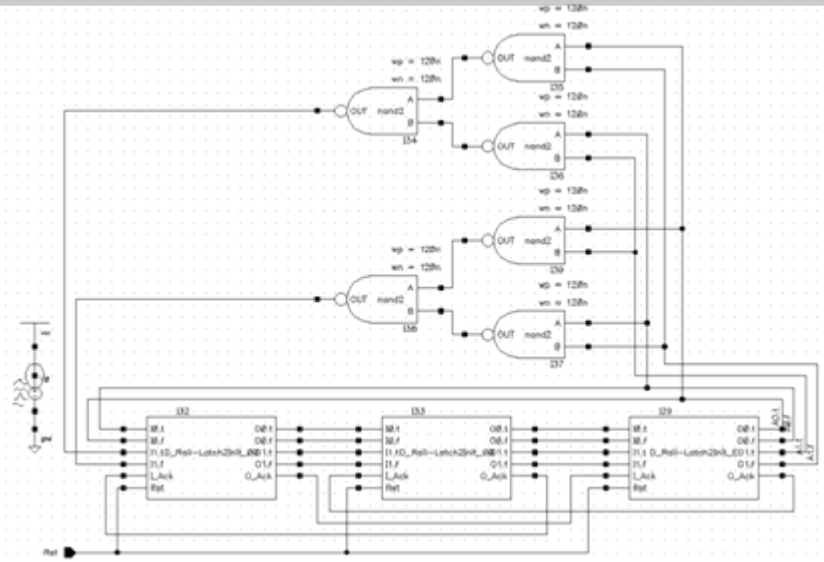


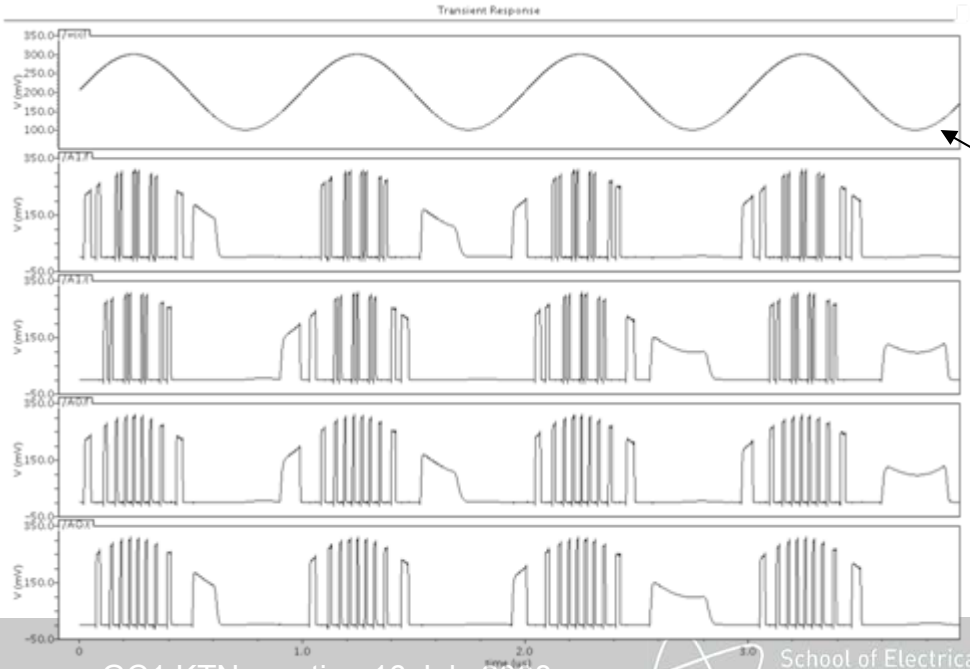
Fast Power-on Reset (4.1nW),
3T DRAM to keep state across supply cycles,
135K transistors in 180nm CMOS
Can supply 250KHz on all process corners for <=50C

J Wenck, R Amirtharajah, J Collier and J Siebert, 2007, “AC Power Supply
Circuits for Energy Harvesting”, 2007 IEEE Symposium on VLSI Circuits, 92-93.

Closer look at AC-powered self-timed logic

2-bit Sequential Dual-rail
Asynchronous Counter





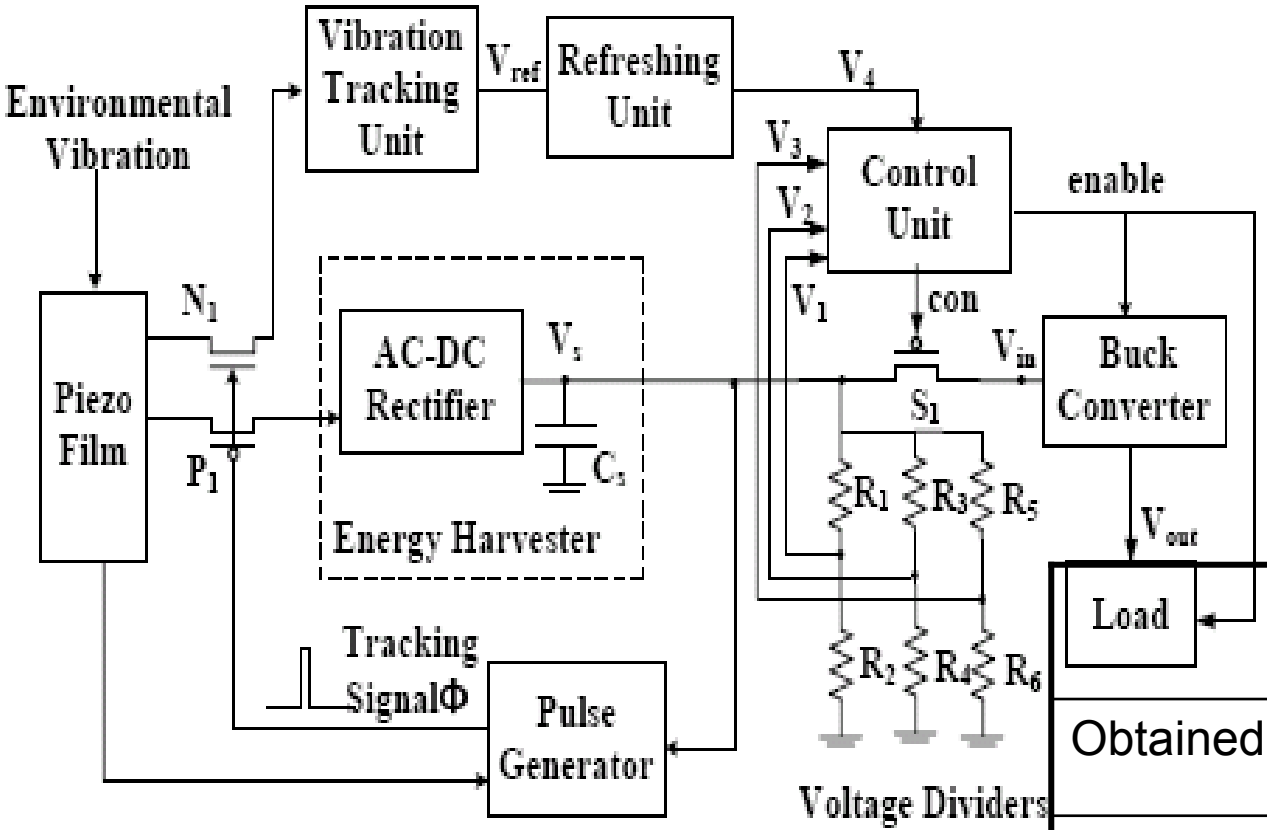
Supply: AC 200mV±100mV
Frequency: 1Mhz

Energy Harvesting Methods

- System design aspects:
  - Voltage-current conversion
    - Linear regulators – low efficiency
    - Switching (buck- higher eff., boost – lower eff.)
  - Maximum Power Point Tracking (MPPT)

  (e.g. for AC max power if rectifier voltage is ½ open circuit voltage)
    - Measurement and control
    - Hardware and software solutions (overhead is an issue!)
  - Energy Storage (battery or supercap's)
- Power Management
  - Harvester-based as opposed to (traditional) battery-based
  - Energy neutrality models

Piezoelectric Energy Harvester with MPPT



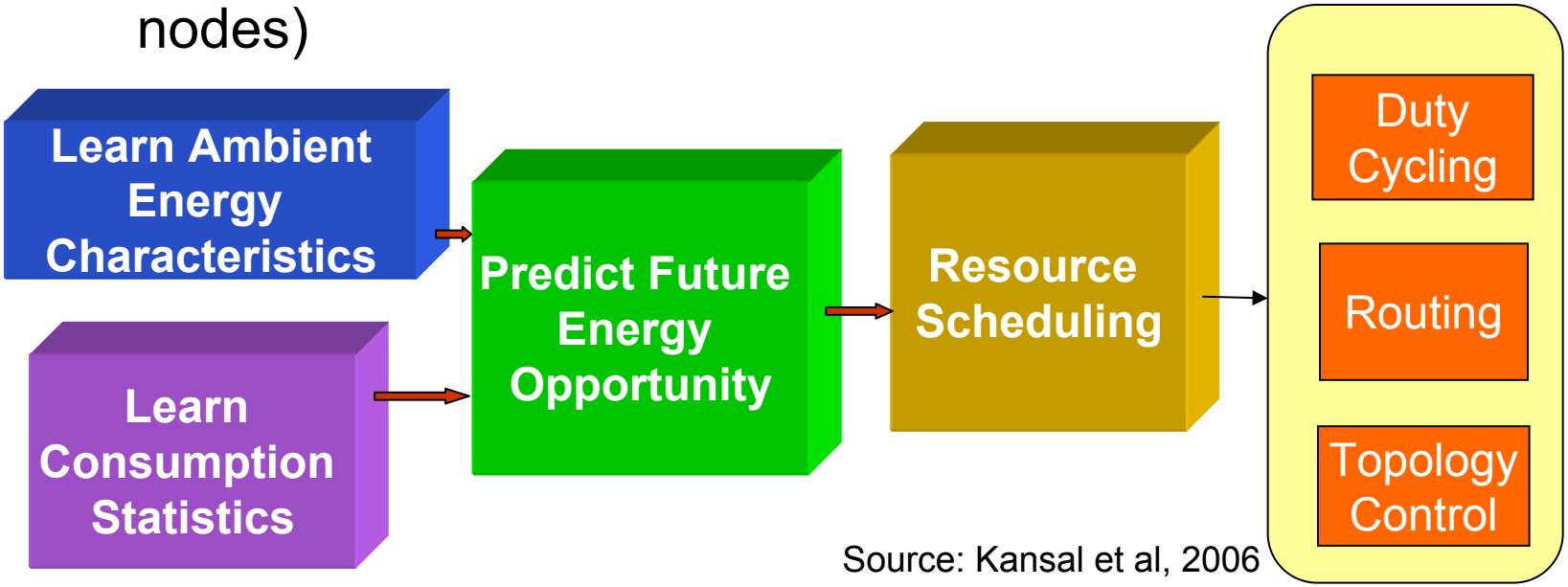
Simple MPPT scheme with
90% efficiency,
and overall power conversion
Efficiency at 70%

Load	60Hz, 100uA	60Hz, 70uA
Obtained Vs	3.95V	2.81V
Harvested Power	110uW	55uW

Source: Chao et al, 2007

Harvesting-aware Power Management (for sensor networks)

- Goal is not power minimization but energy neutrality
  - Indefinitely long lifetime, limited only by h/w longevity
  - Subject to performance constraints and optimization
- Unknown spatio-temporal profile of harvested energy
  - At a node: adapt *temporal* profile of workload
  - In a network: adapt *spatial* profile of workload (across nodes)



Source: Kansal et al, 2006

Understanding Energy Neutrality: A Harvesting Theory

- Condition for energy neutrality with a battery with roundtrip efficiency η and leakage ρ_{leak} is

$$\eta \int_0^T [P_s(t) - P_c(t)]^+ dt - \int_0^T [P_c(t) - P_s(t)]^+ dt - \int_0^T \rho_{leak} dt + B_0 \geq 0 \quad \forall T \in [0, \infty)$$

- Modeling bursty energy source $P_s(t)$ and consumer $P_c(t)$

$$\int_0^T P_s(t) \geq \rho_1 T + \sigma_1 \qquad \int_0^T P_s(t) \leq \rho_1 T - \sigma_2 \qquad \int_0^T P_c(t) \geq \rho_2 T + \sigma_3$$

- Sufficient conditions for energy neutrality

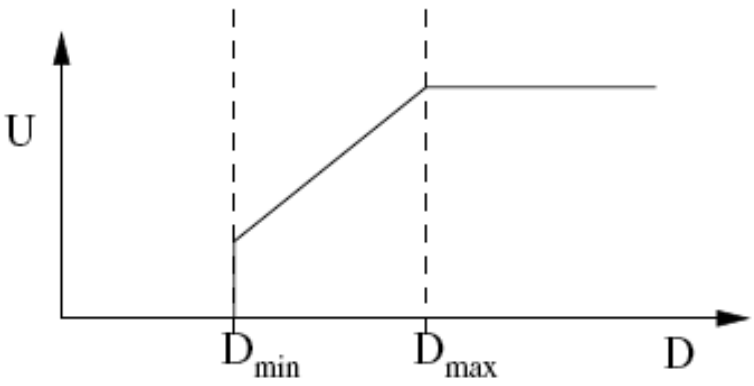
$$\rho_2 \leq \eta \rho_1 - \rho_{leak}$$
$$B_0 \geq \eta \sigma_2 + \sigma_3$$
$$B \geq B_0$$

Source: Kansal et al, 2006

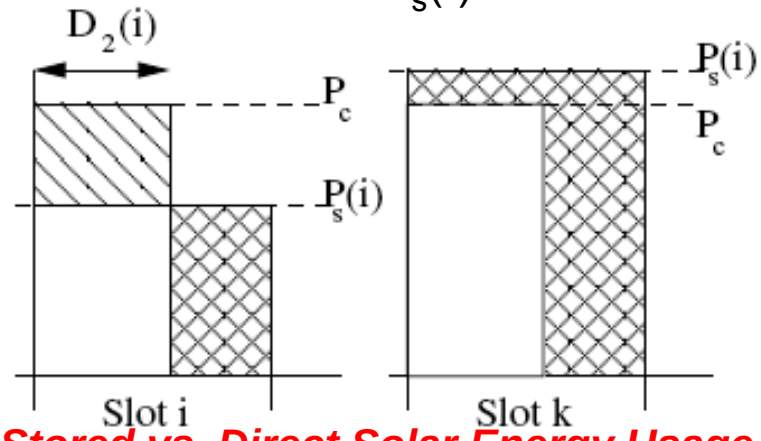
At a Node: *Harvesting-aware Duty Cycling*

Source: Kansal et al, 2006

- Duty cycling between active and low-power states for power scaling
- Approach
  - System utility function U(D) as a function of D
  - Time slots ΔT with duty cycle calculated for a window of N_w slots
    - $\Delta T x N_w$ = a natural energy neutral period such as 1 day
  - At start of window predict harvested energy level for next $\Delta T x N_w$ slots using history and external weather predictions
  - Calculate D for N_w slots for max U subject to energy neutrality
  - Revise duty cycle allocations based on actual observed $P_s(t)$



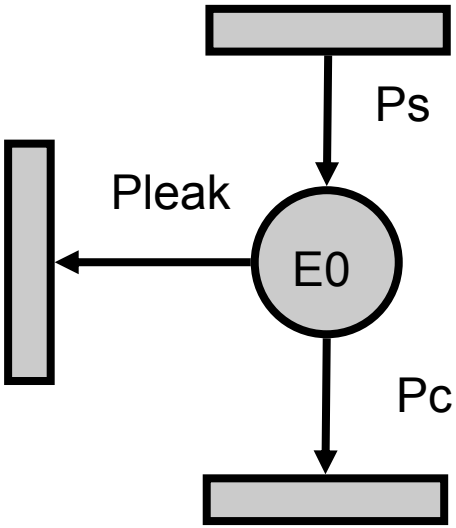
Application Utility vs. Duty Cycle



Stored vs. Direct Solar Energy Usage

Dynamic Models for power-adaptive computing

- Energy neutrality modelling (e.g. in Petri nets)



Simplified energy neutrality conditions:

Ps>=Pc+Pleak

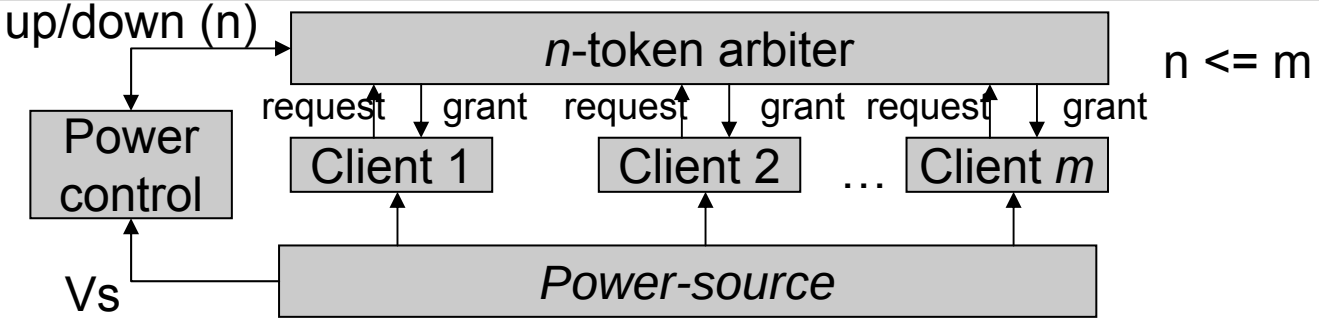
E0>= Pc*tc

Emax.capacity>=E0

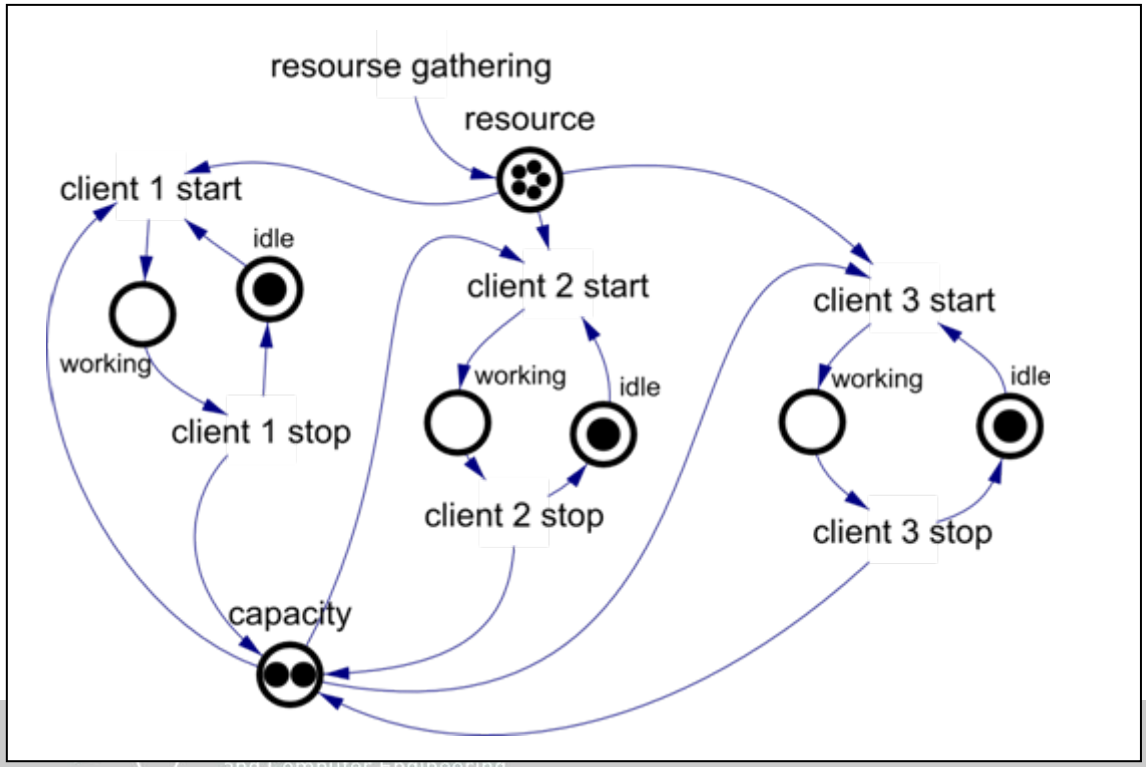
Relevant qualitative Petri net properties: concervativeness, boundedness

Performance analysis (and optimisation): (minimising) cycle time under given power supply parameters

Resource-based power gating and Petri net model



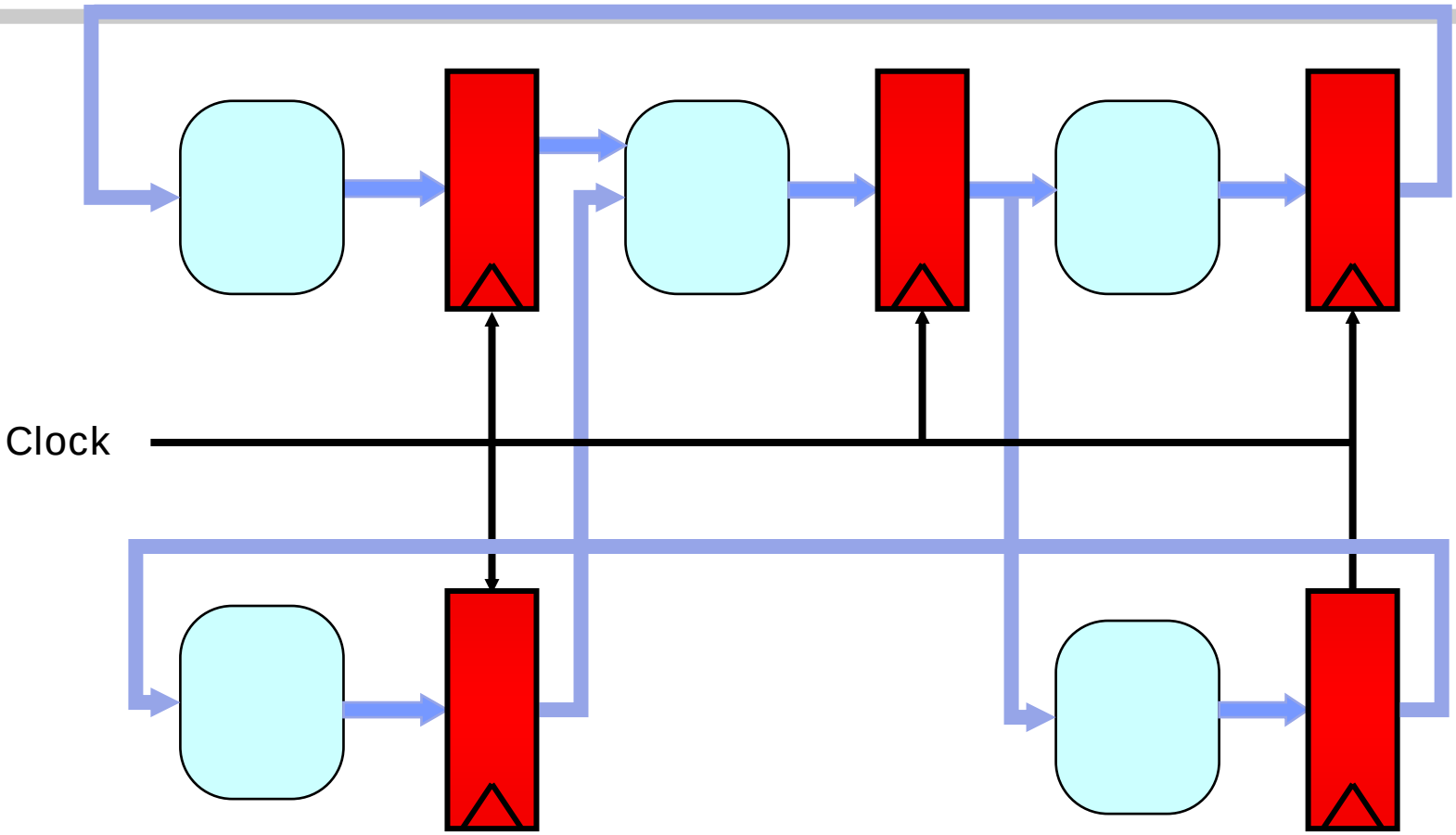
power is gated to client upon grant arrival



On Design Tools

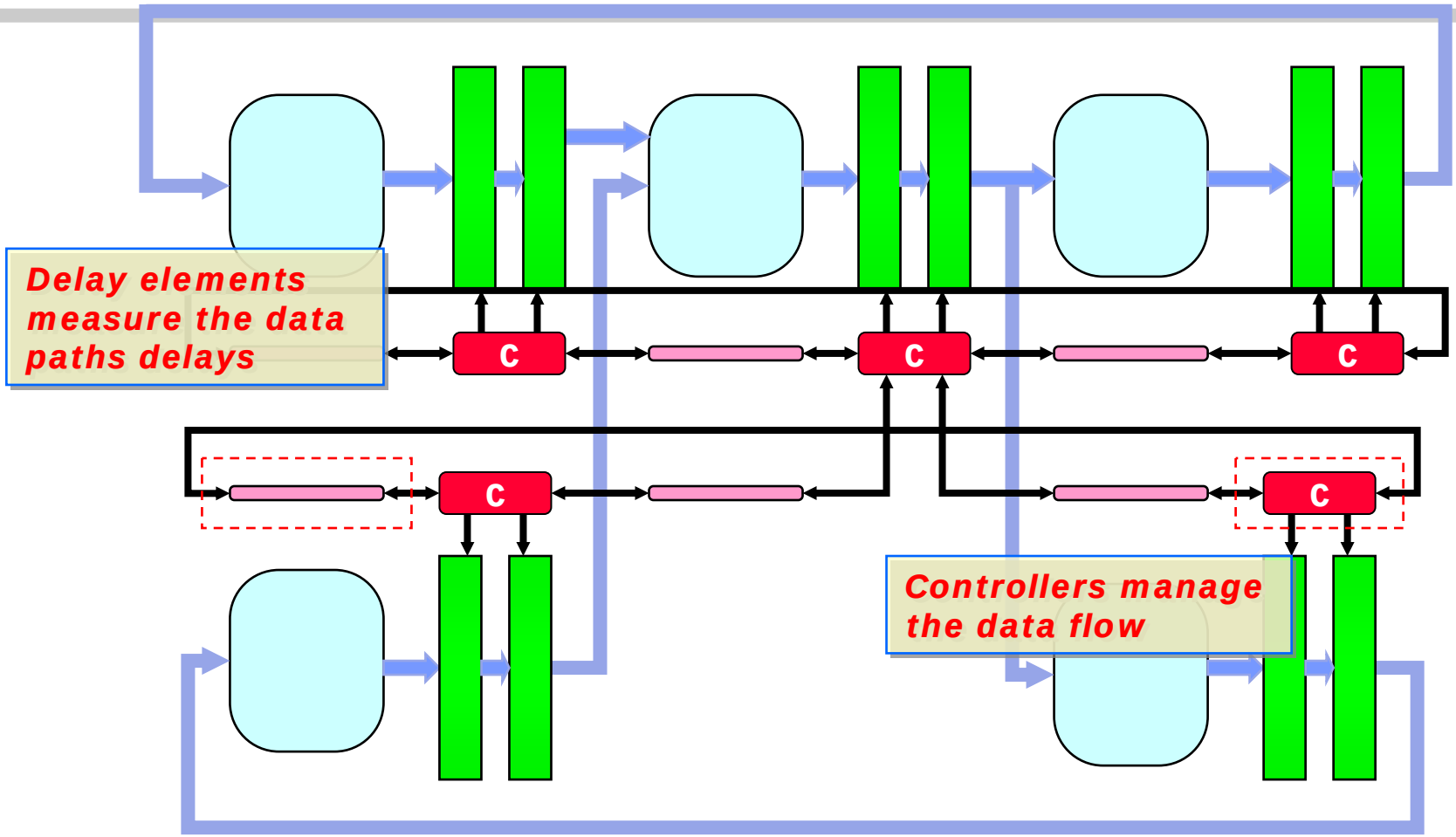
- Available tools only partly support design of adaptive power circuits and systems:
  - Self-timed logic design (upcoming, e.g. TiDE toolset from Handshake Solutions based on CSP, and Elastix tools based on Desynchronised RTL); tools needed for designing interfaces between clocked and self-timed logic
  - Tool support for power-gated and variable power logic (cf. voltage aware simulators from Synopsys)
  - No tool support for holistic harvester-driven electronics co-simulation (could be based on AMS VHDL)
  - New logic libraries are needed for variable Vdd and ultra low power (e.g. subthreshold logic)
- Significant amount of pre-CAD research is still needed!

RTL with global clocks



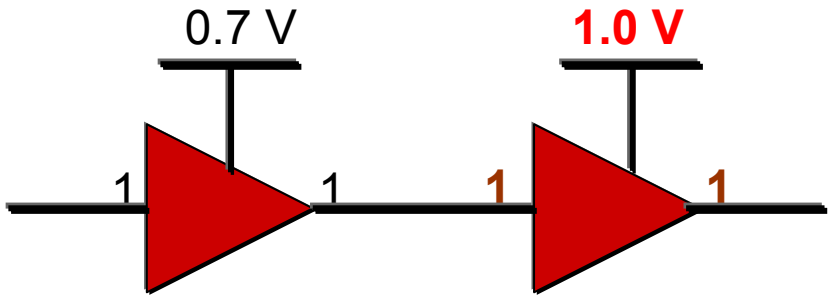
Source: Elastix Corp.

Elastic “clocks”

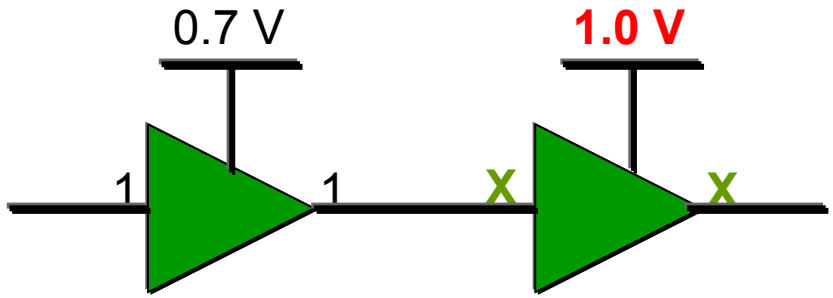


Source: Elastix Corp.

Voltage-Aware Simulation is now necessary!



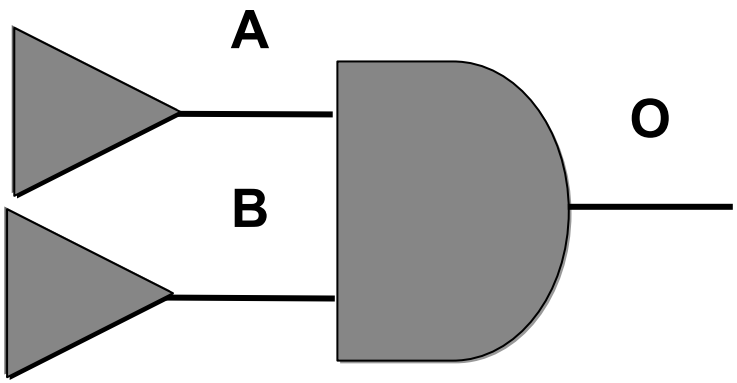
Traditional Simulators are not voltage aware



Voltage-Aware Simulators are Electrically Accurate

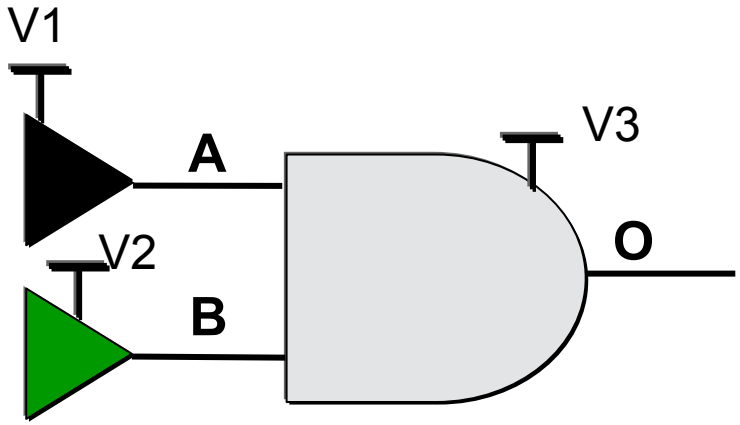
Source: Tom Williams, Synopsys

Voltage Aware Boolean Analysis (MVSIM)



A	B	O
0	0	0
…	…	…
1	1	1

Traditional Boolean Analysis :
Implicit, homogenous, always on voltage



V1	V2	V3	A	B	O
			0	0	0
			…	…	…
			…	…	…
			1	1	X

Voltage-aware Boolean Analysis:
Dynamic, Variable voltages as real numbers

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In conclusion …

- Other examples of self-timed power-adaptive designs: Async-RFID, Automatic power regulation based on asynchronous activity detection
- Power adaptation can be at many levels of abstraction, from simple components (library cells), to circuits (nodes) and complex networks
- Power efficiency is a key to deciding how complex the adaptation algorithm can/should be
- Mixed sources, battery plus harvesting, will call for new models of energy and resource neutrality, new power management optimisation algorithms. It is important to find the right metrics such as utility on duty cycle
- More research is needed on power-adaptive signal processing and comms, power-adaptive fault-tolerance, power-adaptive security …

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Backup slides

Cost of Scaling

Source: ITRS 2005/2006	90nm	65nm	45nm
Device Length (nm) ⇩	1X	0.7X	0.5X
Delay (ps) ⇩	1X	0.7X	0.5X
Frequency (GHz) ⇧	1X	**1.2X**	**1.45X**
Integration Capacity (BTx) ⇧	1X	2X	4X
Capacitance (fF) ⇩	1X	0.7X	0.5X
Die Size (mm^2) ⇨	1X	**1X**	**1X**
Voltage (V) ⇘	1X	**0.85X**	**0.75X**
Dynamic Power (W) ⇘	1X	**> 0.7X**	**>**
Manufacturing (microcents/Tx)	1X	0.35X	0.12X

⇩

Source: Tom Williams, Synopsys

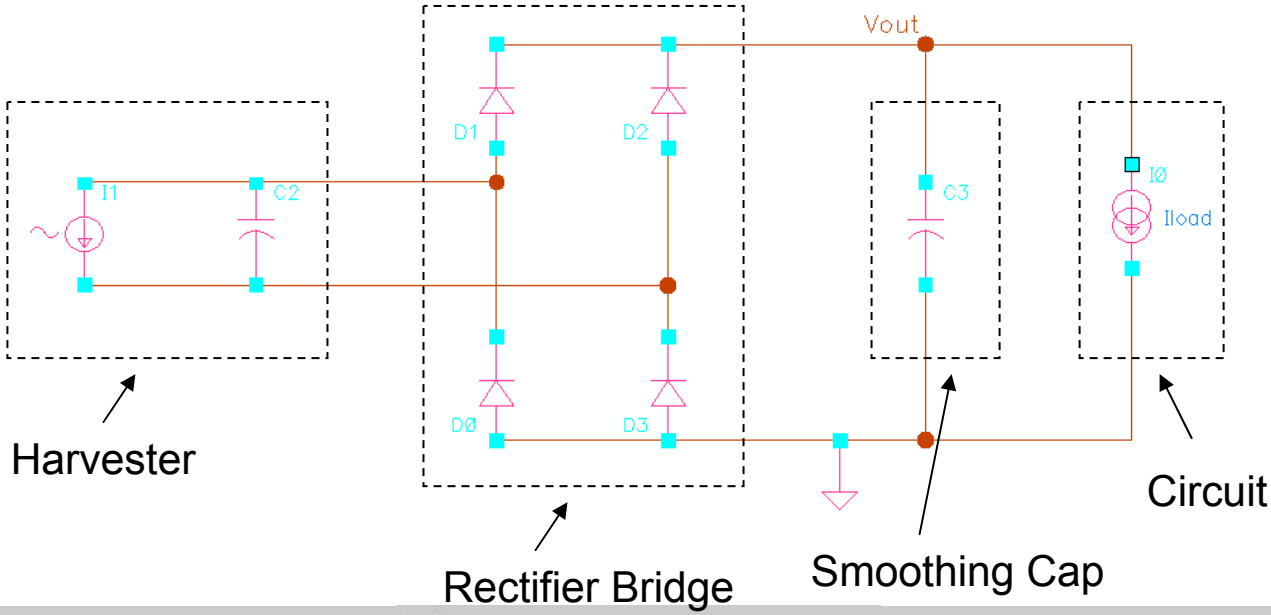
Energy-Harvester Simulations (1)

In practice things can be more complicated. In a piezoelectric energy-harvester, the voltage/power output can change depending on:

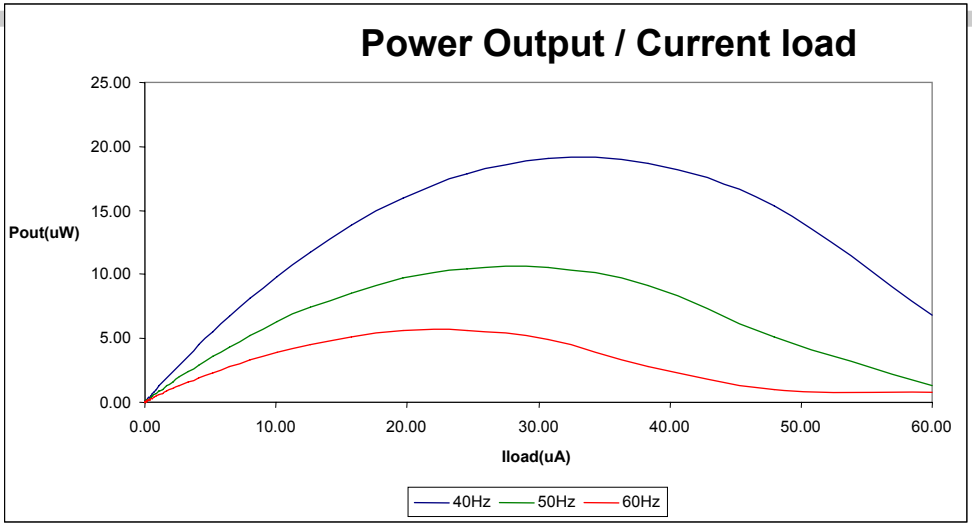
- Excitation amplitude
- Excitation frequency
- Current load

Environment

Circuit

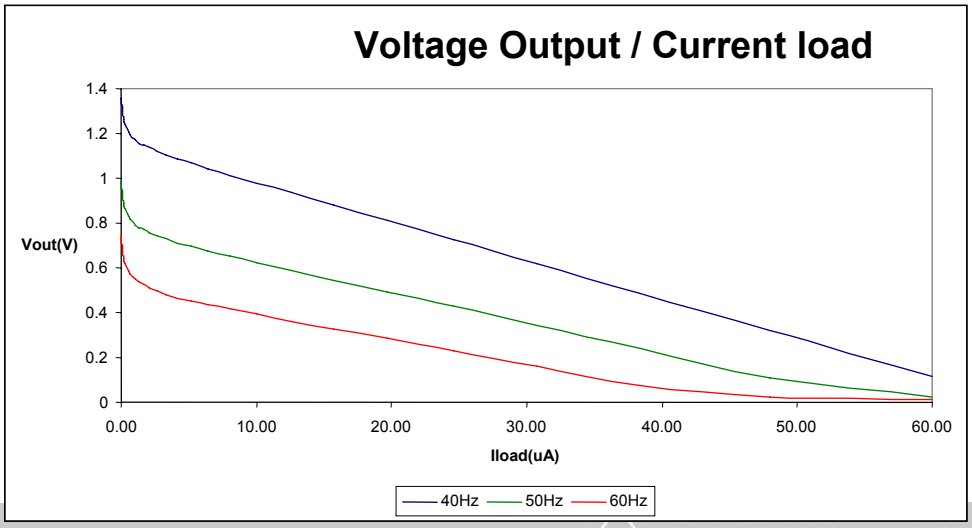


Energy-Harvester Simulations (2)



- Output power changes with different current loads

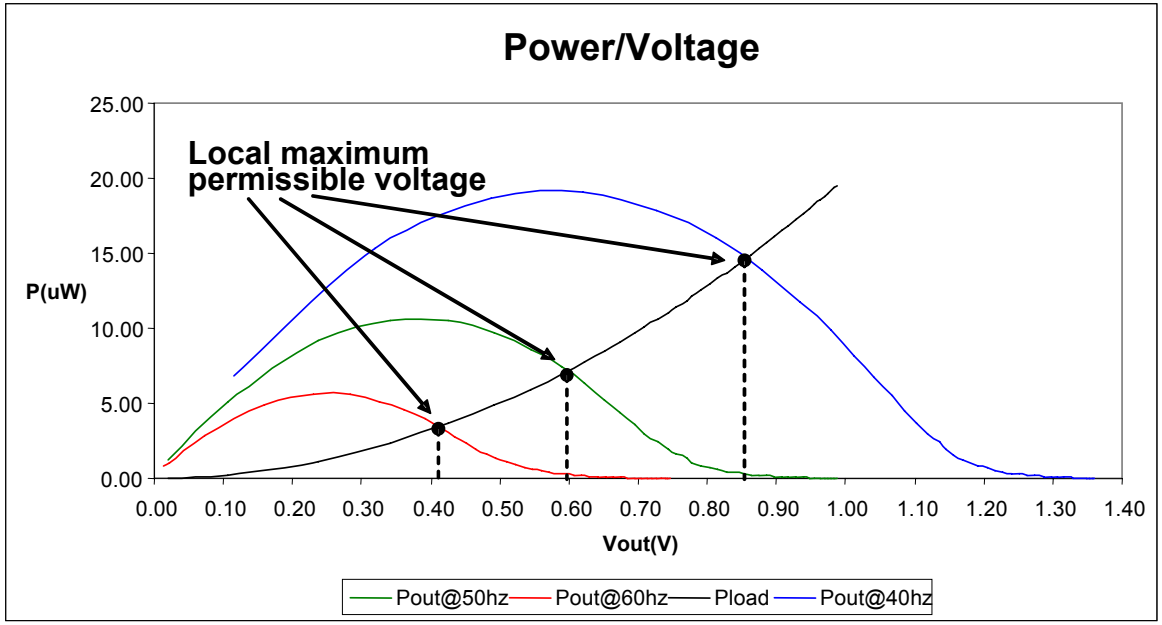
+



- Output voltage changes with different current loads

Maximizing Computational output (1)

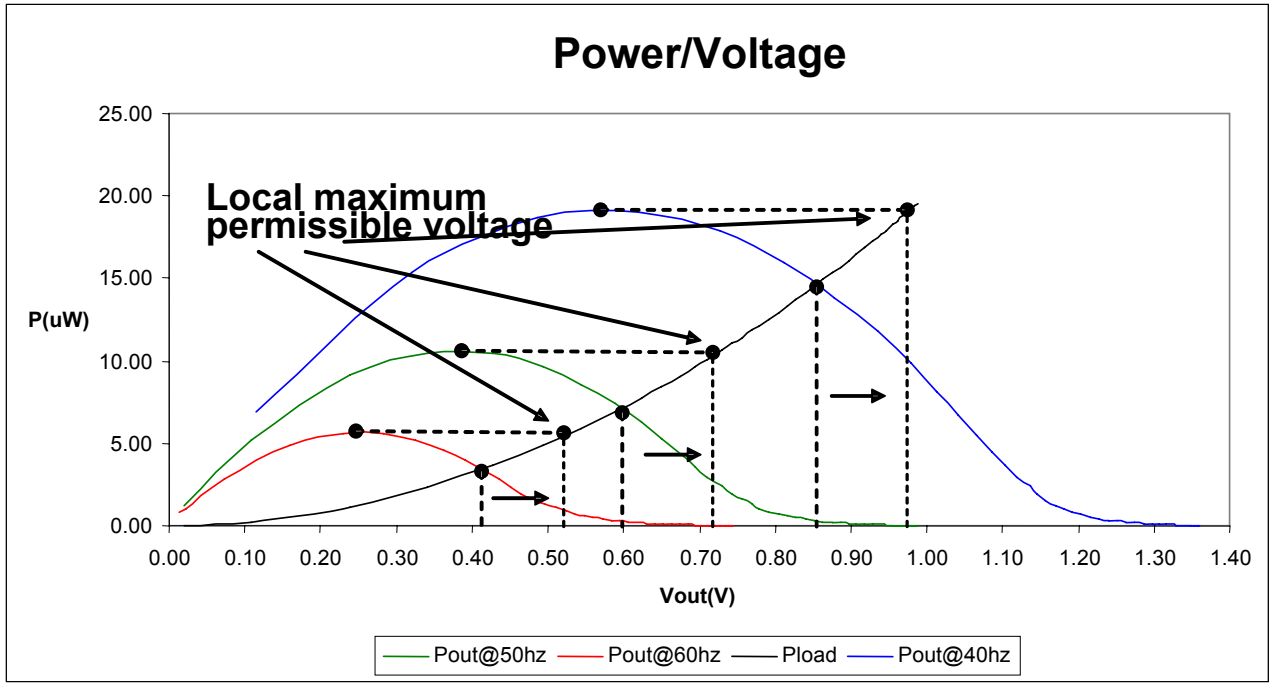
Case 1: Circuit supply voltage = Harvester output voltage.



- The maximum voltage a circuit could operate at, changes with different excitation frequencies.
- To maximize computational output, the circuit must be supplied by the maximum permissible voltage level for each excitation frequency.
- No special method required for tracking voltage, the harvester-circuit system can inherently adjust to the ideal voltage level.

Maximizing Computational output (2)

Case 2: Circuit supply voltage can have any value.



- Supplying the circuit with the largest voltage possible, independently from the harvester output level, could provide additional performance gains.
- Special power adaptive circuit has to be developed to perform that functionality.

Maximizing Computational output (3)