Capacitor Discharging through Asynchronous Circuit Switching

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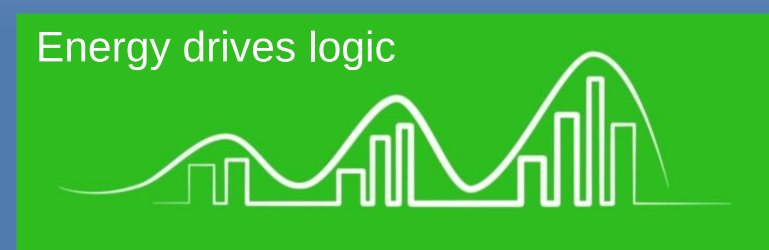
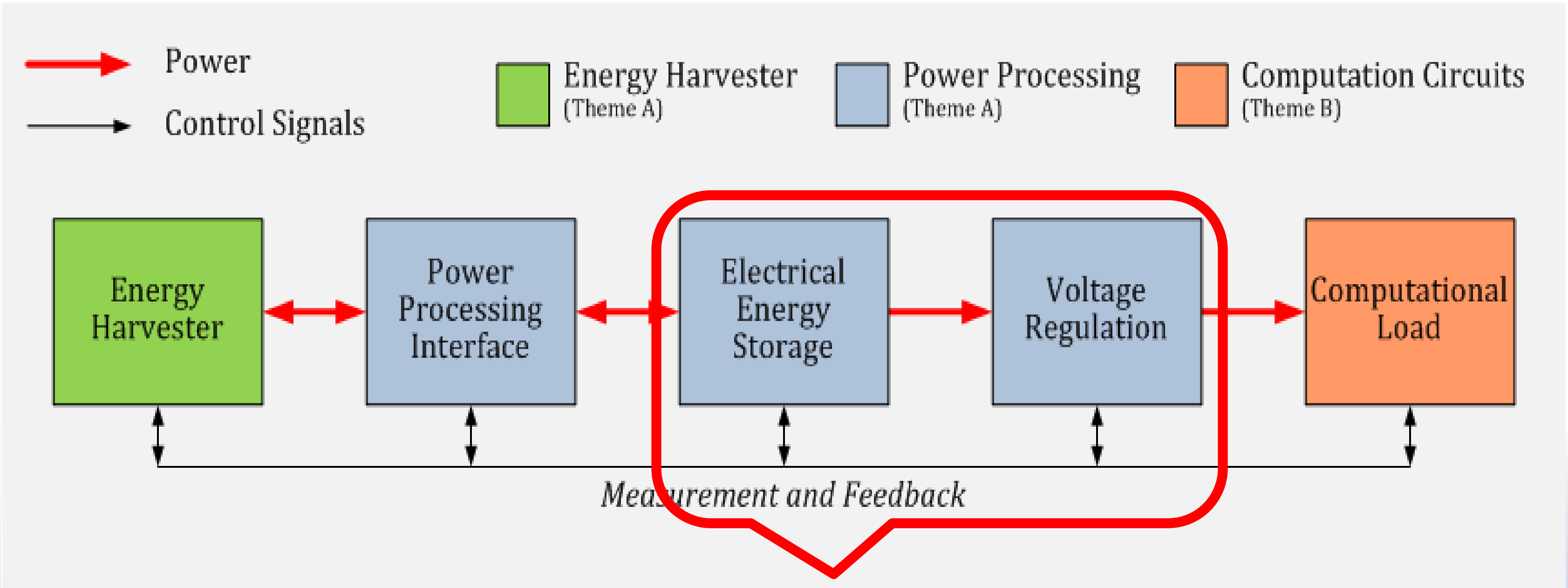


ASYNC'13: Santa Monica, May 20, 2013

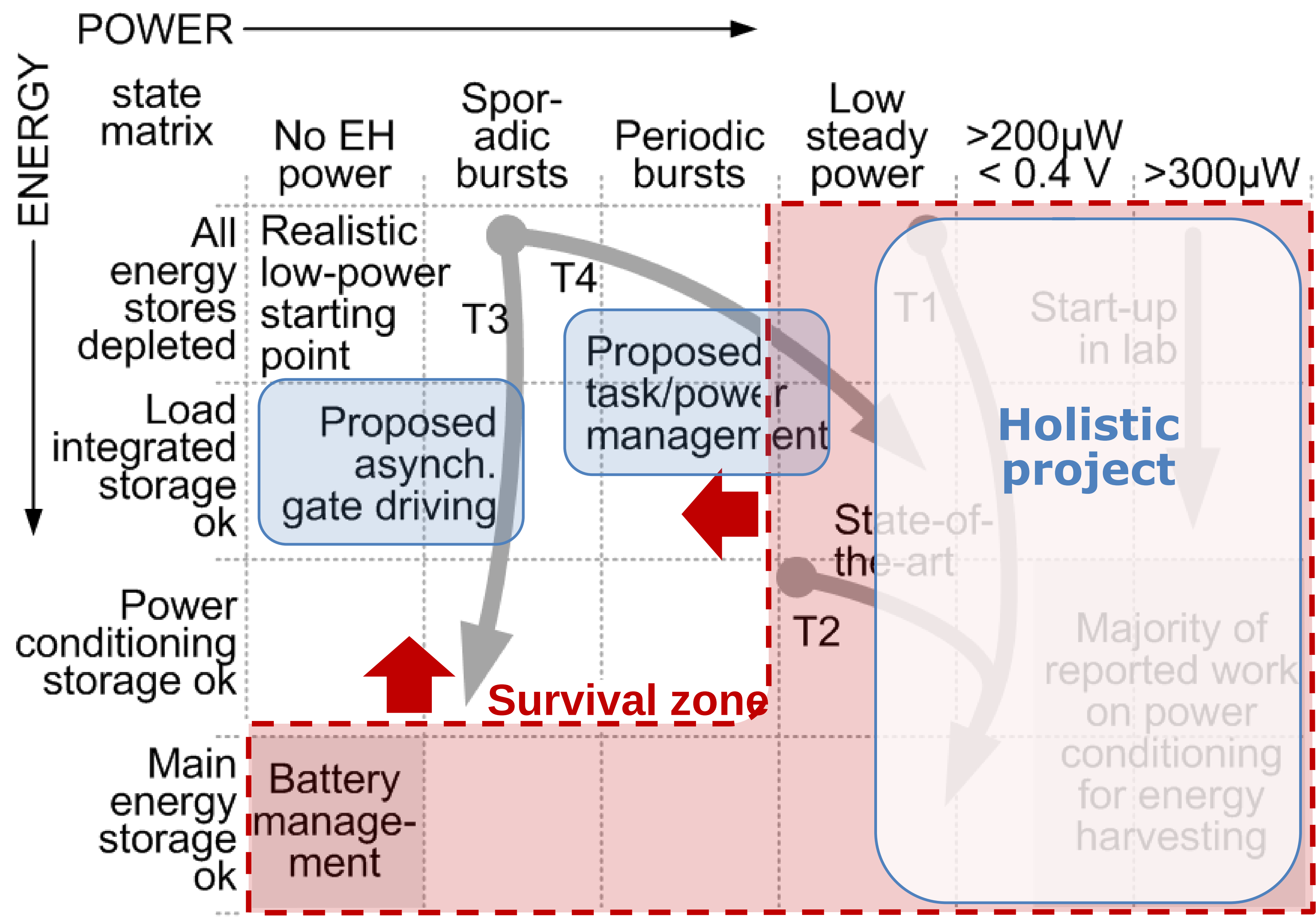
Outline

- **Context**: Energy harvesting systems
- **Origin of the problem**: Reference-free voltage sensor, Analysis Issue
- **Capacitor and Ring Oscillator**: dynamic switching process
- **Circuit Model**: Charge equilibrium and switching index
- **Solutions** for super-threshold and sub-threshold regions
- **Discussion** – can we extend this method to a more general characterisation of "energetic effort"?
- **Conclusion**

Energy harvesting systems



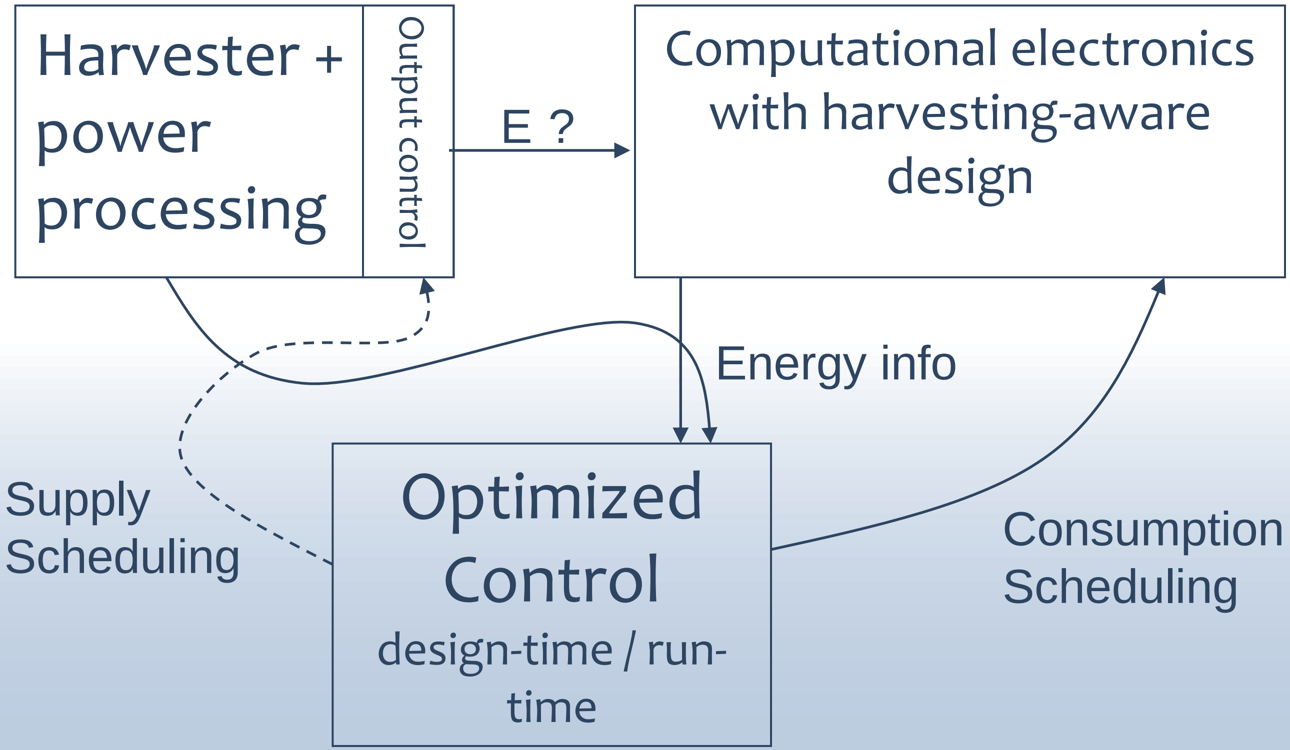
Sporadic source of energy does not allow for fancy power processing and therefore large storage.



POWER
ENERGY
state matrix
No EH power
Spor-adic bursts
Periodic bursts
Low steady power
>200µW < 0.4 V
>300µW
All energy stores depleted
Load integrated storage ok
Power conditioning storage ok
Main energy storage ok
Realistic low-power starting point
T3
T4
T1
T2
Start-up in lab
Proposed asynch. gate driving
Proposed task/power management
Holistic project
State-of-the-art
Survival zone
Majority of reported work on power conditioning for energy harvesting
Battery manage-ment

Energy harvesting system

- Power adaptive system



Energy harvesting system

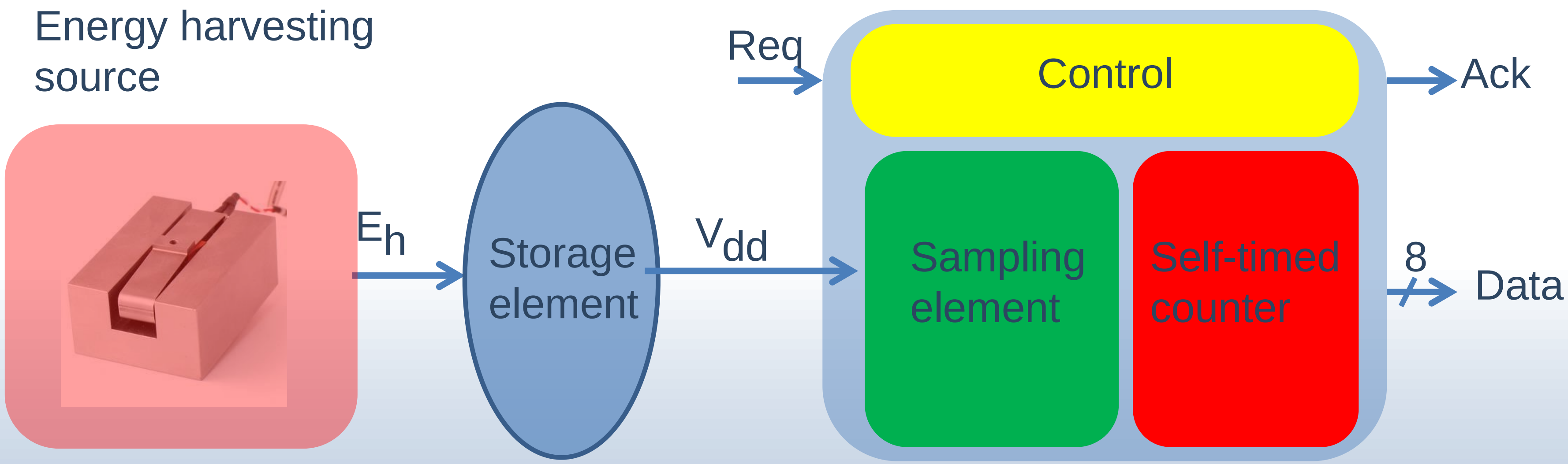
- Adaptation level
  - Cell level: e.g. single-rail vs dual-rail gates
  - Circuit level: e.g. clock/power gating, DVS and DFS (synchronous design)
  - System level
    - Control of computation load to fit the power profile
      - Computationally feasible mathematical models are now available that capture energy storage discharge characteristics in sufficient detail to let designers develop an optimization strategy [1].

1. R. Rao, S. Vrudhula, and D. N. Rakhmatov, "Battery modeling for energy aware system design," *Computer, vol. 36, pp. 77-87, 2003.*

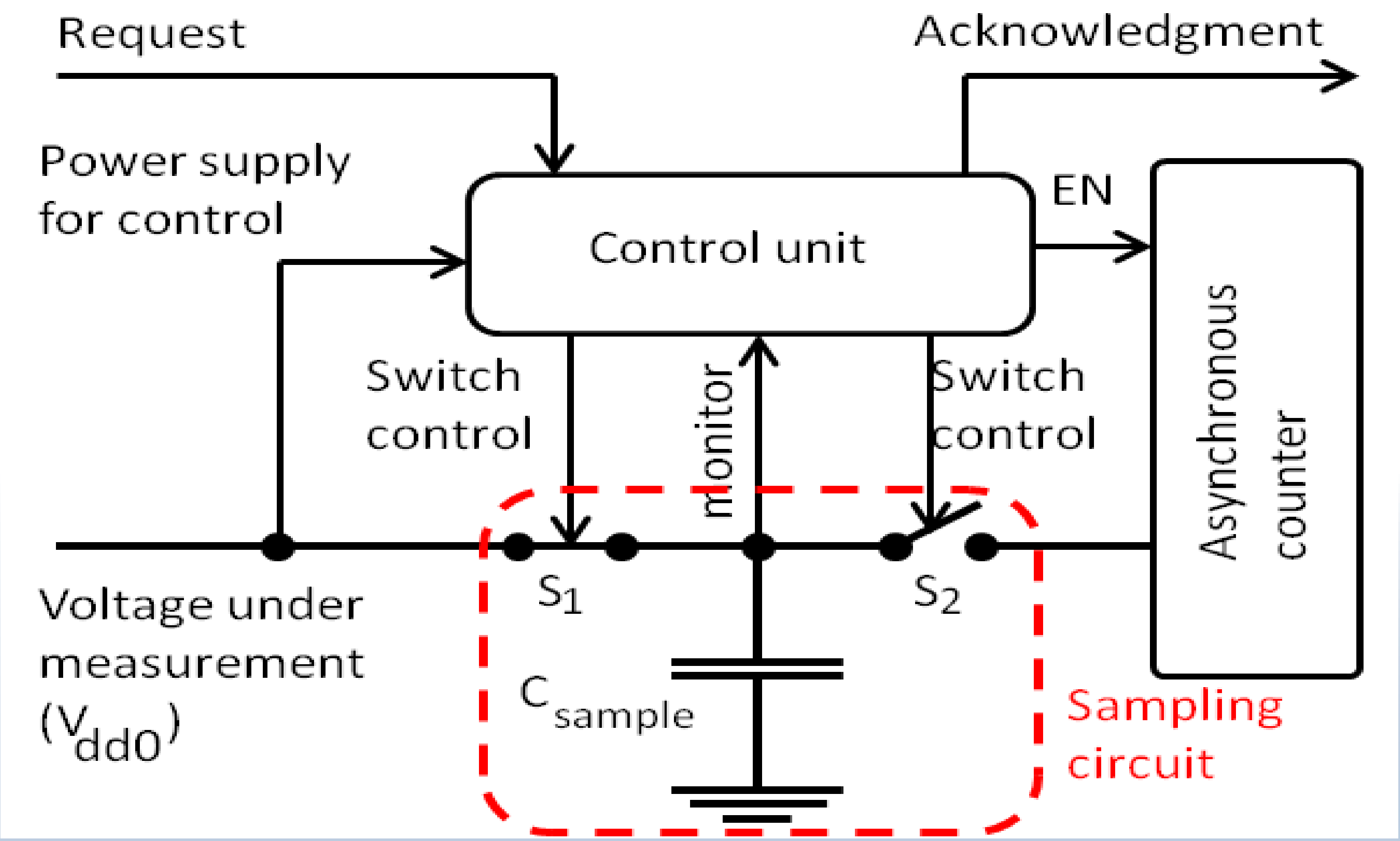
Energy harvesting system design

- Aims and objectives
  1. **well-characterised computational circuit blocks**, in terms of energy per action.
  2. refined **methods for the online measurement and sensing of voltage/power/energy** paths.
  3. high resolution **methods for controlling power** (e.g. power gating, dynamic voltage scaling) and **switching activity** (dynamic frequency scaling, clock gating, concurrency control, task scheduling).
  4. flexible (in terms of different levels of abstraction, granularity and accuracy) **methods of modelling power management and multi-parametric** (power, energy per operation, latency, throughput) analysis of modes of energising (rationing of power and Vdd levels) the computational load.

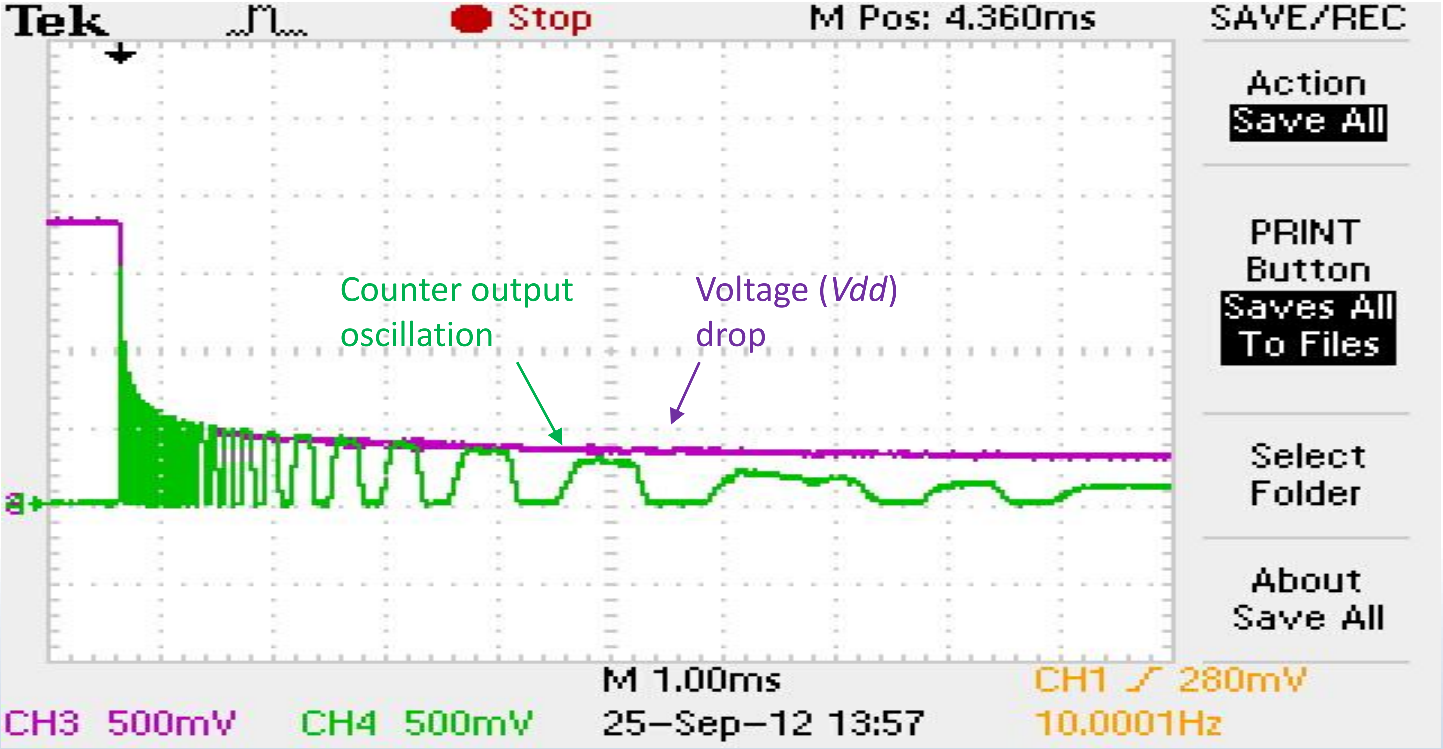
Example: voltage sensor without a reference



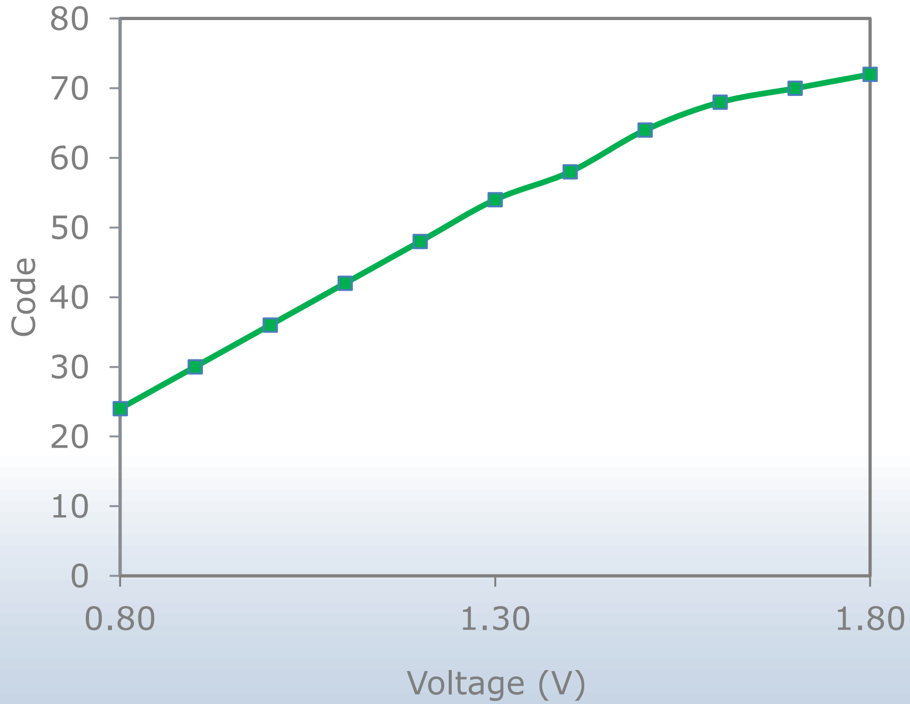
Voltage Sensor



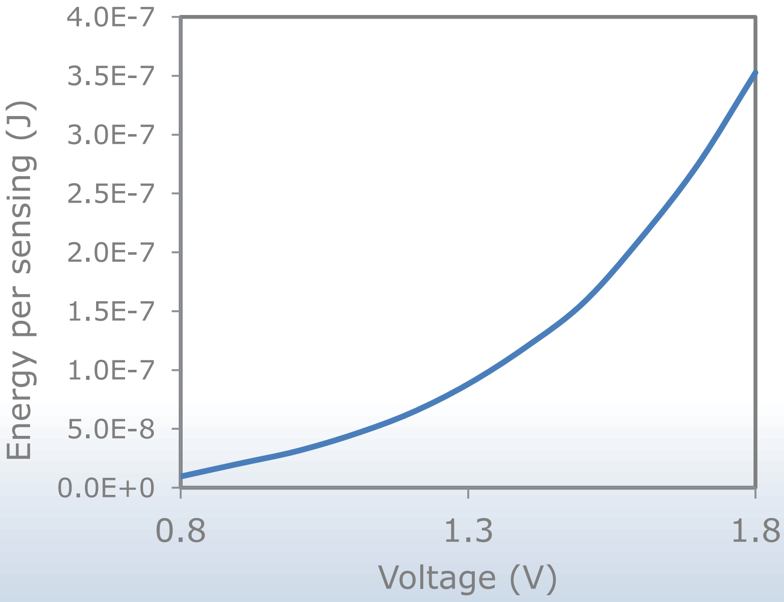
Capacitor discharging



Output count and energy consumption



C_{sample}=10nF



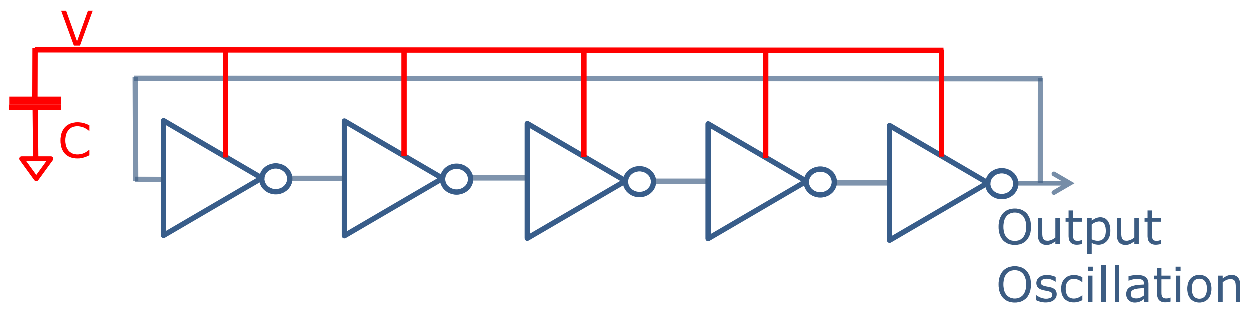
Capacitor Discharging Through Asynchronous Circuit Switching

- This work examines the relationship between the switching behaviour of a self-timed digital circuit and the dynamic characteristic of the voltage on the capacitor while the circuit is powered by the capacitor.

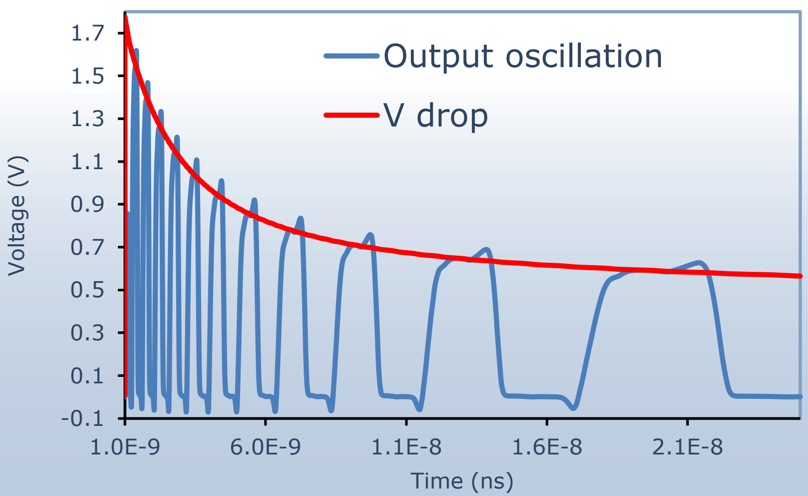
  - For this purpose, a sample system is considered that consists of an initially charged capacitor which is discharged through the switching of a ring oscillator.

  - Closed-form expressions are obtained for the supply voltage of the ring oscillator over time as it operates.

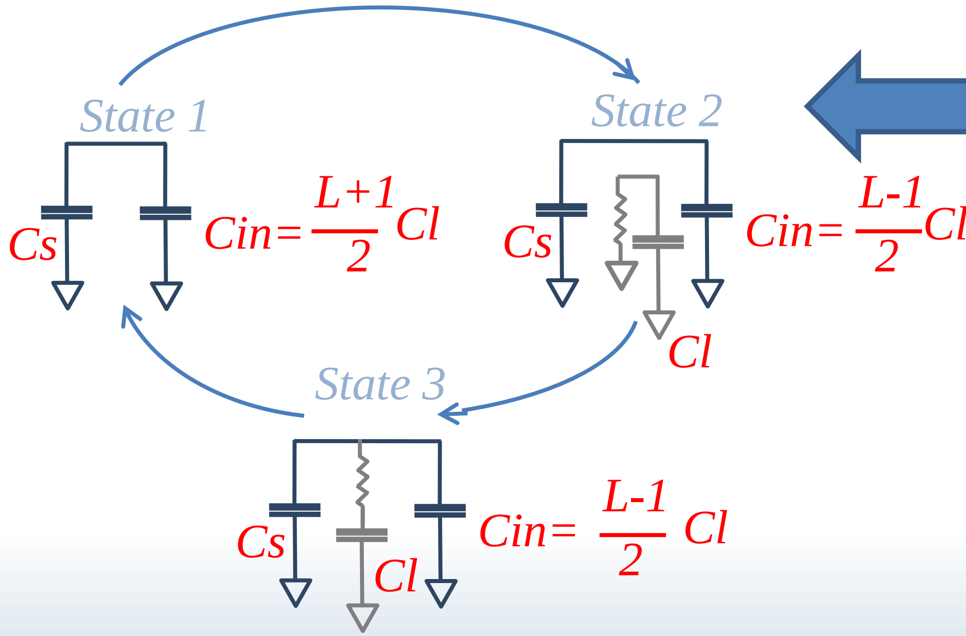
Dynamic Switching

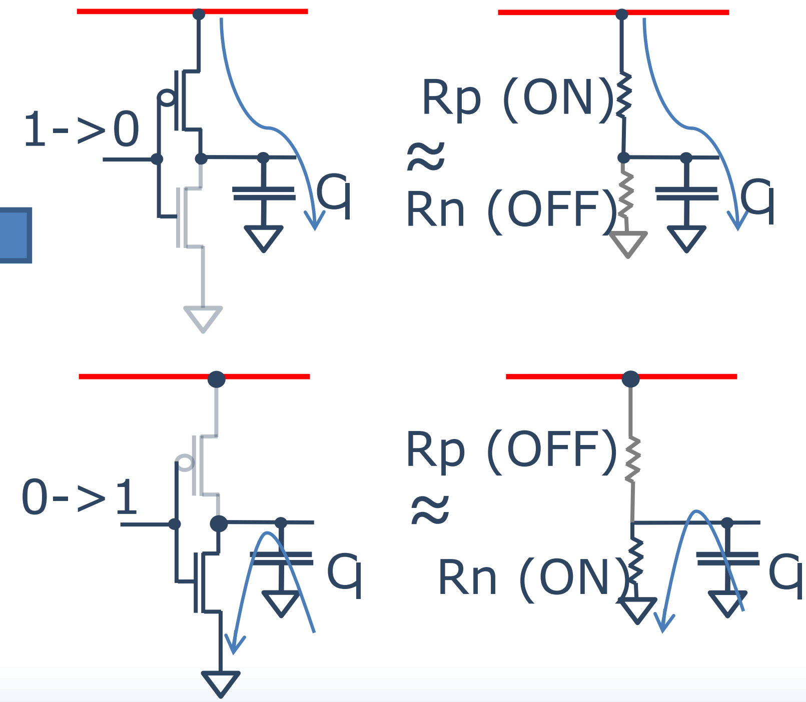


- We employ a simple ring-oscillator to serve as a self-timed digital circuit load.
- It is due to the fact that ring-oscillator can closely mimic the switching behaviour of many closed loop delay-insensitive asynchronous circuits.



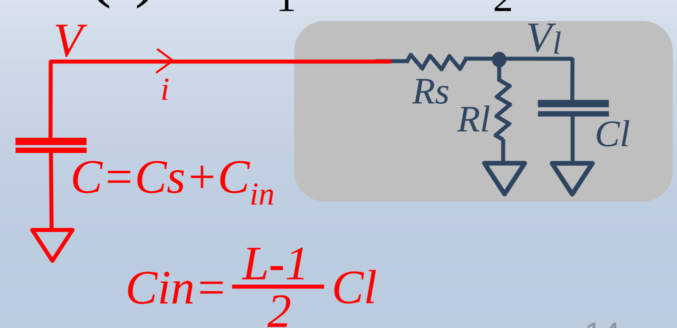
Circuit Model



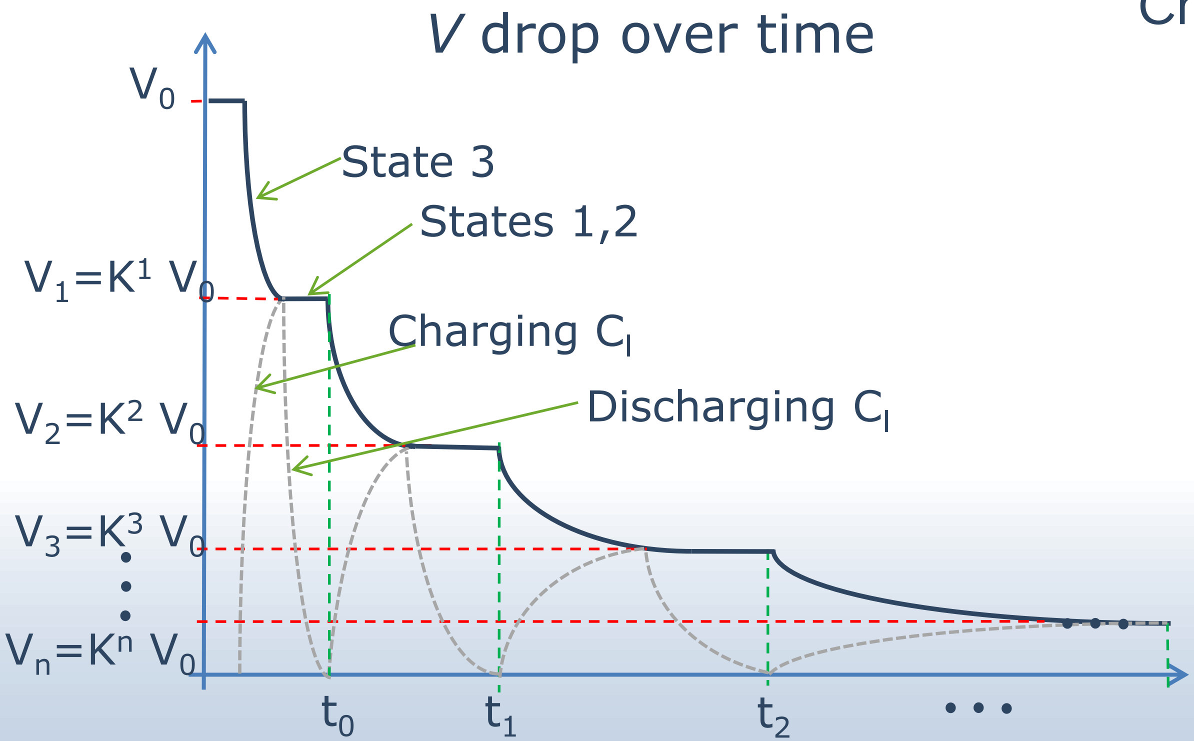


State 1: No switching
State 2: Discharging parasitic capacitor
State 3: Charging parasitic capacitor (consuming energy from the main Cap)

$$V(t) = K_1 e^{s_1 t} + K_2 e^{s_2 t}$$



Circuit Model: switching process



Charge equilibrium at:

$$V_1 = V_0 \frac{C}{C + C_l}$$

$$K = \frac{C}{C + C_l}$$

$$V = K^n V_0$$

$$V_N = K^n$$

Solution for Super-threshold

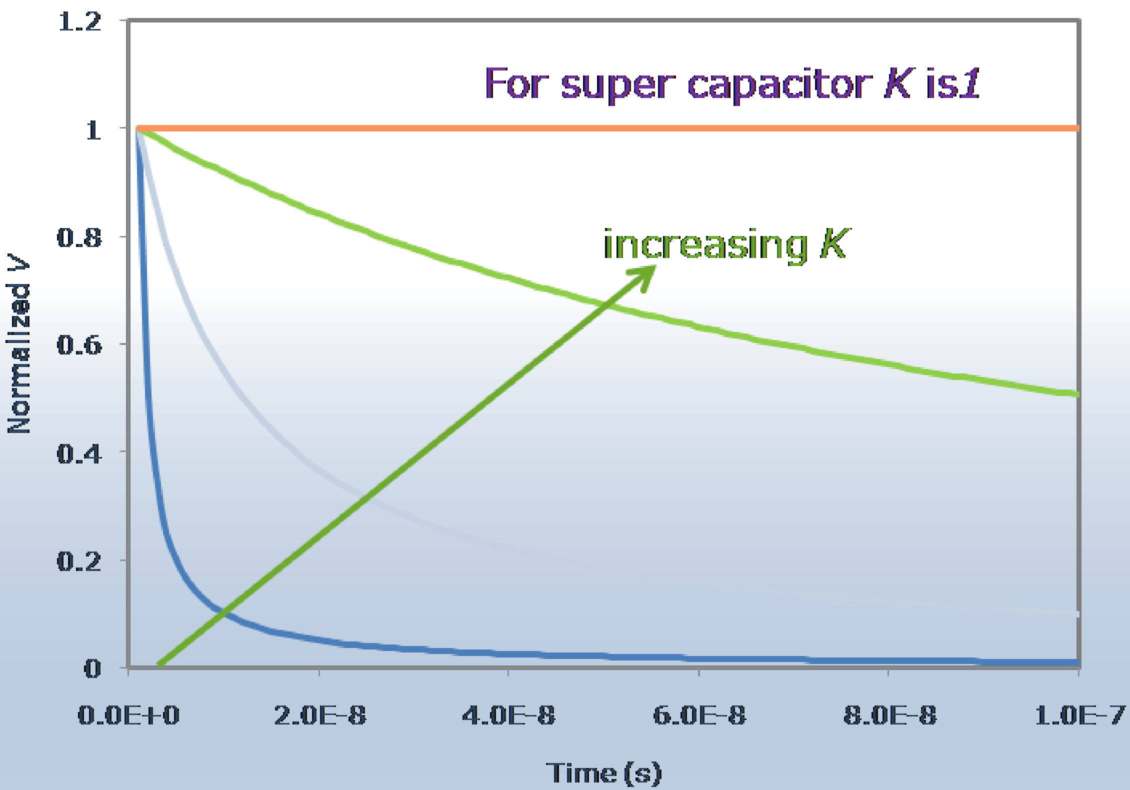
A valid assumption: in super-threshold region we can assume that the propagation delay is inversely proportional to the voltage, so we have:

Switching index	V_N	$t_s = \frac{A}{V}$	Physical time (t)
0	K^0	$\frac{A}{K^0}$	$\frac{A}{K^0}$
1	K^1	$\frac{A}{K^1}$	$\frac{A}{K^0} + \frac{A}{K^1}$
2	K^2	$\frac{A}{K^2}$	$\frac{A}{K^0} + \frac{A}{K^1} + \frac{A}{K^2}$
...			
n	K^n	$\frac{A}{K^n}$	$\sum_{i=0}^{n} \frac{A}{K^i}$

Solution for Super-threshold

$$V_N = \frac{A}{t(1-K)+AK}$$

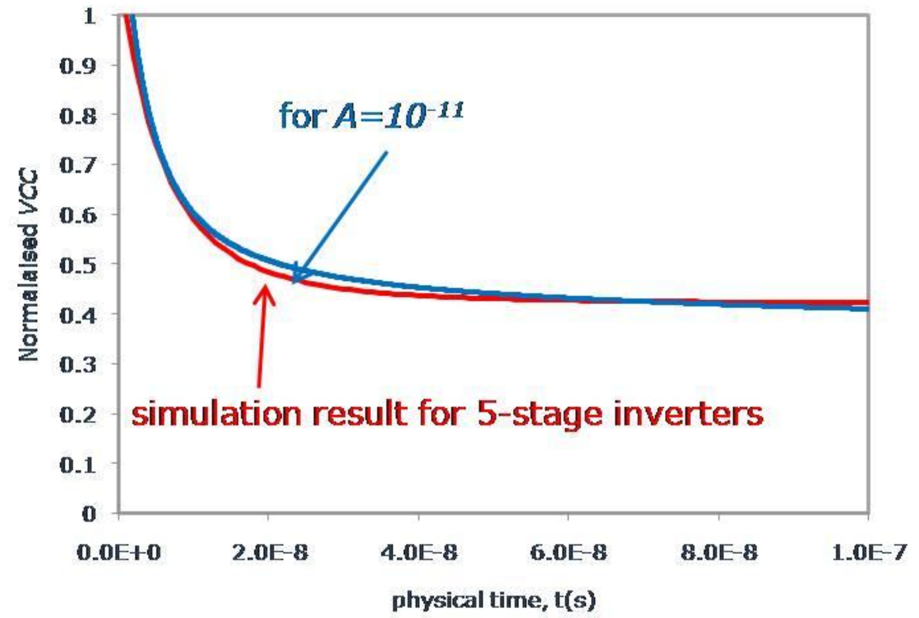
Hyperbolic function of time



More accurate solution for Super-threshold

A general model of gate delay propagation [1] is used:

$$t_p = \begin{cases} t_{p1} = \dfrac{pc_l V}{(V - V_{TH})^{\alpha}} \\ t_{p2} = \dfrac{pc_l V}{I_0 e^{\frac{V - V_{TH}}{N_s}}} \end{cases}$$



Assuming $\alpha = 1.3$

$$\int_0^n \frac{AK^i}{(K^i - V_{THN})^{\alpha}} di = V_{THN} + \left(\frac{-\frac{10}{3}A}{\ln K \cdot (t - B \cdot A)}\right)^{3.33}, B = \frac{\frac{10}{3}}{\ln K \cdot (1 - V_{THN})^{0.3}}$$

[1] “Sub-threshold Design for Ultra Low Power Systems”, Alice Wang, Benton H. Calhoun, Anantha P. Chandrakasan

Solution for Sub-threshold

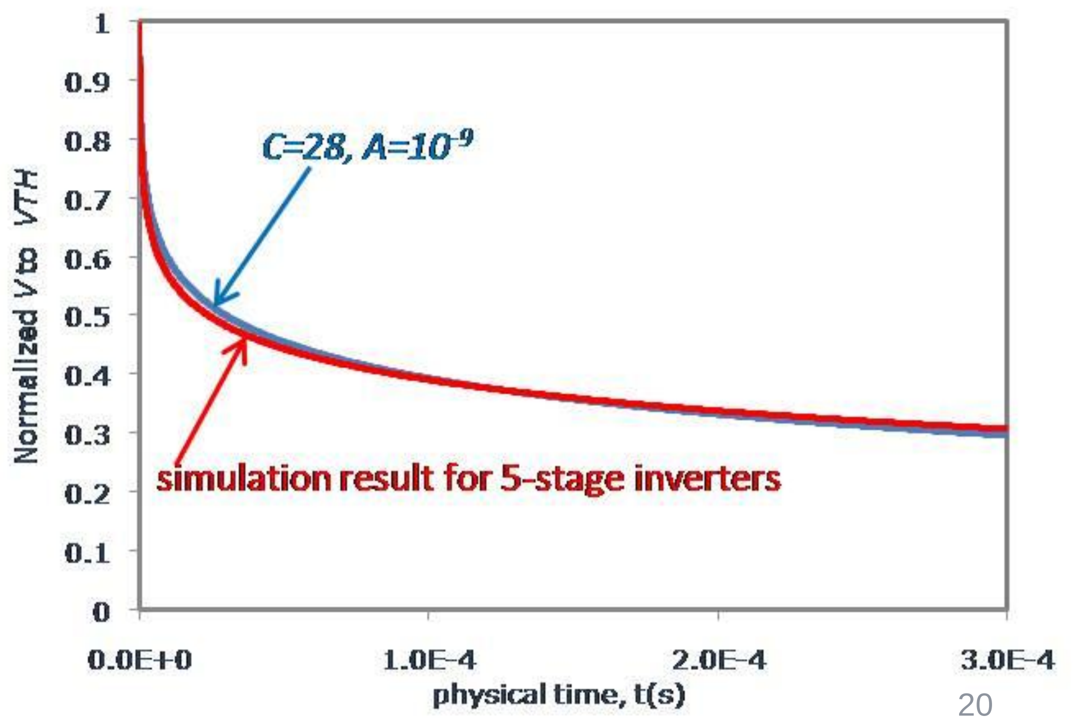
Switching index	V_N	t_s	Physical time (*t*)
0	K^0	A	A
1	K^1	$AKe^{c(1-K)}$	$A + AKe^{c(1-K)}$
2	K^2	$AK^2e^{c(1-K^2)}$	$A + AKe^{c(1-K)} + AK^2e^{c(1-K^2)}$
…			
n	K^n	$AK^ne^{c(1-K^n)}$	$A\sum_{i=0}^{n} K^i e^{c(1-K^i)}$

Solution for Sub-threshold

$$t = A\int_0^n K^i e^{C(1-K^i)}di = -A\frac{e^{C(1-K^i)}}{C\cdot\ln K}\Bigg|_{i=0}^{i=n}$$

In both regions the capacitor voltage drop follows a hyperbola function

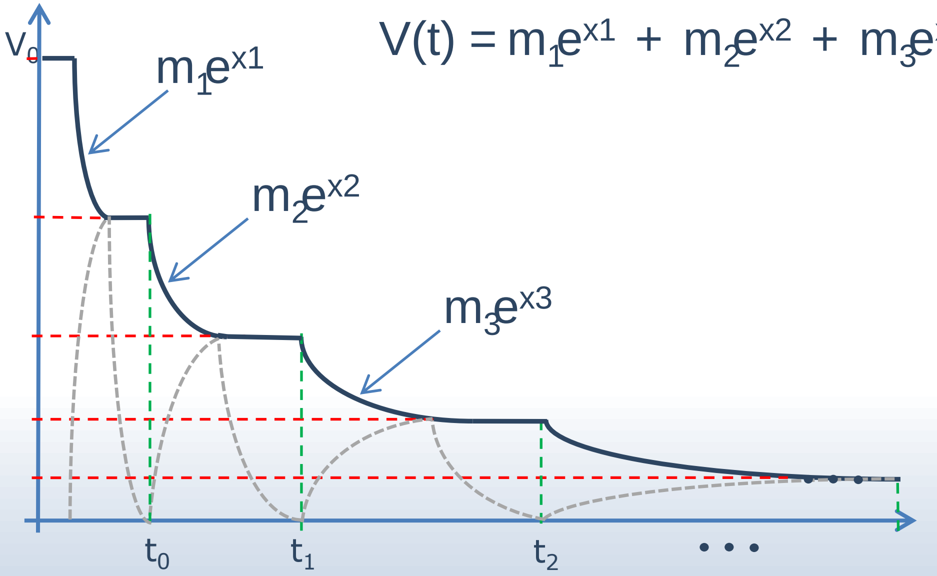
$$V_N = 1 - \frac{\ln(1-\frac{Ct\ln K}{A})}{C}$$



Discussion

In a **more complex circuit** we have:

$$V(t) = m_1e^{x1} + m_2e^{x2} + m_3e^{x3} + \cdots\cdots$$



- In a complex circuit, the switching activity is not as uniform as a ring oscillator.
- However, the overall switching activity within a single charging period can still be simplified as a single exponent term.
- The expansion of these will generate a complex form of the hyperbola function.

Discussion (hypotheses!)

- The energy profile of a circuit is best predictable if the capacitor discharging characteristic of the circuit switching maintains the ideal hyperbola function.
- New system or circuit design objective:
  - A design methodology should provide the switching activity profile which guarantees such an ideal hyperbola function. In such a design, energetic effort across the system would need to be uniform.
    - Overall energy consumption of the circuit at the single switching time over the period of an operation is simple the energy effort.
  - Uniform energy effort makes the circuit energy profile predictable!

Conclusion

- We explored the relationship between a capacitor based power source and a switching circuit, i.e. the capacitor state as a function of time.
- The analysis was fulfilled over the two regions of operation, super and sub-threshold for simple ring oscillator. Leakage, short circuit effects were ignored here.
- It shows a hyperbolic character of the discharge process, determined by the intrinsic properties of the circuit captured by coefficients A and K
- This could be used as an approximation to characterise *energy profile of digital (async) loads i*n energy harvesting systems

Future work

- Investigate the relationship between the hyperbolic discharge process and more general fractal dynamics calculus
- Investigate the idea of “energetic effort” and possibilities of optimising asynchronous circuits on the basis of uniformity in space and time (balanced effort)
- See potential for developing adaptive control laws for charging and discharging processes in energy harvesting systems and not only but in all energy and power constrained systems


THANK
YOU!