INTERNATIONAL JOURNAL OF CIRCUIT THEORY AND APPLICATIONS
Int. J. Circ. Theor. Appl. 2016; **44**:1127–1141
Published online 30 September 2015 in Wiley Online Library (wileyonlinelibrary.com). DOI: 10.1002/cta.2153

Fast-scale stability limits of a two-stage boost power converter

Abdelali El Aroudi[1,*,†], Kuntal Mandal[2,4], Damian Giaouris[3], Soumitro Banerjee[2], Abdullah Abusorrah[4], Mohammed Al Hindawi[4] and Yusuf Al-Turki[4]

[1]*GAEI Research Group, Departament d'Enginyeria Electrònica, Elèctrica i Automàtica, Universitat Rovira i Virgili, Tarragona, Spain*
[2]*Indian Institute of Science Education & Research – Kolkata, Mohanpur Campus, Nadia, WB, India*
[3]*Chemical Process Engineering Research Institute, Centre for Research and Technology Hellas, Thermi-Thessaloniki, Greece*
[4]*Department of Electrical and Computer Engineering, College of Engineering and Renewable Energy Research Group, King Abdulaziz University, Jeddah, Saudi Arabia*

SUMMARY

There are many applications in power electronics that demand high step-up conversion ratio between the source and the load. A simple way of achieving such a high voltage ratio is by cascading DC–DC boost converters in a few stages. The individual converters in such a cascaded system are usually designed separately applying classical design criteria. This paper investigates the stability of the overall system of a cascade connection of two boost converters under current mode control. We first demonstrate the bifurcation behavior of the system, and it is shown that the desired periodic orbit can undergo fast-scale period doubling bifurcation leading to subharmonic oscillations and chaotic regimes under parameter variation. The value of the intermediate capacitor is taken as a design parameter, and we determine the minimum ramp slope in the first stage required to maintain stability. It is shown that smaller capacitance values give rise to wider stability range. We explain the bifurcation phenomena using a full-order model. Then, in order to simplify the analysis and to obtain a closed-form expression to explain the previous observation, we develop a reduced-order model by treating the second stage as a current sink. This allows us to obtain design-oriented stability boundaries in the parameter space by taking into account slope interactions between the state variables in the two stages. Copyright © 2015 John Wiley & Sons, Ltd.

Received 7 March 2015; Revised 24 June 2015; Accepted 25 August 2015

KEY WORDS: DC–DC power conversion; high step-up conversion ratio; cascaded converters; stability analysis

1. INTRODUCTION

Power electronic systems are used in many applications where there is a need to convert one form of electrical energy into another. Examples include power supplies in consumer electronics, industrial electric motor drives, electro-heating, lighting, and energy-efficient interfaces between renewable energy resources and the distribution grid. One of the most used topologies in energy conversion is the boost converter, which steps up a source voltage to a higher voltage level [1].

In some applications, the required step-up conversion ratio is quite high. Such necessities arise in uninterrupted power supplies, automobile high-intensity discharge headlamps, in several medical equipments, among others. This is also the case of renewable energy applications such as distributed photovoltaic generation systems [2,3], fuel cell energy conversion systems, and modern electric vehicles.

*Correspondence to: Abdelali El Aroudi, GAEI Research Group, Departament d'Enginyeria Electrònica, Elèctrica i Automàtica, Universitat Rovira i Virgili, Tarragona, Spain.
†E-mail: abdelali.elaroudi@urv.cat

In these high-step-up-ratio applications, although a single boost converter can be used, there are many inconveniences with its use mainly related to increased stress on the components and the poor system efficiency due to the large conduction losses. Moreover, a high step-up conversion ratio requires a large duty cycle, which makes the system prone to subharmonic instability and consequently large current ripples. As a remedy, the conventional boost converter may be substituted by a number of boost converters connected in cascade, where each could operate with relatively low values of duty ratio [4–7].

The design of such integrated systems would require a comprehensive knowledge about suitable ways of modeling such systems, analysis of stability, the instabilities that can occur, and finally some design guidelines. This paper takes the first step in achieving these objectives.

The desired behavior of any power electronic system is a periodic orbit with the same period as the external clock signal. This orbit is often called period-1 orbit. However, because of the presence of switching nonlinearities, it is possible that the system behaves with a period-k orbit, $k=2,\ 3,\ 4\ldots$, with a period equal to an integer multiple of the external clock period. The system can even enter quasi-periodic or chaotic regimes through different bifurcation scenarios. During the last couple of decades, much effort has been devoted to the study of complex nonlinear phenomena in switching converters [8–10]. These phenomena can have harmful effects on the system operation and may cause system failure, malfunctioning due to large ripple, and poor efficiency or even damages caused by the increase of the stress on the switching components. Therefore, their study and prediction are important both from theoretical and practical points of view.

The study of these nonlinear phenomena is mostly based on accurate modeling approaches coping with switching action such as discrete-time mappings [11] or the Floquet theory combined with Filippov's method [12,13] to obtain the Jacobian of the Poincaré map or the monodromy matrix. In this paper, we investigate the dynamics and stability issues in a system comprising two cascaded boost converters connected to a constant voltage source, which can model a DC bus or a backup battery. Both the converters are controlled by current-mode controllers.

The rest of this work is organized as follows. Section 2 deals with the description of the system under study. In Section 3, some instability problems taking place in the system are shown and then explained in Section 4 in terms of Floquet multipliers corresponding to period-1 orbits. Design-oriented modeling of the system is addressed in Section 4. From a reduced-order model, simplified stability boundaries in parameter space are obtained in Section 5. Design-oriented stability conditions are obtained in the same section. Finally, some conclusions are drawn in the last section.

2. CURRENT MODE-CONTROLLED CASCADED BOOST–BOOST CONVERTERS

2.1. System description

The two-stage DC–DC converter considered in this study is shown in Figure 1. It consists of a cascade connection of two boost converters. The switches are considered ideal, and the equivalent series resistances of inductors and capacitors are included in the model of the circuit. The aim of the controllers is as follows: First, the intermediate voltage must be regulated to a desired reference voltage V_{ref1}. Because boost converters are non-minimum phase systems, if the feedback variable is the output voltage [1], a current mode control is mandatory. In this case, the external voltage regulator provides the reference for the inner current controller, which is a simple (but adequate for this task) peak current controller. The second stage is controlled with the aim to provide the proper current to the load, and therefore, a tight average current controller is used.

More, specifically, the system is controlled by comparing the inductor currents of the first and the second stages i_{L1} and i_{L2} with their reference values i_{ref1} and i_{ref2}. The intermediate voltage v_{o1} is controlled to a desired value by using a peak Current Mode Control (CMC) in the first stage with a closed intermediate voltage loop and an artificial periodic ramp compensator $i_{a1}(t)$ with slope m_{a1}. The second stage must provide a regulated average current to the output, which could be a DC bus or a battery.

DOI: 10.1002/cta

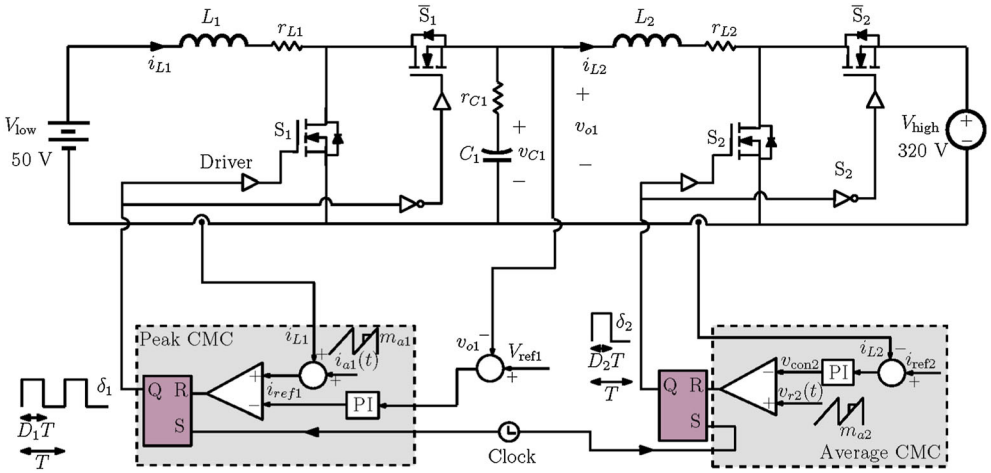


Figure 1. Schematic circuit diagram of a boost switching converter loaded by another boost switching converter. The first stage is under a peak CMC with its output voltage loop closed. The average input current in the second stage is tightly regulated by a PI compensator.

2.2. Power stage modeling

By applying Kirchhoff's current and voltage laws to the circuit depicted in Figure 1, the following set of differential equations are obtained:

$$\frac{\mathrm{d}i_{L1}}{\mathrm{d}t} = \frac{V_{\mathrm{low}}}{L_1} - \frac{r_{L1}i_{L1}}{L_1} - \frac{v_{C1} + r_{C1}(i_{L1} - i_{L2})}{L_1}(1 - \delta_1) \tag{1}$$

$$\frac{\mathrm{d}i_{L2}}{\mathrm{d}t} = \frac{v_{C1} + r_{C1}(i_{L1}(1 - \delta_1) - i_{L2})}{L_2} - \frac{r_{L2}i_{L2}}{L_2} - \frac{V_{\mathrm{high}}}{L_2}(1 - \delta_2) \tag{2}$$

$$\frac{\mathrm{d}v_{C1}}{\mathrm{d}t} = \frac{i_{L1}}{C_1}(1 - \delta_1) - \frac{i_{L2}}{C_1} \tag{3}$$

where for the first stage (resp. second stage), $\delta_1 = 1$ (resp. $\delta_2 = 1$) when the switch S_1 (resp. S_2) is closed and $\delta_1 = 0$ (resp. $\delta_2 = 0$) when the switch S_1 (resp. S_2) is open. The switches $\overline{S}_1$ and $\overline{S}_2$ are driven complementarily to S_1 and S_2, respectively. The variables δ_1 and δ_2 are the binary command signals used to drive the switches S_1 and S_2, respectively.

2.3. Controllers modeling

With the aim to regulate the intermediate voltage to its desired value, the inductor current reference in the first stage is generated from an outer voltage loop PI controller whose input is the intermediate voltage error $e_{v1} = V_{\mathrm{ref1}} - v_{o1}$, $v_{o1} = v_{C1} + r_{C1}C_1\mathrm{d}v_{C1}/\mathrm{d}t$, and whose output is i_{ref1} given by

$$i_{\mathrm{ref1}} = W_v(e_{v1} + \omega_{zv}x_4) \tag{4}$$

where $x_4 = \int e_{v1}(t)\mathrm{d}t$ is the integral of intermediate voltage error. To regulate the inductor current i_{L2} in the second stage to its desired value, the error $i_{\mathrm{ref2}} - i_{L2}$ is processed by a PI compensator whose output is given by

$$v_{\mathrm{con2}} = W_i(e_{i2} + \omega_{zi}x_5) \tag{5}$$

where $x_5 = \int e_{i2}(t)\mathrm{d}t$ is the integral of the current error.

DOI: 10.1002/cta

So, the extra state equations for these two integral state variables are

$$\frac{\mathrm{d}x_4}{\mathrm{d}t} = V_{\mathrm{ref1}} - v_{C1} - r_{C1}(i_{L1}(1-\delta_1) - i_{L2}) \tag{6}$$

$$\frac{\mathrm{d}x_5}{\mathrm{d}t} = i_{\mathrm{ref2}} - i_{L2} \tag{7}$$

2.4. Operating modes and piecewise linear state equations

Different types of period-1 cycles are possible for the system depending on the parameters of the first and the second stages. These different period-1 orbits define different operating modes for the system depending on the relationship between the duty cycles of the driving signals. It can be shown that there are basically three operating modes that can be summarized as follows (Figure 2).

Within a clock period T, four different configurations C_1, C_2, C_3, and C_4 are possible corresponding to the pair states (ON, ON), (OFF, ON), (OFF, OFF), or (ON, OFF) of the switches S_1 and S_2, respectively. However, during a switching period, the system can switch among only three of them as either the configuration C_2:=(OFF, ON) or C_4:=(ON, OFF) is skipped depending on whether $D_1 < D_2$ or $D_2 < D_1$, where D_1 and D_2 are the duty cycles of the first stage and the second stage, respectively.

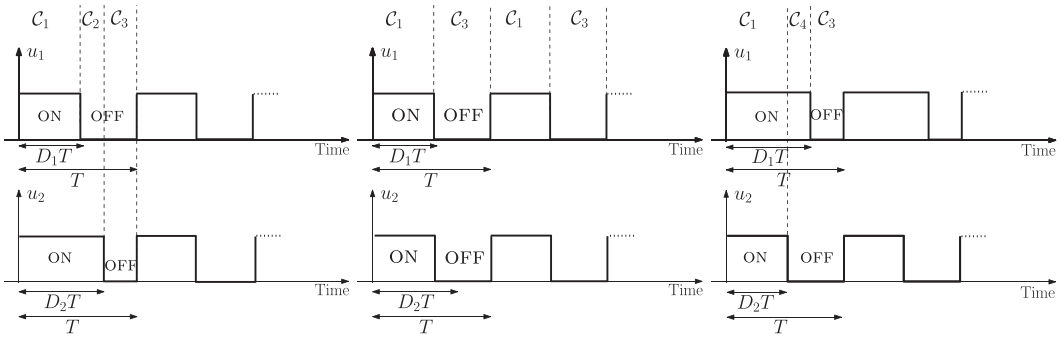
For each state of the switch pair (S_1, S_2), the system can be described by a set of linear differential equations that can be written as follows:

$$\dot{\mathbf{x}} = \mathbf{A}_{ij}\mathbf{x} + \mathbf{B}_{ij},\ (i,j) \in \{0,1\}^2$$

The vector of the state variables of the system is $\mathbf{x} = (i_{L1}, i_{L2}, v_{C1}, x_4, x_5)^\top \in \mathbb{R}^5$. Obtaining $\mathbf{A}_{ij}$ and $\mathbf{B}_{ij}$ from (1)–(3) and (6), (7) is straightforward. The matrices and vectors corresponding to each configuration are given in the following.

- Configuration C_1 corresponding to the switch state pair (ON, ON)

$$\mathbf{A}_{11} = \begin{pmatrix} -\frac{r_{L1}}{L_1} & 0 & 0 & 0 & 0 \\ 0 & -\frac{r_{L2}+r_{C1}}{L_2} & \frac{1}{L_2} & 0 & 0 \\ 0 & -\frac{1}{C_1} & 0 & 0 & 0 \\ 0 & r_{C1} & -1 & 0 & 0 \\ 0 & -1 & 0 & 0 & 0 \end{pmatrix}, \mathbf{B}_{11} = \begin{pmatrix} \frac{V_{\mathrm{low}}}{L_1} \\ 0 \\ 0 \\ V_{\mathrm{ref1}} \\ i_{\mathrm{ref2}} \end{pmatrix} \tag{8}$$



(a) Mode 1: $D_1 < D_2$ (b) Mode 0: $D_1 = D_2$ (c) Mode 2: $D_1 > D_2$

Figure 2. Possible operating modes for the system.

DOI: 10.1002/cta

- Configuration C_4 corresponding to the switch pair state (ON, OFF)

$$\mathbf{A}_{10} = \mathbf{A}_{11}, \mathbf{B}_{10} = \left(\frac{V_{\text{low}}}{L_1}, \quad -\frac{V_{\text{high}}}{L_2}, \quad 0, \quad V_{\text{ref1}}, \quad i_{\text{ref2}} \right)^{\top} \tag{9}$$

- Configuration C_3 corresponding to the switch pair state (OFF, OFF)

$$\mathbf{A}_{00} = \begin{pmatrix} -\dfrac{r_{L1}+r_{C1}}{L_1} & -\dfrac{r_{C1}}{L_1} & -\dfrac{1}{L_1} & 0 & 0 \\ -\dfrac{r_{C1}}{L_2} & -\dfrac{r_{C1}+r_{L2}+r_{C1}}{L_2} & \dfrac{1}{L_2} & 0 & 0 \\ \dfrac{1}{C_1} & -\dfrac{1}{C_1} & 0 & 0 & 0 \\ -r_{C1} & r_{C1} & -1 & 0 & 0 \\ 0 & -1 & 0 & 0 & 0 \end{pmatrix}, \tag{10}$$

$$\mathbf{B}_{00} = \mathbf{B}_{01}$$

- Configuration C_2 corresponding to the switch pair state (OFF, ON)

$$\mathbf{A}_{01} = \mathbf{A}_{00}, \mathbf{B}_{01} = \mathbf{B}_{11} \tag{11}$$

It is worth noting also that the system is linear for each switch pair state, and the nonlinearities arise in this kind of systems basically from interaction between feedback and switching processes that make the dynamics of the system highly nonlinear.

At the beginning of each switching cycle in the first stage, the switch S_1 is turned ON. The controlled current i_{L1} increases until it reaches the signal $i_{\text{ref1}} - m_{a1}(t \mod T)$; the switch S_1 is then turned OFF and remains OFF until the next cycle begins. The switch S_2 is switched ON at the beginning of each switching period and is switched OFF whenever v_{con2} crosses v_{r2}.

Therefore, the switch S_1 in the first stage is closed periodically at each clock period, and it is turned OFF whenever the following switching function

$$\sigma_1(\mathbf{x}, t) := i_{L1} - i_{r1} : \quad = \mathbf{F}_1 \mathbf{x}(t) - W_v V_{\text{ref1}} + m_{\text{a1}}(t \bmod T) \tag{12}$$

is equal to zero, where $i_{r1} = i_{\text{ref1}} - m_{a1}(t \mod T)$ and $\mathbf{F}_1 = (1, -W_v r_{C1}, W_v, -W_v \omega_{zv}, 0)$. In the second stage, the switching decision is taken by comparing the control signal $v_{\text{con2}}(t)$ with a periodic ramp modulator $v_{r2}(t)$. The switching instants are therefore solutions of the equation

$$\sigma_2(\mathbf{x}, t) := v_{\text{con2}}(t) - v_{r2}(t) := \mathbf{F}_2 \mathbf{x}(t) + W_i i_{\text{ref2}} - m_{a2}(t \bmod T) = 0, \tag{13}$$

where $\mathbf{F}_2 = (0, -W_i, 0, 0, W_i \omega_{zi})$. Note that $\mathbf{F}_1$ and $\mathbf{F}_2$ are also the normal vectors to the switching manifolds defined by (12) and (13), respectively.

3. SYSTEM BEHAVIOR FROM NUMERICAL SIMULATIONS

The fixed circuit parameter values used in this study are shown in Table I, and they are selected as practical values for connecting a photovoltaic panel or a storage battery with a low voltage $V_{\text{low}} = 50\,\text{V}$ interfaced through a two-stage boost converter with a DC bus whose voltage is $V_{\text{high}} = 320\,\text{V}$ [14]. The switching frequency for both the stages is $f_s = 100\,\text{kHz}$. The intermediate voltage v_{o1} is regulated to approximately 200 V in order to make the first stage to work with a duty

DOI: 10.1002/cta

Table I. The used parameter values.

L_1 r_{L1}	r_{C1}	V_{ref1}	W_v, ω_{zv}	L_2 r_{L2}	W_i	i_{ref2}	ω_{zi}
420 µH, 100 mΩ	50 mΩ	200 V	1, 1 krad/s	2 mH, 100 mΩ	1 Ω	1 A	10 krad/s

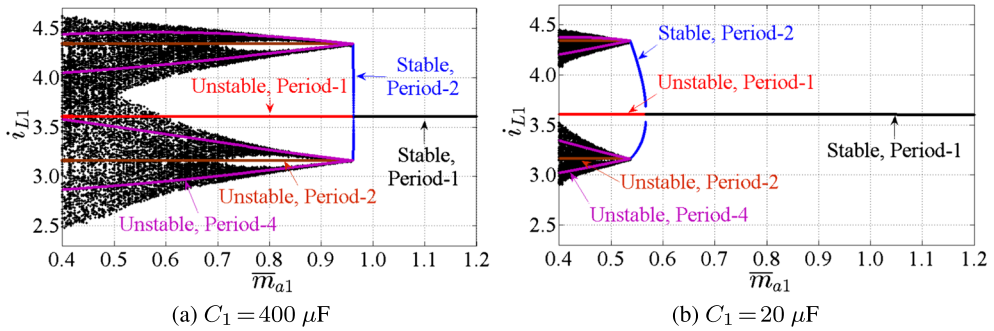
cycle $D_1 = 0.75\,\%$. With this value of the duty cycle ($D_1 > 0.5\,\%$), a ramp compensator is necessary in this stage to avoid subharmonic oscillation according to [1]. The duty cycle in the second stage is $D_2 = 0.375$, and according to the classical design criterion in [1], no ramp compensation is needed. In the classical design, the minimum ramp needed to avoid subharmonic oscillations in a boost converter with duty cycle D, inductance L, and output voltage v_o is given by the expression [1]

$$\underbrace{\frac{v_o}{L}\left(D-\frac{1}{2}\right)}_{m_{a,\text{cri}}(D)} < m_a \tag{14}$$

where m_a is the slope of the T-periodic artificial ramp compensator, D is the duty cycle, v_o is the output voltage, and L is the inductance value. In our example, we have for the first stage $m_{a,\text{cri},1}(D_1) = v_{o1}(D_1 - 1/2)/L_1$, where $D_1 = 0.75$, that is, $m_{a,\text{cri},1} \approx 119$ kA/s. Because the switching frequency is $f_s = 100$ kHz, the minimum ramp amplitude must be $I_{M1} = 1.19$ A. Therefore, with a ramp amplitude less than 1.19 A, the system should be unstable according to (14). However, we will see that this is not always the case, and in particular, we will show that the stability boundary also depends on other parameters not appearing in (14). For the second stage, the duty cycle is $D_2 = 0.375 < 0.5$, and a priori, the system can be stable even without a ramp compensator. In our study, a constant ramp slope $m_a = m_2 = (V_{\text{high}} - v_{o1})/L_2$ is used guaranteeing a deadbeat response with a zero discrete time eigenvalue in the second stage according to the conventional approach [1]. Therefore, in our interconnected scheme, a ramp voltage whose amplitude is $V_{M2} = 0.6$ V has been used in the second stage to obtain this kind of response.

In order to investigate the possible nonlinear phenomena that the system can exhibit, a bifurcation diagram is computed by taking the normalized ramp slope $\overline{m}_{a1} = m_{a1}/(V_{\text{low}}/L_1)$ as a bifurcation parameter, which is varied between 0.4 and 1.2 for two different values of the output capacitances $C_1 = 20$ and 400 µF. The results are shown in Figure 3. It shows that as the ramp slope is reduced, at a specific parameter value, the converter loses stability and goes into a period-2 subharmonic oscillation, and as the slope is reduced further, there is a border-collision bifurcation leading to chaotic behavior. For example, Figure 4(a) shows the period-2 waveforms before and after the border collision at $C_1 = 20$ µF. At the border-collision bifurcation point, an infinite number of unstable orbits are created, two of which (period 2 and period 4) are shown in the figure. All the unstable orbits in Figure 3 are drawn using the method given in [12,15].

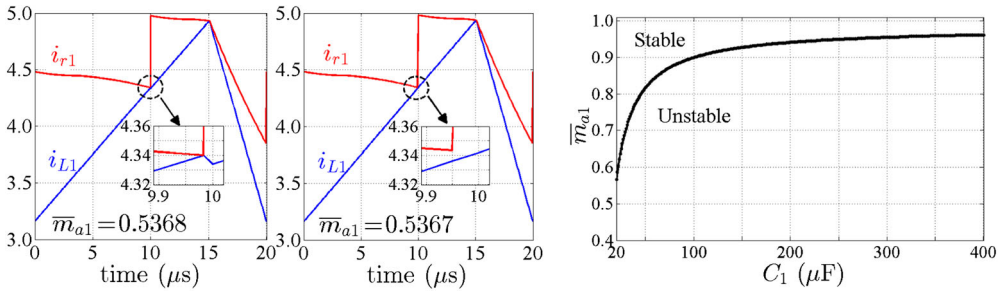
The most remarkable observation is that the slope required for stabilization for a capacitance $C_1 = 20$ µF is smaller than that required for 400 µF. In general, it can be claimed that within a



(a) $C_1 = 400$ µF (b) $C_1 = 20$ µF

Figure 3. Bifurcation diagram by taking $\overline{m}_{a1}$ as a bifurcation parameter for two different values of the intermediate capacitance C_1. The required ramp slope for $C_1 = 400$ µF is larger than the one for $C_1 = 20$ µF.

DOI: 10.1002/cta



(a) (b)

Figure 4. (a) Period-2 waveforms before (stable at $\overline{m}_{a1} = 0.5368$) and after (unstable at $\overline{m}_{a1} = 0.5367$) the border-collision bifurcation for $C_1 = 20\,\mu$F (Table III). (b) Boundary between stable and unstable regions in the parameter space $(C_1, \overline{m}_{a1})$.

certain practical range of capacitance values, the larger the capacitance C_1, the larger the ramp slope required for stabilization. This is confirmed in Figure 4(b) where the stability boundary is plotted in the parameter space $(C_1, \overline{m}_{a1})$. Two main remarks can be carried out from the results of this figure:

- The stability boundary shows a significant dependence on the capacitance values. Note that the design based on the conventional approach in (14) does not show any dependence of the stability limits on the capacitance C_1.
- Because higher capacitance values will imply lower ripples in the voltage, it is broadly believed by the power electronics community that the larger values of the capacitance makes the system more stable. Surprisingly, the system with a lower capacitance value has a wider stability region. Note however, that general constraints on the maximum allowed ripple must be met in such a way that the value of the intermediate capacitance must be selected according to a compromise between stability requirement and allowed ripple.

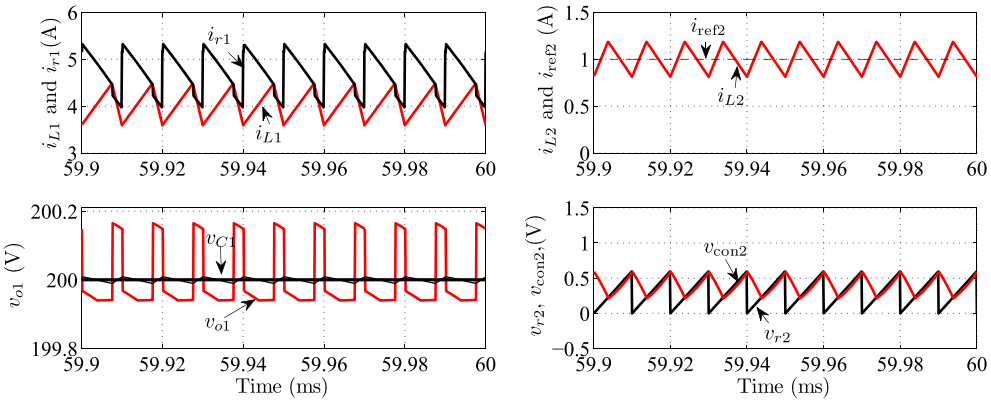
To check the results shown in Figure 4, we obtain a plot of the system waveforms for different values of capacitance C_1 and normalized ramp slope $\overline{m}_{a1}$. Figure 5 shows the steady-state response of the system for $C_1 = 400\,\mu$F with $\overline{m}_{a1} = 1.008$ and $\overline{m}_{a1} = 0.9584$. It can be observed that the steady-state cycle-by-cycle behavior of the first stage exhibits fast-scale subharmonic oscillation for $\overline{m}_{a1} = 0.9584$. Note that the second stage maintains negligibly small subharmonic oscillation because the slope of the ramp is selected to be equal to $m_2 = (V_{\text{high}} - v_{o1})/L_2$, guaranteeing deadbeat response. That is why subharmonic oscillation is not appreciable in the second stage.

Figure 6 shows the steady-state response of the system for $C_1 = 20\,\mu$F. From this figure, it can be observed that the system is stable even with much smaller ramp slope than in the previous case, which is in good agreement with the results in Figure 4. In particular, this parameter was decreased to $I_{M1} = 0.2\,$A for Figure 6(a). By numerical simulation, it was found that the new critical value of the ramp slope m_{a1} is close to 0.19 A and if the ramp slope m_{a1} is selected less than this value, the system will exhibit subharmonic oscillation (Figure 6(b)), and this is also in perfect agreement with the stability boundary shown in Figure 4. Notice that like before, the second stage is maintained stable, and subharmonic oscillation is exhibited only in the first stage.

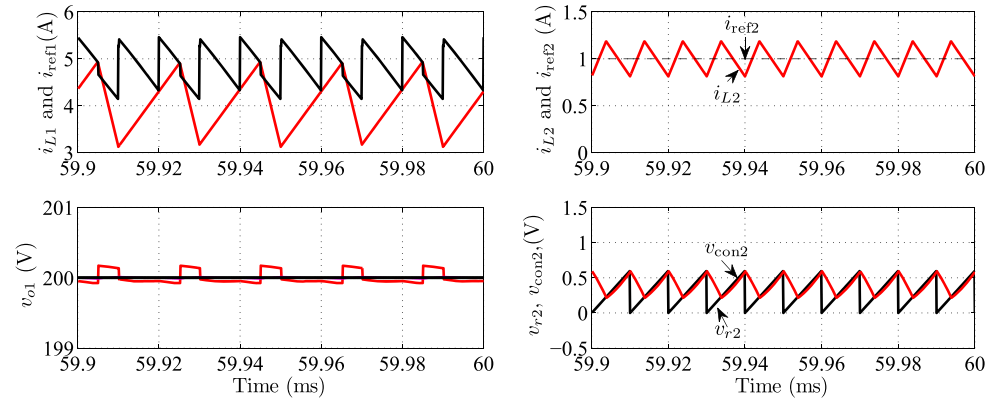
4. STABILITY ANALYSIS USING FLOQUET THEORY AND THE MONODROMY MATRIX

Nonlinear dynamical systems can present many types of steady-state behaviors such as period-k orbits ($k = 1, 2, \ldots$), quasi-periodic motions and chaotic regimes. The stability of periodic motions can be determined by the Floquet multipliers, which are the eigenvalues of the fundamental solution matrix or the monodromy matrix. This matrix is the Jacobian of the linearized system along the periodic orbit and can be obtained from the product of the state transition matrices corresponding to each subcycle and the corresponding saltation matrices [12,13]. Suppose a

DOI: 10.1002/cta



(a) $\overline{m}_{a1} = 1.008$.



(b) $\overline{m}_{a1} = 0.9584$.

Figure 5. Waveforms of the state variables and the control signals in the two stages for two different values of $\overline{m}_{a1}$ and for $C_1 = 400\,\mu\text{F}$.

trajectory starts at time instant t_i and as described by the vector field $\mathbf{f}_i(\mathbf{x})$ intersects the switching boundary described by the equation $\sigma_{i,i+1}(\mathbf{x}(t), t) = 0$ at t_i and switches to the vector field $\mathbf{f}_{i+1}(\mathbf{x})$. It has been shown, using the Filippov method [12,13], that when there is a transversal intersection, the state transition matrix across the switching boundary, also called the saltation matrix $\mathbf{S}_{i,i+1}$, is given by

$$\mathbf{S}_{i,i+1} = \mathbf{I} + \frac{(\mathbf{f}_{i+1}(\mathbf{x}(t_i)) - \mathbf{f}_i(\mathbf{x}(t_i)))\mathbf{K}_{i,i+1}}{\mathbf{K}_{i,i+1}\mathbf{f}_i(\mathbf{x}) + \frac{\partial \sigma_i}{\partial t}|_{t=t_i}} \tag{15}$$

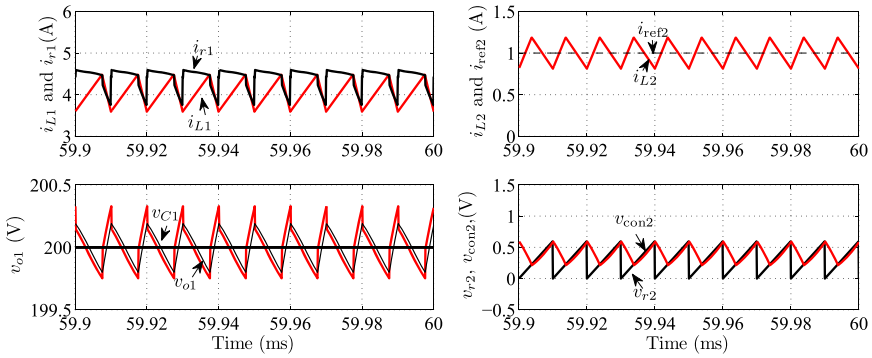
where $\mathbf{I}$ is an identity matrix with appropriate size and $\mathbf{K}_{i,i+1}$ is the gradient of the surface $\sum_{i,i+1} := \{(\mathbf{x}, t) = \sigma_{i,i+1}(\mathbf{x}(t), t) = 0\}$. Then, the monodromy matrix $\mathbf{M}$ for a switched system with N_c different configurations can be composed during a complete cycle as follows:

$$\mathbf{M}(\mathbf{x}(0)) = \mathbf{S}_{N_c,N_c-1}\Phi_{N_c}\mathbf{S}_{N_c-1,N_c}\ldots\Phi_2\mathbf{S}_{1,2}\Phi_1 \tag{16}$$

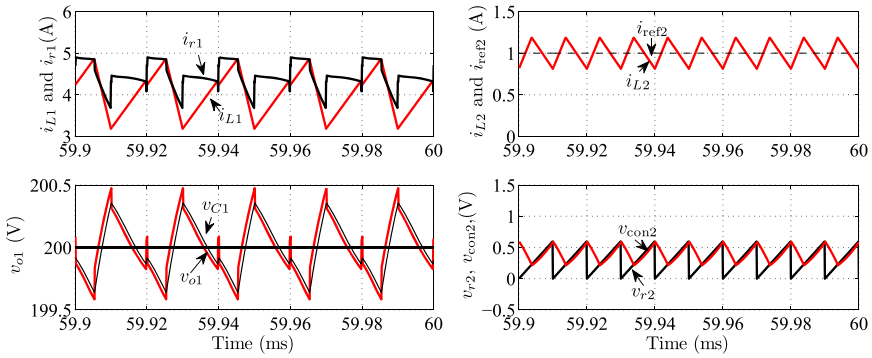
For switched linear systems, $\mathbf{f}_i = \mathbf{A}_i\mathbf{x} + \mathbf{B}_i$, and therefore $\Phi_i = \Phi_i(t_i - t_{i-1}) = e^{\mathbf{A}_i(t_i - t_{i-1})}$, $i = 1 \ldots N_c$, is the state transition matrix corresponding to the interval (t_{i-1}, t_i) within which the vector field $\mathbf{f}_i$ is taking place, $\mathbf{x}(0)$ is the value of the periodic orbit at the beginning of the its period which can obtained by enforcing periodicity during one cycle. It is worth noting that this approach can be applied to different periodic orbits (stable and unstable) of any period.

In this paper, we have used this approach for studying the stability of period-1, period-2, and period-4 orbits of the cascaded system for an operating mode characterized by $N_c = 3$, $N_c = 6$ (or $N_c = 5$), and

DOI: 10.1002/cta



(a) $\overline{m}_{a1} = 0.588$.



(b) $\overline{m}_{a1} = 0.546$.

Figure 6. Waveforms of the state variables and the control signals in the two stages for two different values of $\overline{m}_{a1}$ for $C_1 = 20\,\mu$F.

$N_c = 11$, respectively. The branches corresponding to these periodic orbits are shown in Figure 3. Their corresponding eigenvalues are shown in Tables II and III for $C_1 = 400$ and $C_1 = 20\,\mu$F, respectively, where the switching sequences are also indicated. The results from the stability analysis using the monodromy matrix are in perfect agreement with the brute force bifurcation diagrams presented in the previous section. In particular, the critical values of the normalized slope $\overline{m}_{a1}$ for the period-1 orbit to lose its stability are $\overline{m}_{a1} = 0.9618$ and $\overline{m}_{a1} = 0.5658$ for $C_1 = 400$ and $C_1 = 20\,\mu$F, respectively.

5. MODEL REDUCTION AND SIMPLIFIED STABILITY LIMITS IN THE PARAMETER SPACE

5.1. *Model reduction*

Although a full-order model can be used to obtain numerically the critical value of the parameters as it was performed in the previous section, it is more useful to have a simplified reduced-order model to derive from it explicit analytical expressions for the stability boundaries or to speed-up the simulation [16].

Table II. Eigenvalues of the fixed point with variation of the normalized slope $\overline{m}_{a1}$ for $C_1 = 400\,\mu$F.

$\overline{m}_{a1}$	Periodic orbit	Subsystem sequence	Eigenvalues
1.200	Stable period 1	[1-2-3]	-0.7833, 0.9968 ± 0.0072j, 0.8998, 0.0123
0.09617	Stable period 1	[1-2-3]	-0.9999, 0.9968 ± 0.0072j, 0.8998, 0.0123
0.9618	Unstable period 1	[1-2-3]	-1.0007, 0.9968 ± 0.0072j, 0.8998, 0.0123
0.9618	Stable period 2	[1-2-3 – 1-2-3]	0.9969, 0.9950 ± 0.0157j, 0.8097, 0.0002
0.9609	Stable period 2	[1-2-3 – 1-2-3]	0.9956, 0.9957 ± 0.0165j, 0.8097, 0.0002
0.9610	Unstable period 2	[1-2 – 1-2-3]	-1.0049, 0.9936 ± 0.0144j, 0.8097, 0.0002
0.9610	Unstable period 4	[1-2-3 – 1-2-3 –1-2 – 1-2-3]	-1.0083, 0.9869 ± 0.0287j, 0.6557, 0.016×10^{-6}

DOI: 10.1002/cta

Table III. Eigenvalues of the fixed point with variation of the normalized slope $\overline{m}_{a1}$ for $C_1 = 20\,\mu\text{F}$.

$\overline{m}_{a1}$	Periodic orbit	Subsystem sequence	Eigenvalues
1.200	Stable period 1	[1-2-3]	−0.2131, 0.9894, 0.9020, 0.7839, 0.0123
0.5659	Stable period 1	[1-2-3]	−0.9998, 0.9894, 0.9021, 0.7983, 0.0123
0.5658	Unstable period 1	[1-2-3]	−1.0000, 0.9894, 0.9021, 0.983, 0.0123
0.5658	Stable period 2	[1-2-3 – 1-2-3]	0.9838, 0.9765, 0.8140, 0.6449, 0.0002
0.5368	Stable period 2	[1-2-3 – 1-2-3]	0.9799, 0.7664 ± 0.1975j, 0.8101, 0.0001
0.5367	Unstable period 2	[1-2 – 1-2-3]	−1.2771, 0.9791, 0.8132, 0.6131, 0.0001
0.5367	Unstable period 4	[1-2-3 – 1-2-3 – 1-2-3 –1-2]	$-1.2496, 0.9586, 0.6614, 0.3913, 0.0290 \times 10^{-6}$

The inductor current i_{L2} in the second stage is programmed to track perfectly in average its reference current i_{ref2} by using a PI controller. Of course, this current controller may fail in carrying out this task, and the second stage may exhibit fast-scale subharmonic oscillation or slow-scale low-frequency oscillation. Both instabilities can be avoided by selecting appropriately the ramp slope or amplitude according to a traditional design because the output voltage in the second stage is constant. For instance, a deadbeat design will guarantee the recovery of the steady state in this stage after only one switching cycle in the presence of any disturbance. It should be noted here that because of using a PI compensator for controlling the average value instead of the peak value, the response does not strictly correspond to a deadbeat response unless the additional eigenvalue due to the integrator is also placed in the origin. In this case, the system will theoretically recover its steady state in two switching cycles instead of only one. However, it can be demonstrated that the discrete-time eigenvalue corresponding to the integrator is practically equal to 1, and as far as the dynamics of the inductor current is concerned, we can still say that this variable recovers its steady state in one switching cycle. Figure 7 shows the response of the second stage due to a 20% step change in the reference current i_{ref2}. Note that the system steady state is recovered in one cycle.

Under these conditions, the output port of the first stage can be substituted by a current sink with a current intensity $i_{L2} \approx i_{\text{ref2}}$ without losing accuracy [16]. Therefore, the cascaded system can be approximated by the simplified scheme depicted in Figure 8. The averaged output current in the second stage will be $i_{\text{ref2}}/M_2(D_2)$. The first stage can therefore be seen as a boost converter loaded by a current sink whose dynamic behavior and output voltage controller design have been recently addressed using the state-space averaging technique [14]. However, to the authors' knowledge, nonlinear analysis and the subharmonic oscillation phenomena have not been reported yet. The simplified system can be mathematically described by the following set of differential equations representing the reduced-order model:

$$\frac{\mathrm{d}i_{L1}}{\mathrm{d}t} = \frac{v_g}{L_1} - \frac{r_{L1} i_{L1}}{L_1} - \frac{v_{C1} + r_{C1}(i_{L1} - i_{\text{ref2}})}{L_1}(1 - \delta_1) \tag{17}$$

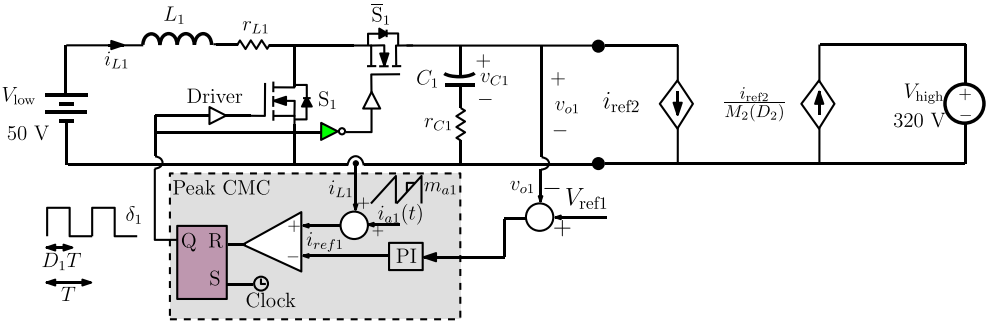


Figure 7. Response of the second stage due a 20% step change in the reference current i_{ref2}.

DOI: 10.1002/cta

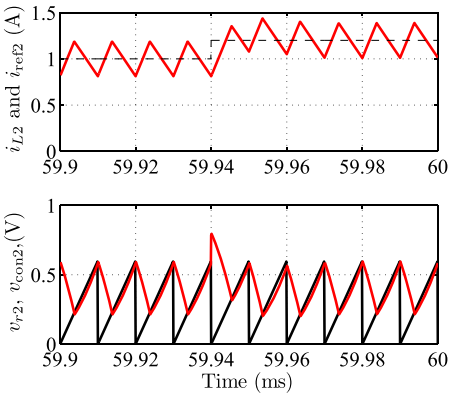


Figure 8. Schematic diagram of the simplified system.

$$\frac{dv_{C1}}{dt} = \frac{i_{L1}}{C_1}(1-\delta_1) - \frac{i_{ref2}}{C_1} \tag{18}$$

$$\frac{dx_3}{dt} = V_{ref1} - v_{C1} - r_{C1}i_{L1}(1-\delta_1) + r_{C1}i_{ref2} \tag{19}$$

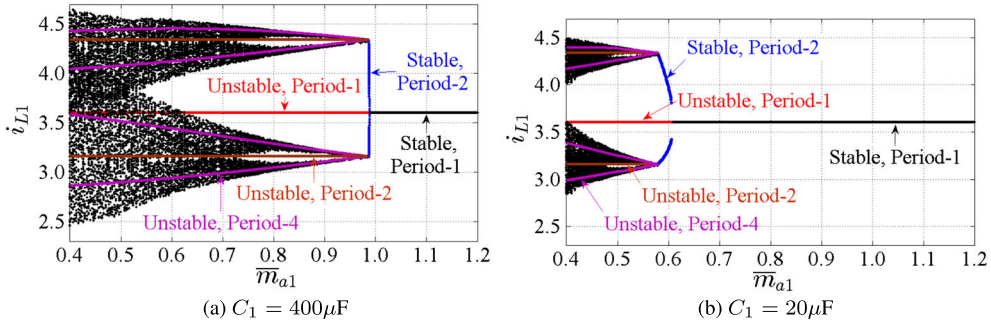
To validate this model, two bifurcation diagrams are obtained from it for the same parameter values considered for the full-order model. The results are shown in Figure 9. It can be observed that, apart from a slight shift of the critical value of $\overline{m}_{a1}$, a good agreement is obtained between the full-order model and the reduced-order model.

5.2. *Simplified stability boundaries in the parameter space*

The reduced-order model can be written in matrix form as follows:

$$\dot{\mathbf{x}} = \mathbf{A_1 x} + \mathbf{B_1 w} \quad \text{for } S_1 \text{ ON} \tag{20}$$

$$\dot{\mathbf{x}} = \mathbf{A_2 x} + \mathbf{B_2 w} \quad \text{for } S_1 \text{ OFF} \tag{21}$$



(a) $C_1 = 400\mu$F (b) $C_1 = 20\mu$F

Figure 9. Bifurcation diagram by taking $\overline{m}_{a1}$ as a bifurcation parameter for different values of C_1 using the reduced-order model.

DOI: 10.1002/cta

where

$$\mathbf{A}_1 = \begin{pmatrix} \dfrac{-r_{L1}}{L_1} & 0 & 0 \\ 0 & 0 & 0 \\ 0 & -1 & 0 \end{pmatrix}, \mathbf{B}_1 = \begin{pmatrix} \dfrac{1}{L_1} & 0 & 0 \\ 0 & -\dfrac{1}{C_1} & 0 \\ 0 & r_{C1} & 1 \end{pmatrix}, \tag{22}$$

$$\mathbf{A}_2 = \begin{pmatrix} \dfrac{-(r_{L1}+r_{C1})}{L_1} & -\dfrac{1}{L_1} & 0 \\ \dfrac{1}{C_1} & 0 & 0 \\ -r_{C1} & -1 & 0 \end{pmatrix}, \mathbf{B}_2 = \begin{pmatrix} \dfrac{1}{L_1} & 0 & 0 \\ 0 & -\dfrac{1}{C_1} & 0 \\ 0 & r_{C1} & 1 \end{pmatrix} \tag{23}$$

$$\mathbf{x} = \begin{pmatrix} i_{L1} \\ v_{C1} \\ x_4 \end{pmatrix}, \mathbf{w} = \begin{pmatrix} V_{\text{low}} \\ i_{\text{ref2}} \\ V_{\text{ref1}} \end{pmatrix} \mathbf{F}_1 = (1, W_v, -W_v\omega_{zv}) \tag{24}$$

Let $D_1 = D$ for simplicity of notation. Let us define the following matrix and vector duty cycle-dependent functions:

$$\Phi_1 = \exp(\mathbf{A}_1 DT), \quad \Phi_2 = \exp(\mathbf{A}_2(1-D)T), \quad \Phi = \Phi_2\Phi_1 \tag{25}$$

In [17,18], it has been shown that at the onset of subharmonic oscillation boundary, the following condition is fulfilled:

$$-\mathbf{F}_1(\mathbf{I}+\Phi)^{-1}\Phi_1(\mathbf{f}_1(\mathbf{x}(0)) + \mathbf{f}_2(\mathbf{x}(0))) = m_{a1} \tag{26}$$

where $\mathbf{f}_1(\mathbf{x}(0)) = \mathbf{A}_1\mathbf{x}(0) + \mathbf{B}_1\mathbf{w}$ and $\mathbf{f}_2(\mathbf{x}(0)) = \mathbf{A}_2\mathbf{x}(0) + \mathbf{B}_2\mathbf{w}$. For the boost converter, $\mathbf{B}_1 = \mathbf{B}_2 = \mathbf{B}$, and hence, (26) becomes

$$-\mathbf{F}_1\left[(\mathbf{I}+\Phi)^{-1}\right]\Phi_1(((\mathbf{A}_1+\mathbf{A}_2)\mathbf{x}(0) + 2\mathbf{B}\mathbf{w}). = m_{a1} \tag{27}$$

Although the previous equation is a closed-form expression for the stability boundary, which can be plotted as function of any parameter of the system, its use for design-oriented analysis is not easy. To overcome this problem, the following section provides an approximate closed-form expression of the stability boundaries in the parameter space that can be used for design purposes.

5.3. Design-oriented stability conditions

In order to obtain a design-oriented stability condition, we will perform a slope analysis as it is performed traditionally in many textbooks [1]. However, we will take into consideration the slope contributed by the output voltage, which is fed back through i_{ref1}. When i_{ref} is constant, the stability condition is (14). When i_{ref} is given by the voltage feedback loop, it contains switching ripple that alter the previous stability condition, which becomes

$$\frac{v_{o1}(D)}{L_1}\left(D - \frac{1}{2}\right) < m_a + m_{\text{ref1,ON}} \tag{28}$$

where $m_{\text{ref1,ON}}$ is the slope of the current reference i_{ref1} during the ON phase to be determined in the

DOI: 10.1002/cta

following. From (29), the inductor current reference i_{ref1} in the first stage is given by

$$i_{\text{ref1}} = W_v(V_{\text{ref1}} - v_{o1} + \omega_{zv} \int (V_{\text{ref1}} - v_{o1})\text{d}t) \tag{29}$$

Performing a piecewise linear approximation of the state variables and differentiating with respect to time, the steady-state slope $m_{\text{ref1,on}}$ of i_{ref1} during the conducting time is given by

$$m_{\text{ref1,ON}} = W_v\left(-m_{o1,\text{ON}} + \omega_{zv}(V_{\text{ref1}} - v_{o1})\right) \approx -W_v m_{o1,\text{ON}} \tag{30}$$

where $m_{o1,\text{ON}}$ is the slope of the output voltage of the first stage. In (33), it has been considered that $v_{o1} \approx V_{\text{ref1}}$. According to (19), the slopes of the intermediate capacitor voltage during the ON phase ($\delta_1 = 1$) is given by the equation

$$m_{C,\text{ON}} = -\frac{i_{\text{ref2}}}{C_1} \tag{31}$$

Accordingly and because $v_{o1} = v_{C1} + r_{C1}C_1\text{d}v_{C1}/\text{d}t$, the slope of the output voltage of the first stage is given by

$$m_{o1,\text{ON}} = -\frac{i_{\text{ref2}}}{C_1} - r_{C1}\frac{\text{d}i_{\text{ref2}}}{\text{d}t} \tag{32}$$

Hence, the slope contributed by the current reference i_{ref1} can be expressed by

$$m_{\text{ref1}} \approx W_v\left(\frac{i_{\text{ref2}}}{C_1} + r_{C1}\frac{\text{d}i_{\text{ref2}}}{\text{d}t}\right) \tag{33}$$

Therefore, (28) becomes

$$\frac{v_{o1}(D)}{L_1}\left(D - \frac{1}{2}\right) < m_a + W_v\left(\frac{i_{\text{ref2}}}{C_1} + r_{C1}\frac{\text{d}i_{\text{ref2}}}{\text{d}t}\right) \tag{34}$$

The new expression for the minimum ramp needed to avoid subharmonic oscillations in a current mode-controlled dual-stage cascaded boost converter is given by the expression

$$\underbrace{\frac{v_{o1}(D)}{L_1}\left(D - \frac{1}{2}\right) - W_v\left(\frac{i_{\text{ref2}}}{C_1} + r_{C1}\frac{\text{d}i_{\text{ref2}}}{\text{d}t}\right)}_{m_{a,\text{cri,new}}(D)} < m_{a1} \tag{35}$$

Although it is possible to simplify the expression by considering i_{ref2} constant, it is still possible to use the slope of the inductor current i_{L2} instead. This slope depends on the value of the inductance L_2 and the output voltage v_{o1} and can be expressed as $m_{\text{on},2} \approx v_{o1}/L_2$, and (34) finally becomes

$$\underbrace{\frac{v_{o1}(D)}{L_1}\left(D - \frac{1}{2}\right) - W_v\left(\frac{i_{\text{ref2}}}{C_1} + r_{C1}\frac{v_{o1}}{L_2}\right)}_{m_{a,\text{cri,new}}(D)} < m_{a1} \tag{36}$$

Figure 10 shows the boundary between stable and unstable regions in the parameter space $(C_1, \overline{m}_{a1})$ obtained from different expressions. In Figure 10(a), this boundary is obtained from stability analysis

DOI: 10.1002/cta

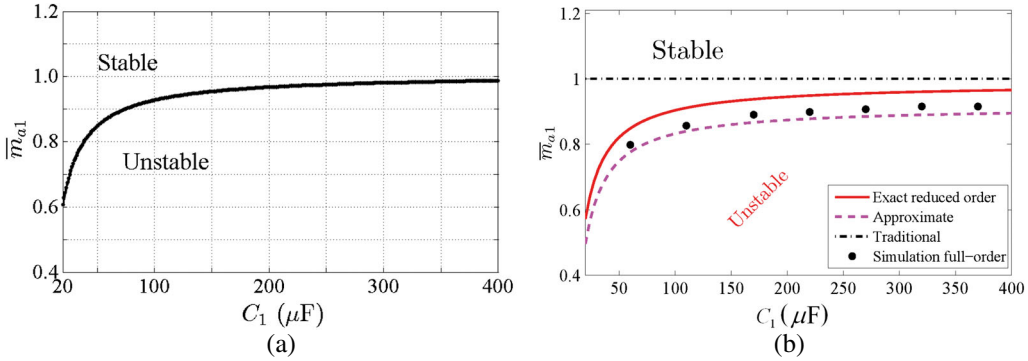


Figure 10. Boundary between stable and unstable regions in the parameter space $(C_1,\ \overline{m}_{a1})$, (a) using the monodromy matrix corresponding to the reduced-order system and (b) from the design-oriented approach.

using the monodromy matrix corresponding to the reduced-order system. In Figure 10(b), we show the results from the conventional expression (14), from the matrix-form expression (27), from the design-oriented expression (36), and from numerical simulations using the full-order model. Firstly, it can be observed from the presented results that the new critical value in (36) is smaller than the one obtained from the traditionally used expression (14). Therefore, a classical design procedure can predict subharmonic oscillation while the system is still stable. The new design-oriented expression is more accurate than the traditional expression. Secondly, it should be also noted that according to the results in Figure 10, (36) is more accurate than the exact stability boundary expression (27). The reason is that (36) takes into account the time-varying effect of i_{ref2}, which is not taken into account in (27). If i_{ref2} is considered constant in (36), the effects of r_{C1} and L_2 disappear from this equation, and the curves obtained from both expressions are almost coincident. Finally, it can be observed from (36) that the intermediate bus voltage contributes in the process of slope compensation. If C_1 decreases, the contributed slope increases because of the larger ripple involved, and therefore, the use of a smaller capacitance C_1 will require a smaller compensating slope m_{a1}.

6. CONCLUSIONS

Converters with high step-up conversion ratio are required for a variety of applications including DC distribution systems with photovoltaic electrical energy generation. Cascaded boost converter configuration is a preferred choice in achieving this requirement, because a desired output voltage/current can be obtained with higher efficiency than in single-stage systems and a specified variation in output voltage can be realized faster and more precisely. The penalty is the added complexity that follows from using a larger number of components and the possible interaction between the different stages.

In this paper, we have investigated the dynamical behavior of a cascade connection of current mode-controlled boost converters with a high conversion ratio. Floquet theory and Filippov method have been used to obtain the monodromy matrix for different periodic orbits together with their Floquet multipliers to explain the observed subharmonic oscillations and to obtain the stability boundary in the parameter space. We have reported the counter-intuitive observation that a smaller intermediate capacitance increases the stability of the system.

To obtain designer guidelines, a reduced-order model has been developed that has enabled us to obtain analytical expressions for the stability boundaries. By approximating the exact critical conditions under practical and realistic conditions, simple design-oriented expressions have been obtained for predicting subharmonic instability in the system.

The analysis of design-oriented expression reveals with relative ease the effect of each parameter upon the stability boundary, and its applicability has been demonstrated by means of numerical simulations from the full-order switched model. The paper finally formulates the stability condition in terms of the minimum ramp slope needed for removing fast-scale instability.

DOI: 10.1002/cta

ACKNOWLEDGEMENTS

The author would like to express their thanks to the anonymous reviewers for their comments that have helped in improving an initial version of this work. This project was supported by the NSTIP strategic technologies program in the Kingdom of Saudi Arabia – project no. 12-ENE3049-03. The authors also acknowledge with thanks the Science and Technology Unit, King Abdulaziz University, for the technical support.

REFERENCES

1. Erickson R, Maksimovic D. *Fundamentals of Power Electronics* (2nd edn). Springer: Kluwer, Norwell, MA, USA, 2001.
2. Garcerá G, González-Medina R, Figueres E, Sandia J. Dynamic modeling of DC–DC converters with peak current control in double-stage photovoltaic grid-connected inverters. *International Journal of Circuit Theory and Applications* 2012; **40**(8):793–813.
3. Chiu H-J, Lo Y-K, Lee T-P, Chen QS, Yu WL, Lee J-X, Shih F, Mou S-C. A battery charger with maximum power point tracking function for low-power photovoltaic system applications. *International Journal of Circuit Theory and Applications* 2011; **39**(3):241–256.
4. Li W, He X. Review of nonisolated high-step-up DC/DC converters in photovoltaic grid-connected applications. *IEEE Transactions on Industrial Electronics* 2011; **58**(4):1239–1250.
5. Haroun R, El Aroudi A, Cid-Pastor A, Garcia G, Martinez-Salamero L. Large-signal modeling and stability analysis of two-cascaded boost converters connected to a PV panel under SMC with MPPT. *IECON 2013 – 39th Annual Conference of the IEEE Industrial Electronics Society*, 10–13, 2013; 949–954.
6. Haroun R, Cid-Pastor A, El Aroudi A, Martinez-Salamero L. Synthesis of canonical elements for power processing in DC distribution systems using cascaded converters and sliding-mode control. *IEEE Transactions on Power Electronics* 2014; **29**(3):1366–1381.
7. Haroun R, El Aroudi A, Cid-Pastor A, Garcia G, Olalla C, Martinez-Salamero L. Impedance matching in photovoltaic systems using cascaded boost converters and sliding-mode control. *IEEE Transactions on Power Electronics* 2015; **30**(6):3185–3199.
8. Banerjee S, Verghese GC. *Nonlinear Phenomena in Power Electronics: Attractors, Bifurcations Chaos, and Nonlinear Control*. IEEE Press: New York, 2001.
9. Tse CK. *Complex Behavior of Switching Power Converters*. CRC Press: New York, 2003.
10. Zhusubalyev Z, Mosekilde E. *Bifurcations and Chaos in Piecewise-Smooth Dynamical Systems*. World Scientific: Singapore, 2003.
11. El Aroudi A, Debbat M, Olivar G, Benadero L, Toribio E, Giral R. Bifurcations in DC–DC switching converters: review of methods and applications. *International Journal of Bifurcation and Chaos* 2005; **15**(5):1549–1578.
12. Giaouris D, Maity S, Banerjee S, Pickert V, Zahawi B. Application of Filippov method for the analysis of subharmonic instability in DC–DC converters. *International Journal of Circuit Theory and Applications* 2009; **37**(8):899–919.
13. Giaouris D, Banerjee S, Stergiopoulos F, Papadopoulou S, Voutetakis S, Zahawi B, Pickert V, Abusorrah A, Al Hindawi M, Al-Turki Y. Foldings and grazings of tori in current controlled interleaved boost converters. *International Journal of Circuit Theory and Applications* 2014; **42**:1080–1091.
14. Yang S, Goto K, Imamura Y, Shoyama M. Dynamic characteristics model of bi-directional DC-DC converter using state-space averaging method. *IEEE INTELEC*, Scottsdale, AZ, 2012;1–5.
15. Mandal K, Chakraborty C, Abusorrah A, Al-Hindawi MM, Al-Turki Y, Banerjee S. An automated algorithm for stability analysis of hybrid dynamical systems. *The European Physical Journal Special Topics* 2013; **222**:757–768.
16. Pavlovic TB, Bjazić T, Ban Z. Simplified averaged models of DC–DC power converters suitable for controller design and microgrid simulation. *IEEE Transactions on Power Electronics* 2013; **28**(7):3266–3257.
17. El Aroudi A. A time-domain asymptotic approach to predict saddle-node and period doubling bifurcations in pulse width modulated piecewise linear systems. *MATEC web of Conferences*. *International Conference on Structural Nonlinear Dynamics and Diagnosis*, Agadir, Morocco, 2014.
18. El Aroudi A. A new approach for accurate prediction of subharmonic oscillation in switching regulators. *IEEE Transactions on Power Electronics* 2015. (submitted)

DOI: 10.1002/cta