Non-averaged Control-Oriented Modeling and Stability Analysis of DC-DC Switching Converters with Fixed Frequency Naturally Sampled Pulse Width Modulation and Integrating Feedback Loop

Y. Al-Turki¹, A. El Aroudi², K. Mandal³, D. Giaouris⁴, A. Abusorrah¹, M. Al Hindawi¹ and S. Banerjee⁵

¹Renewable Energy Research Group, Faculty of Engineering, King Abdulaziz University, Jeddah, Saudi Arabia
²GAEI research group, Dept. d'Enginyeria Electrònica, Elèctrica i Automàtica, Universitat Rovira i Virgili, 43007, Tarragona, Spain. Email address: abdelali.elaroudi@urv.cat.

³Department of Electrical & Electronics Engineering, National Institute of Technology Sikkim Ravangla, South Sikkim -737139, India

⁴School of Electrical and Electronic Engineering, Newcastle University, Newcastle upon Tyne, United Kingdom
 ⁵Indian Institute of Science Education & Research - Kolkata, Mohanpur Campus, Nadia-741246, W.B., India.

SUMMARY

This paper presents a unified and exact non-averaged approach to derive a frequency-domain control-oriented model for accurate prediction of the fast time-scale dynamics and performances of switching converters with fixed frequency naturally sampled pulse width modulation and integrating feedback loop. Because the approach avoids averaging and approximations related to this process, a very good accuracy of the derived model is obtained. The main difference between the presented approach and the existing methodology for accurately predicting the behavior of switching converters is that here we break the feedback loop and we focus on analyzing the open-loop gain and the effect of the system parameters on relative stability. This results in an approach much similar to control systems techniques rather than nonlinear dynamical system approaches. Consequently, the relative stability is tackled easily in the frequency domain. In particular, by treating the modulator as a gain depending on the operating point, the new model is formulated in such a way that standard control-oriented tools such as Bode diagrams and root-loci can be easily used. Therefore, the proposed approach gives some important issues like gain and phase margins that are highly useful in controller design. It is noticed that the crossover frequency, gain and phase margins predicted by using the averaged model may deviate significantly from the actual values given by

^{*}Correspondence to: Abdelali El Aroudi, Departament d'Enginyeria Electrònica, Elèctrica i Automàtica (DEEEA), Universitat Rovira i Virgili, Tarragona, Spain.

[†]E-mail: abdelali.elaroudi@urv.cat

the proposed approach. The paper points out the sources of discrepancies and the theoretical results are validated by simulations using a circuit-level switched model. Copyright © 2017 John Wiley & Sons, Ltd.

1. Introduction

Pulse Width Modulation (PWM) with natural sampling is the traditional technique for controlling DC-DC switching converters and it consists in imposing the duration during which a switch is maintained closed or open according to an appropriate compensated/filtered analog error signal by comparing it with a repetitive triangular or saw-tooth periodic signal [1, 2]. High performance controllers for switching converters can be strongly affected by the model accuracy. It is recognized that a of nonlinear phenomena can take place in DC-DC converters. These phenomena greatly downgrade the performance of these systems and reduce their lifetime. For example, when a period doubling bifurcation occurs the current ripple doubles and this increases the overall losses. Therefore, the prediction of these phenomena as in [3–7] with the ultimate aim of their avoidance as in [8–15] remains an important research topic.

The control loop of these systems is conventionally designed based on well-known linear techniques after the linearization of the nonlinear averaged model [1]. This makes the controller design a relatively easy task utilizing frequency-domain approaches such as Bode plots. However, the averaging approach, widely used in industrial applications, although it can provide useful insights for the designer on the system performance at the low frequency averaged dynamics, also leads to inaccurate conclusions about the actual behavior of the switched system at the fast time-scale. It is well known that DC-DC switching converters can exhibit instabilities at both the slow and the fast time-scale. While slow timescale low-frequency instabilities can be deeply analyzed and accurately predicted by using an averaged approach like in [3], the fast time-scale instabilities such as those corresponding to subharmonic oscillation are mainly due to the switching action which is destroyed by the averaging procedures. Therefore, using the averaged model for controller design, the performances are only guaranteed for the averaged dynamics and for a practical design they are *a posteriori* checked for the actual switched converter at a final design stage mainly by performing extensive time consuming trial and error numerical simulations to verify that the response of the switched system matches to some extent with the averaged one. It is worse, under large ripple conditions in the control signals, the averaged models not only cannot predict correctly the fast time-scale behavior of switching converters but also can inaccurately predict their DC steady-state value as reported in [16].

Extracting real converter dynamics taking into account the switching action lead to accurate

prediction of the system behavior [2, 17] and, in particular, predict faithfully the fast time-scale dynamics of these systems. An analysis taking into account the switching action at the modeling stage may offer an in-depth information about the dynamical behavior of the switched circuit and can be used to predict the real behavior due to the switching action [19] because eliminating averaging approximations improves the accuracy and extends the frequency range over which the model is valid. In an attempt to extend the validity of the design-oriented averaging approach to high frequencies using small-signal frequency domain models, an approach has been proposed in [18] consisting of augmenting the dimension of the averaged model by taking into account the switching effects. Recent results based on the describing function (DF) technique proved that the approach of [18] still fail short in predicting the behavior of switching converters under ripple-based control strategies that use the output voltage ripple in the fast loop [20, 21]. Other more advanced small-signal models and their equivalent circuit representations are also proposed in [22] based on a linearized DF method extending the results obtained in peak Current Mode Control (CMC) in [18] to average CMC.

Using discrete-time modeling and Floquet theory, it was demonstrated recently in [4] that the approach based on the DF models [22] is inaccurate for predicting the fast time-scale instabilities such as subharmonic oscillation in switching converters under ripple-based Voltage Mode Control (VMC) strategies. Under these circumstances, the use of average models is not justified when an exact discretization of the system dynamics is possible although much more involved [2]. This exact discretization lead to a model that circumvents all inaccuracies related to the approximation involved in the averaging approach.

Some discrete-time models reported in the literature are obtained by discretizing the average model and mapping the *s* plane to the *z*-domain using well known approximations such as Euler, bilinear, zero-order hold and pole zero matching transformations [23-25] and, although they are control-oriented models, they suffer from the the same inaccuracies inherited from the averaging process and those from the *s*-to-*z* transformation. The discrete-time models obtained by directly sampling the switched model are obtained using an exact discretization of this model [2, 26-32] are enough accurate but, except for digitally controlled converters with uniformly sampled PWM [27, 28, 32], they are of high level of abstraction to be appropriately used for design purposes. Hence, obtaining an optimal compromise between the accuracy and the control-oriented formulation is a real challenge. A natural question, therefore, arises: can a non-averaged model which takes into account the switching nonlinearity can be put into a control-oriented formulation for design and stability analysis like when the problem is addressed using the average approach? In this paper, we will show that the response to this question is affirmative.

Early developments along this line of research were reported for a boost converter by performing some approximations justified by the nature of the waveforms in this specific topology and the control used [2, 29, 31]. Simplified versions of DC-DC power converters that are obtained by removing the storing capacitors on the output circuits have been studied in [32]. In [33] a first-order current mode controlled buck converter is analyzed using a root-locus approach. The assumptions made in [29] allow to linearize the matrix exponentials and this is applicable also to the buck LED driver studied in [33] and the first-order buck and boost converters considered in [32]. In [34] the authors propose an approximate current discrete-time model for a digitally controlled multi-loop buck converter which achieves higher accuracy than the conventional averaged model at the fast time-scale.

The purpose of this paper is to present a general framework to extract small-signal control-oriented z-domain model of switching converters for accurate prediction of their dynamics and performances at the fast time-scale. The approach has a starting point an exact discretization of the state variables [2,32]. Hence, the model can be used for practical design to meet the system stability requirements while maximizing the bandwidth of the system thus and optimizing the fast controllers design. Unlike many existing models in the literature dealing with accurate prediction of switching converters based on non-averaging procedures [4, 17, 35-38], here we break the feedback loop and we focus on analyzing the open-loop gain and the effect of the system parameters on relative stability. As a consequence, the integral loop widely used in the output feedback to get zero static error, is separated from the rest of dynamics hence avoiding many singularity problems appearing in the expressions of the system trajectories and their steady-state values [5,6]. Using the obtained model, the relative stability analysis and the controller design of the DC-DC switching converter taking into account its switching nature can be addressed with a relative ease and without any singularity problem. The results are presented in a way to be control-oriented to facilitate parameter tuning using standard techniques such as root-locus and bode plots. The approach of this paper can be applied to any switching converter topology under both CMC and VMC. An example illustrate the different steps of the modeling while comparing the results from the new approach with those obtained from the conventional averaged model, pointing out the sources of discrepancies and validating the theoretical results by simulations using a detailed circuit-level switched model.

The rest of the paper is organized as follows. Section 2 revisits the unified open-loop piecewise linear switched model representation of switching regulators. Section 3 presents a review of their discrete-time modeling, the steady-state values of the state variables and the duty cycle in terms of the system parameters keeping in mind the previously mentioned separation between the integral variable and the rest of state variables. Section 4 presents the corresponding small-signal model in the vicinity of

Copyright © 2017 John Wiley & Sons, Ltd.

the operating point. From the previous model, the system loop gain is derived in Section 5. Taking a buck DC-DC converter under VMC with fixed frequency and natural sampling PWM as an example, a validation of the approach is given in Section 6 using control-oriented plots such as the Bode diagram and root-locus and a comparison is given with the averaged model highlighting the deficiencies of the last one in correctly predicting the behavior of the system at the fast-scale. Finally conclusions are drawn in the last section.

2. Unified open-loop piecewise linear models of switching regulators with an integrating feedback

loop

2.1. The open-loop continuous time switched model

The dynamics of a DC-DC switching regulator can be described by a state-space model that can be written in the following form [5]:

$$\dot{\mathbf{x}}(t) = \mathbf{A}_1 \mathbf{x}(t) + \mathbf{B}_1 \mathbf{w} \quad \text{for} \quad u = 1,$$
 (1a)

$$\dot{\mathbf{x}}(t) = \mathbf{A}_0 \mathbf{x}(t) + \mathbf{B}_0 \mathbf{w} \quad \text{for} \quad u = 0,$$
(1b)

$$\dot{v}_i(t) = v_r - y. \tag{1c}$$

where **x** is the vector of non-integral state variables, $\mathbf{A}_0 \in \mathbb{R}^{N \times N}$, $\mathbf{A}_1 \in \mathbb{R}^{N \times N}$, $\mathbf{B}_0 \in \mathbb{R}^{N \times p}$ and $\mathbf{B}_1 \in \mathbb{R}^{N \times p}$ are the system state matrices and $\mathbf{w} \in \mathbb{R}^p$ is the vector of the external parameters of the plant and/or the controller supposed to be constant within a switching cycle. The signal u in the model (1a)-(1b) is the driving signal which is generated by the PWM process to be described later. Eq. 1c describes the integrating feedback loop and the variable v_i in this equation stands for the integral of the sensed outer error signal $v_r - y$, where $y = \mathbf{Cx}$ is a suitable output variable, v_r is its desired reference and \mathbf{C} is row vector with appropriate dimension. The first differential equations for the system exclude the integral variable throughout. As commented previously, this variable was deliberately separated from the rest of state variables in the vector **x** to avoid some matrix singularity problems [5, 6].

2.2. The continuous-time switching condition dictated by the PWM

The driving signal u of the main switch is the result of comparing cyclically a control signal v_{con} depending on the state variables and a T-periodic ramp signal v_{ramp} together with additional logic rules dictated by a set-reset latch and a clock signal to force a single switching per cycle. Some VMC implementations do not use a latch [35, 37] but the approach presented here is still valid for these cases

provided that the T-periodic orbit is characterized by one and only one switching within the period T. Therefore any non-smooth instabilities due to multiple pulsing during one switching period or bordercollision bifurcations due to non presence of pulsing during one switching period are excluded from the analysis presented in this paper.

In Trailing Edge Modulation (TEM) strategies, the state of the main switch is forced to be ON (u = 1)at the beginning of each switching period and it is turned OFF (u = 0) whenever the control signal v_{con} and the ramp signal v_{ramp} intersect. The previous logic is inverted in Leading Edge Modulation (LEM) strategies. Hereinafter, let us focus our study on TEM strategies and hence the ratio of the first interval duration to the complete period $(nT, (n + 1)T), (n \in \mathbb{N})$ is the duty cycle d[n] of the square wave signal u in that period. This variable is dictated cyclically by the following switching condition that completes the model given in (1a)-(1c):

$$v_{\rm con}(t) = v_{\rm ramp}(t). \tag{2}$$

The variables $v_{\rm con}$ and $v_{\rm ramp}$ stand for the control and the ramp signals that can be expressed by:

$$v_{\rm con}(t) = \kappa (v_r - \mathbf{C}\mathbf{x}(t)) + W_i v_i(t)$$
(3a)

$$v_{\rm ramp}(t) = V_l + m_a(t \bmod T) \tag{3b}$$

where κ and W_i are suitable proportional and integral gains, V_l is the lower value of the ramp signal, $m_a = V_M/T$ is its slope, V_M is its amplitude and T is its period. The ramp voltage can be used either for modulation or for slope compensation. For instance, in conventional VMC, the ramp is used for modulation [7, 17, 35, 37] while in CMC and in ripple-based VMC, it is used for compensation [4, 25].

3. Review of discrete-time modeling of switching converters under PWM with integral feedback loop

3.1. Closed-form solution of the state variables

Our starting point is the discrete-time representation of a switching converter which is detailed in [2]. However, the integral variable is separated from the rest of dynamics hence avoiding many singularity problems appearing in the expressions of the system trajectories and their steady-state values [5, 6]. Since the state equations between the switching events are linear we can use the exact analytical solution to express the value of the state vector at the end of a switching cycle in terms of its value at the beginning of that cycle. By integrating (1a)-(1a), the trajectory $\mathbf{x}(t)$ of the system at time instant t starting from an initial condition $\mathbf{x}(t_0)$ at time instant t_0 can be expressed as follows:

$$\mathbf{x}(t) = \phi_u(t - t_0)\mathbf{x}(t_0) + \psi_u \mathbf{B}_u \mathbf{w}$$
(4)

Copyright © 2017 John Wiley & Sons, Ltd.

where $\phi_u(t)$ and $\psi_u(t)$ are defined by:

$$\phi_u(t) = e^{\mathbf{A}_u t} \quad \text{and} \quad \psi_u(t) = \mathbf{A}_u^{-1} (e^{\mathbf{A}_u t} - \mathbf{I})$$
(5)

Although ideally, the matrix A_1 for some converter topologies, like boost, Ćuk, SEPIC and flyback is singular, the parasitic resistances in the reactive components render this matrix invertible. This will not be the case, however, if the integral variable was included in the vector x.

By taking $t_0 = nT$ ($n \in \mathbb{N}$) and denoting $\mathbf{x}[n] = \mathbf{x}(nT)$, the mapping of the system described by the state equations given in (1a)-(1b) can be written in the following form [2]:

$$\mathbf{x}[n+1] := \mathbf{P}(\mathbf{x}[n], d[n])$$
$$= \mathbf{\Phi}(d[n])\mathbf{x}[n] + \mathbf{\Psi}(d[n])$$
(6)

where $\Phi(d[n])$ and $\Psi(d[n])$ are given by:

$$\Phi(d[n]) := \phi_0((1 - d[n])T)\phi_1(d[n]T)$$
(7a)

$$\Psi(d[n]) := \phi_0((1 - d[n])T)\psi_1(d[n]T)\mathbf{B}_1\mathbf{w} + \psi_0(d[n]T)\mathbf{B}_0\mathbf{w}$$
(7b)

According to (1c), the equation describing the error dynamics is given by:

$$\dot{v}_i = v_r - \mathbf{C}\mathbf{x} \tag{8}$$

By integrating (8) one obtains the following expression for the integral of the error $v_i(t)$:

$$v_i(t) = v_i(t_0) + (t - t_0)v_r - \mathbf{C} \int_{t_0}^t \mathbf{x}(t) d\tau$$
(9)

Let $v_i[n]$ be the integral of the error signal at the beginning of each switching period (at nT). The value of this variable at the time instants (n + d[n])T and (n + 1)T can therefore be expressed by:

$$v_i[n+d[n]] = v_i[n] + d[n]Tv_r - \mathbf{C}\mathcal{I}_1[n]$$
 (10a)

$$v_i[n+1] = v_i[n+d[n]] + (1-d[n])Tv_r - \mathbf{C}\mathcal{I}_0[n]$$
(10b)

where $\mathcal{I}_1[n]$ and $\mathcal{I}_0[n]$ are two integral vectors given by:

$$\mathcal{I}_{1}[n] = \int_{nT}^{(n+d[n])T} (\phi_{1}(t-nT)\mathbf{x}_{n} + \psi_{1}(t-nT)\mathbf{B}_{1}\mathbf{w})dt$$
(11a)
$$\mathcal{I}_{0}[n] = \int_{(n+d[n])T}^{(n+1)T} (\phi_{0}(t-(n+d[n])T)(\phi_{1}(d[n]T)\mathbf{x}_{n} + \psi_{1}(d[n]T)\mathbf{B}_{1}\mathbf{w})$$
$$+ \psi_{1}(t-(n+d[n])T)\mathbf{B}_{0}\mathbf{w})dt$$
(11b)

Copyright © 2017 John Wiley & Sons, Ltd.

Eqs. (10a)-(10b) define the mapping P_i corresponding to the integral variable v_i . This mapping can be expressed as follows:

$$v_{i}[n+1] := P_{i}(\mathbf{x}[n], v_{i}[n], d[n])$$

= $v_{i}[n] + T(v_{r} - y_{avg}[n])$ (12)

where $y_{avg}[n]$ is the moving average of the output variable y which is given by:

$$y_{\text{avg}}[n] = \frac{1}{T} \int_{nT}^{(n+1)T} y(t) dt = \frac{1}{T} \mathbf{C}(\mathcal{I}_1[n] + \mathcal{I}_0[n])$$
(13)

The complete model in the discrete-time domain can be obtained by combining (7b) and (12) taking into account (11a)-(11b) and (13).

As mentioned previously, the duty cycle d[n] is imposed by the PWM process cycle by cycle. The feedback loop together with the PWM process imposes the following constraint between the duty cycle d[n], the state vector $\mathbf{x}[n + d[n]]$ and the integral variable $v_i[n + d[n]]$:

$$\sigma(\mathbf{x}[n+d[n]], d[n]) := v_{\rm con}[n+d[n]] - v_{\rm ramp}[n+d[n]] = 0$$
(14)

where, according to (3a)-(3b), $v_{con}[n+d[n]]$ and $v_{ramp}[n+d[n]]$ can be expressed as follows:

$$v_{\rm con}[n+d[n]] = \kappa(v_r - \mathbf{Cx}[n+d[n]]) + W_i v_i[n+d[n]]$$
(15a)

$$v_{\rm ramp}[n+d[n]] = V_l + m_a d[n]T$$
(15b)

The constraint given in (14) is nonlinear in d[n] and it is responsible for many nonlinear phenomena that takes place in switching converters under PWM.

3.2. The fundamental steady-state periodic response of the system

In this subsection, let D be the steady-state duty cycle d[n] and let $\overline{D} = 1 - D$. Let us define $\Phi_1 = e^{\mathbf{A}_1 DT}, \ \Phi_0 = e^{\mathbf{A}_0(1-D)T}, \ \Psi_1 = \mathbf{A}_1^{-1}(e^{\mathbf{A}_1 DT} - \mathbf{I})^{-1}$ and $\Psi_0 = \mathbf{A}_0^{-1}(e^{\mathbf{A}_0 \overline{D}T} - \mathbf{I})^{-1}$. Let $\Phi = \Phi_1 \Phi_0, \ \Psi = \Phi_1 \Psi_0 \mathbf{B}_0 \mathbf{w} + \Psi_1 \mathbf{B}_1 \mathbf{w}$ and $\overline{\Phi} = \Phi_0 \Phi_1, \ \overline{\Psi} = \Phi_0 \Psi_1 \mathbf{B}_1 \mathbf{w} + \Psi_0 \mathbf{B}_0 \mathbf{w}$. Let $\mathbf{x}(0)$ and $\mathbf{x}(DT)$ be the steady-state values of the vector \mathbf{x} at the starting of the switching period and at the time instant DT respectively. By enforcing periodicity in steady-state regime, $\mathbf{x}(0)$ and $\mathbf{x}(DT)$ can be obtained and they are given by:

$$\mathbf{x}(0) = (\mathbf{I} - \overline{\mathbf{\Phi}})^{-1} \overline{\mathbf{\Psi}}$$
(16a)

$$\mathbf{x}(DT) = (\mathbf{I} - \mathbf{\Phi})^{-1} \mathbf{\Psi}$$
(16b)

Copyright © 2017 John Wiley & Sons, Ltd.

where the matrix $(\mathbf{I} - \mathbf{\Phi})$ and $\mathbf{I} - \overline{\mathbf{\Phi}}$ are nonsingular since the integral variable was separated from the rest of state variables within the vector \mathbf{x} . Note that if the integral variable v_i was included in the state vector \mathbf{x} , the previous matrices will be singular and their inverse will not exist.

3.3. The steady-state value of the duty cycle for the fundamental periodic regime

A necessary condition for the system to have a periodic orbit in steady-state is that $v_i[n] = v_i[n+1] = v_i[\infty]$, where $v_i[\infty]$ is the steady-state value of $v_i[n]$. Therefore, according to (12), the following equality must hold in steady-state:

$$y_{\rm avg}[\infty] = v_r \tag{17}$$

In turn, the steady-state average value $y_{avg}[\infty]$ is the constant term (DC component) of y(t) and can be obtained using the averaged model. This establishes the following relationship between the steady-state duty cycle D and $y_{avg}[\infty]$:

$$y_{\text{avg}}[\infty] = -\mathbf{C}(\mathbf{A}_1 D + \mathbf{A}_0 \overline{D})^{-1} (\mathbf{B}_1 D + \mathbf{B}_0 \overline{D}) \mathbf{w}$$
(18)

As commented in [5, 6], the steady-state value D can be obtained from the previous equation once all the matrices and the parameters of the system are specified and there is no need to obtain it using numerical root-finding algorithms such as in previous studies like [4,17,35,37,38]. Once D is obtained, the steady-state state vector $\mathbf{x}(0)$ and $\mathbf{x}(DT)$ are straightforward from (16a) and (16b) respectively.

4. Control-oriented discrete-time modeling of a switching regulator

Let us define the deviations $\hat{\mathbf{x}}[n]$, $\hat{d}[n]$ and $\hat{y}[n]$ from their respective steady-state values $\mathbf{x}(0)$, D and y(0) in such a way that:

$$\mathbf{x}[n] = \mathbf{x}(0) + \hat{\mathbf{x}}[n], d[n] = D + \hat{d}[n], y[n] = y(0) + \hat{y}[n]$$
(19)

Let us assume that these deviations are much smaller than their corresponding steady-state values, i.e, $\hat{\mathbf{x}}[n] \ll \mathbf{x}(0)$, $\hat{d}[n] \ll D$ and $\hat{y}[n] \ll y(0)$. Then, higher order terms can be neglected and by linearizing (6), (12) and (14), the small-signal model of a switching regulator can be conveniently



Figure 1. Equivalent block diagram of a switching DC-DC regulator under a naturally sampled fixed frequency PWM control strategy..

written in a control-oriented form as follows:

$$\hat{\mathbf{x}}[n+1] = \mathbf{\Phi}\hat{\mathbf{x}}[n] + \mathbf{J}_d \hat{d}[n], \qquad (20a)$$

$$\hat{v}_{o,n} = \mathbf{C}\hat{\mathbf{x}}[n], \tag{20b}$$

$$\hat{v}_i[n+1] = \mathbf{J}_i \hat{\mathbf{x}}[n] + \hat{v}_i[n],$$
 (20c)

$$\hat{v}_{con}[n+d[n]] = -\mathbf{K}\hat{\mathbf{x}}[n] + W_i\hat{v}_i[n],$$
 (20d)

$$\hat{d}_n = H_m \hat{v}_{\rm con}[n+d[n]]. \tag{20e}$$

where \mathbf{J}_d , \mathbf{J}_i , \mathbf{K} and H_m are given by the following expressions:

$$\mathbf{J}_{d} = \frac{\partial \mathbf{P}}{\partial d} = T(\mathbf{\Phi}_{0}(\mathbf{A}_{1} - \mathbf{A}_{0})\mathbf{x}(DT) + (\mathbf{B}_{1} - \mathbf{B}_{0})\mathbf{w}),$$
(21a)

$$\mathbf{J}_{i} = \frac{\partial P_{i}}{\partial \mathbf{x}} = -\mathbf{C}(\boldsymbol{\Psi}_{1} + \boldsymbol{\Psi}_{0}\boldsymbol{\Phi}_{1}), \tag{21b}$$

$$\mathbf{K} = \mathbf{C}(\kappa \mathbf{\Phi}_1 + W_i \mathbf{\Psi}_1), \tag{21c}$$

$$H_m = \frac{1}{T(\kappa \mathbf{C}(\mathbf{A}_1 \mathbf{x}(DT) + \mathbf{B}_1 \mathbf{w}) - W_i(v_{\text{ref}} - \mathbf{C}\mathbf{x}(DT)) + m_a)}.$$
 (21d)

An equivalent block diagram of the previous model, first proposed in [39] without taking into account the integral variable, is depicted in Fig. 1.

It is worth to note that (20d) describes the effect of a small perturbation in the control voltage v_{con} at time instant d[n]T onto the duty cycle d[n], and therefore H_m stands for the discrete-time PWM small-signal gain.

Remark 1: Conventionally, using the averaged model, the modulator gain is a constant equal to the reciprocal of the modulator ramp signal amplitude V_M . It has been widely believed for many

decades that in VMC with naturally sampling switching frequency, the modulator transfer function has no dependence of the switching frequency. One can observe in (21d) that if the control signal has negligible switching ripple in such a way that $\kappa \mathbf{C}(\mathbf{A}_1\mathbf{x}(t) + \mathbf{B}_1\mathbf{w})(\mathbf{x}(DT)) \approx 0$ and because $\mathbf{C}\mathbf{x}(DT) \approx v_r$, the expression of the modulator gain can be simplified as $H_m \approx 1/(Tm_a) = 1/V_M$ which is the expression used in the averaged model [1].

Remark 2: The gain H_m in (21d) is not constant and it depends on the steady-state operating duty cycle D. In particular it depends on the slope $-\kappa \mathbf{C}(\mathbf{A}_1\mathbf{x}(DT) + \mathbf{B}_1\mathbf{w})$ of the control voltage v_{con} evaluated at the time instant DT. If this slope monotonically increases with the steady-state duty cycle D like in CMC and in ripple-based VMC schemes, H_m is monotonically increasing with D reaching its maximum value at D = 1 and its minimum value at D = 0. However, in buck converters under a conventional VMC strategy, the slope of v_{con} at time instant DT, is a convex function of D and the gain H_m inherits the same shape.

Remark 3: The gain H_m in (21d) is not exactly the complete PWM modulator transfer function since a term is missing in the expression of H_m and which is included in the expression of the feedback vector **K**.

5. The system loop gain in the z-domain

Supposing zero initial conditions and performing z-transform in (20a) and (20b), the \hat{d} -to- \hat{v}_o transfer function can be expressed as follows:

$$H_p(z) := \frac{\hat{v}_o(z)}{\hat{d}(z)} = \frac{\operatorname{Cadj}(z\mathbf{I} - \boldsymbol{\Phi})\mathbf{J}_d}{\det(z\mathbf{I} - \boldsymbol{\Phi})} = \frac{\det(z\mathbf{I} - \boldsymbol{\Phi} + \mathbf{J}_d\mathbf{C}) - \det(z\mathbf{I} - \boldsymbol{\Phi})}{\det(z\mathbf{I} - \boldsymbol{\Phi})}$$
(22)

According to (20c), the transfer function $H_i(z)$ of the analog integrator can be obtained from the following expression relating the z-transform of the integral variable v_i to the z-transform of the rest of the state variables x:

$$V_i(z) = \frac{\mathbf{J}_i}{z - 1} \mathbf{X}(z)$$
(23)

where $V_i(z)$ and $\mathbf{X}(z)$ are the z-transform of $v_i[n]$ and $\mathbf{x}[n]$ respectively. The transfer function between the vector state variables \mathbf{x} and the control signal v_{con} in the z-domain can be derived by combining (20d) with (23) hence obtaining:

$$V_{\rm con}(z) = \left(-\mathbf{K} + \frac{W_i}{z-1}\mathbf{J}_i\right)\mathbf{X}(z)$$
(24)

Copyright © 2017 John Wiley & Sons, Ltd.

where $V_{con}(z)$ is the z-transform of $v_{con}[n + d[n]]$. Taking into account (20c) and (20d), the \hat{d} -to- \hat{v}_{con} transfer function (total loop gain $\mathcal{L}(z)$ by excluding H_m) can be expressed in the z-domain as follows:

$$\frac{\hat{v}_{\rm con}(z)}{\hat{d}(z)} := \mathcal{L}(z) = (-\mathbf{K} + \frac{W_i}{z - 1} \mathbf{J}_i) \frac{\operatorname{adj}(z\mathbf{I} - \boldsymbol{\Phi})}{\det(z\mathbf{I} - \boldsymbol{\Phi})} \mathbf{J}_d$$
(25)

Therefore, $\mathcal{L}(z)$ can be expressed in the following form:

$$\mathcal{L}(z) = \frac{\Delta_1 - \Delta_2}{(z - 1)\Delta_2} \tag{26}$$

where Δ_1 and Δ_2 are given by the following expressions:

$$\Delta_1 = \det(z\mathbf{I} - \mathbf{\Phi} + (W_i\mathbf{J}_i - (z-1)\mathbf{K})\mathbf{J}_d)$$
(27a)

$$\Delta_2 = \det(z\mathbf{I} - \boldsymbol{\Phi}) \tag{27b}$$

The open-loop zeros and poles can be straightforwardly calculated from the total loop gain in (26) and these can be used for controller-design. In particular one can note that in the z-domain the integrator introduces an open-loop pole at 1 and that the remaining open-loop poles can be obtained by solving the equation $det(z\mathbf{I} - \boldsymbol{\Phi}) = 0$ either analytically for low-order converters or using CAD tools such as Matlab[©] for high-order converters. The closed-loop poles of the system can be obtained from the following characteristic equation [40]:

$$1 + H_m \mathcal{L}(z) = 0 \tag{28}$$

This is a control-oriented characteristic equation like in digital control systems [40] and can be used for designing the feedback of the switching converter by considering H_m as a proportional gain for the total loop $\mathcal{L}(z)$.

6. Example: A buck converter under analog PI VMC with fixed frequency naturally sampled PWM

6.1. System description

Fig. 2 shows the circuit diagram of a buck DC-DC converter under PI VMC. For simplicity, the voltage loop is closed by a simple PI controller whose transfer function can be expressed as follows:

$$H_c(s) = \kappa \left(1 + \frac{1}{\tau_i s} \right) \tag{29}$$

where, according to Fig. 2, $\kappa = R_2/R_1$ is a suitable proportional feedback gain and $\tau_i = R_2C_i$ is the integrator time constant ($W_i = R_2/(R_1\tau_i)$) is the integrator gain). The approach can be applied to more practical controllers of of buck converters such as the type-III compensator [7].



Figure 2. Circuit diagram of a DC-DC buck converter under analog PI VMC with fixed frequency naturally sampled PWM.

6.2. The continuous-time piecewise linear switched model

Let v_C be the voltage of the output capacitor and i_L the inductor current. By applying KVL to the power stage we obtain the following set of differential equations:

$$\frac{\mathrm{d}v_C}{\mathrm{d}t} = -\alpha \frac{v_C}{RC} + \alpha \frac{i_L}{C}, \qquad (30a)$$

$$\frac{\mathrm{d}i_L}{\mathrm{d}t} = -\alpha \frac{v_C}{L} - \frac{\alpha r_C + r_L}{L} i_L + \frac{v_s}{L} u, \qquad (30b)$$

where $\alpha = R/(R + r_C)$, C is the capacitance of the output capacitor with ESR r_C , L is the inductance of the inductor with winding resistance r_L , R is the load resistance, v_s is the input source voltage. All these parameters can be identified in the schematic circuit diagram of Fig. 2. The output voltage v_o applied to the load R can be expressed as follows:

$$v_o = \alpha (v_C + r_C i_L) \tag{31}$$

Note that with an ideal capacitor, $r_C = 0$, then $\alpha = 1$ and $v_o = v_C$. Let $\mathbf{x} = (v_C, i_L)^{\mathsf{T}}$ be the vector of the state variables by excluding the integral variable. Let $\mathbf{C} = \alpha(1, r_C)$. The matrices $\mathbf{A}_1, \mathbf{A}_0, \mathbf{B}_1$, \mathbf{B}_0 and the external input vector \mathbf{w} are given by:

$$\mathbf{A}_{1} = \mathbf{A}_{0} = \mathbf{A} = \begin{pmatrix} -\frac{\alpha}{RC} & \frac{\alpha}{C} \\ -\frac{\alpha}{L} & -\frac{\alpha r_{C} + r_{L}}{L} \end{pmatrix}, \qquad (32a)$$

$$\mathbf{B}_{1} = \mathbf{B} = \begin{pmatrix} 0\\ \frac{1}{L} \end{pmatrix}, \quad \mathbf{B}_{0} = \mathbf{0}, \quad \mathbf{w} = v_{s}$$
(32b)

Copyright © 2017 John Wiley & Sons, Ltd.

The open-loop poles of the system in the continuous-time domain are the eigenvalues of the matrix A and these are given in a canonical form in terms of the quality factor Q and the natural frequency ω_n as follows [1]:

$$p^+ = -\frac{\omega_0}{2Q}(1 - \sqrt{1 - 4Q^2})$$
 (33a)

$$p^{-} = -\frac{\omega_0}{2Q} (1 + \sqrt{1 - 4Q^2})$$
(33b)

where ω_n and 1/Q are

$$\begin{split} \omega_n &= \sqrt{\frac{R+r_L}{(R+r_C)LC}}, \\ \frac{1}{Q} &= \frac{Z_0 + \left(R(r_C+r_L) + r_C r_L\right)/Z_0}{\sqrt{(R+r_C)(R+r_L)}}, \end{split}$$

and $Z_0 = \sqrt{L/C}$. In z-domain, for this second-order switching converter, the open-loop poles are the roots of the following polynomial:

$$\Delta_2(z) = z^2 + \operatorname{tr}(e^{\mathbf{A}T})z + \det(e^{\mathbf{A}T})$$
(34)

These open-loop poles can be used to predict the evolution of the closed-loop poles (root-locus) in the z-domain. The open-loop poles in this domain are related to the ones in the s- domain given in (33a)-(33b) as follows:

$$p_z^+ = e^{p^+T} = e^{-\frac{\omega_0 T}{2Q}(1+\sqrt{1-4Q^2})}$$
 (35a)

$$p_z^- = e^{p^- T} = e^{-\frac{\omega_0 T}{2Q}(1 - \sqrt{1 - 4Q^2})}$$
 (35b)

The zeros can be derived by setting the numerator of $\mathcal{L}(z)$ to zero ($\Delta_1 = \Delta_2$) and solving for z. In particular, one of the zeros is introduced by the integrator and can be approximated by:

$$z_{\rm pi} \approx e^{-W_i T/\kappa} = e^{-T/\tau_i} \approx 1 - \frac{T}{\tau_i}$$
(36)

One can observe that this zero is always smaller than 1 but very close to it and is shifted to the left when τ_i increases. Another zero is given by [28]

$$z_c \approx \frac{r_C (T^2 R + RLC - TL)}{LR(T + r_C C)} \tag{37}$$

This zero is located at the origin if $r_C = 0$ and it is shifted to the right when r_C increases being its value independent on the operating duty cycle D. The steady-state value of the vector of the state variables $\mathbf{x}(DT)$ in (16b) can be expressed for the buck converter as follows:

$$\mathbf{x}(DT) = (\mathbf{I} - e^{\mathbf{A}T})^{-1} \mathbf{A}^{-1} (e^{\mathbf{A}T} - e^{\mathbf{A}\overline{D}T}) \mathbf{B} v_s.$$
(38)

Copyright © 2017 John Wiley & Sons, Ltd.



Figure 3. Evolution of the PWM gain H_m in term of the steady-state duty cycle D. The constant gain corresponding to the averaged model is also shown in dashed line.

Note that because the integral action was separated from the rest of system dynamics, the matrices **A** and $\mathbf{I} - e^{\mathbf{A}T}$ are invertible and $\mathbf{x}(DT)$ is unique. This will not be the case if the integral action was included in the vector \mathbf{x} [5,6]. According to (18), the value of the steady-state duty cycle is given by the following expression:

$$D = \frac{v_{\text{ref}}}{-\mathbf{C}\mathbf{A}^{-1}\mathbf{B}v_s} = \frac{v_{\text{ref}}(\alpha(R+r_C)+r_L)}{\alpha(R+r_C)v_s}.$$
(39)

which is in agreement with the well-known expression $D = v_{ref}/v_s$ for the buck converter obtained from a steady-state analysis based on net volt-seconds assuming low ripple at the output voltage and ideal components ($r_C = r_L = 0$) [1].

6.3. Validation of the small-signal control-oriented model by means of numerical simulations using the switched circuit-level model

Let us take the following power stage parameter values: inductance $L = 120 \ \mu$ H, winding resistance $r_L = 0.04$, Ω , capacitance $C = 22 \ \mu$ F, ESR $r_C = 0.05 \ \Omega$, input voltage $v_s = 12$ V, output voltage reference $v_{ref} = 5$ V, load resistance $R = 2.5 \ \Omega$, proportional gain $\kappa = 4$ and switching frequency $f_s = 50$ kHz. The time constant of the PI integrator is selected to be $\tau_i = 5\sqrt{LC} \approx 203 \ \mu$ s which is enough larger than $RC = 55 \ \mu$ s and the system is stable at the slow scale according to [3].

Fig. 3 shows the evolution of the PWM gain H_m as function of the steady-state duty cycle D. The constant gain of the PWM conventionally used in the averaged model is also shown in the same figure.



Figure 4. The bifurcation diagram of the buck converter taking the modulator gain H_m as a bifurcation parameter. The critical value is $H_m \approx 0.51$.

Note that the different gains coincide only for D = 1. For $r_C = 0$ they also coincide for D = 0. The error is maximum in the vicinity of D = 0.5. It can also be demonstrated that if a significant amount of inductor current i_L feedback is used in the control signal either through CMC or through significant effect of the ESR r_C , the discrepancy between the modulator gains monotonically increases by decreasing the steady-state duty cycle D reaching its maximum value at D = 0.

6.4. Steady-state behavior from simulation of the switched model

Let us now focus on the steady-state behavior of the system whose evolution can be checked by using a bifurcation diagram when a suitable parameter is varied. Such a diagram is shown in Fig. 4 and can be used to explore the different steady-state regimes that the system can exhibit. Here we consider the PWM gain H_m as bifurcation parameter. According to (21d), this gain can be varied by changing many parameters such as the steady-state duty cycle D, the switching frequency 1/T or equivalently the slope m_a of the ramp signal. However, it is necessary that only H_m is changed and not the operating points $\mathbf{x}(0)$ and $\mathbf{x}(DT)$. Hence, we cannot use D or T for changing H_m . Varying κ although it does not alter the operating point, it will change, at the same time, both H_m and \mathbf{K} . Hence in order to change only H_m while maintaining constant other parameters of the total loop gain \mathcal{L} , we do it through the amplitude of the ramp voltage V_M . The obtained bifurcation diagram shows that the system behavior is periodic for relatively low values of the gain H_m . However, as this parameter is increased beyond a critical

Copyright © 2017 John Wiley & Sons, Ltd.

value $H_m \approx 0.51$, one can observe that the system exhibits a period doubling bifurcation leading to subharmonic oscillation and chaotic regime with the same characteristics reported in [7, 17, 35, 37]. From a design point of view, it is very important to be able to predict the onset of instability using control-oriented models and standard control system tools such as Bode and root-locus plots rather than bifurcation diagrams. Next, these two control-oriented plots will be used to predict this critical value of H_m .

6.5. A control-oriented root-locus approach for predicting subharmonic oscillation

Fig. 5 shows a root-locus plot of the system by using the Matlab[©] command RLOCUS applied to the loop gain $\mathcal{L}(z)$. This plot shows that the closed-loop poles leave the unit circle at the point z = -1 when $H_m = 0.51$ in agreement with the bifurcation diagram of Fig. 4.



Figure 5. The root-locus of the total loop gain as H_m is varied. The critical value is $H_m \approx 0.51$ in agreement with Fig.4.

Remark 4: It can be observed that one of the closed-loop poles is very close to 1 tending, when H_m is increased, to the open-loop zero $z_{pi} \approx 0.924$ from the open-loop pole $p_{pi} = 1$, both introduced by the PI controller. This is in agreement with root-locus theory from which it is well-known that the closed loop poles tend to the open-loop zeros when the gain increases [40]. From the root-locus in Fig. 5 it can be observed that the loci of the complex conjugate poles, when the control parameter changes, involves practically a circle because $z_{pi} \approx p_{pi}$ and these cancel each other. The center of the circle is at the zero $z_c \approx 0.046$ (0 for the ideal buck converter) and its radius is $\rho \approx \sqrt{\Re((p_z^+) - z_c)^2 + \Im(p_z^+)^2} \approx 0.8$.

Copyright © 2017 John Wiley & Sons, Ltd.

The root-locus plot also shows that the closed loop poles are approaching the real axis at $z \approx -0.77$. In general, for finding the points at which the root locus breaks into real axis, one has to maximize or minimize the gain (H_m) with respect to z [40]. For the buck converter under PI VMC, the break-in point can be identified easily since the radius of the circle and the location of the zero z_c are known.

Remark 5: In previous studies like [35], the monodromy matrix was computed numerically using central differences and Richardson extrapolation and it was observed that the poles are complex conjugates that move on a circle of radius equal to $\rho = 0.8241$. In [35], no ESR r_C and no r_L have been considered, $\alpha = 1$ and only a proportional controller was used. If the same parameter values in [35] are used, according to (35a)-(35b), the radius of the circle formed by the closed-loop poles can be obtained from $\rho = e^{-\omega_0 T/(2Q)} \approx 0.8241$ in agreement with the results in [35] which have been entirely determined by numerical procedures. This is also in agreement with [17] which also used a numerical approach to determine the steady-state duty cycle D and to determine the steady-state periodic orbit $\mathbf{x}(DT)$. There, the periodic orbit are located by the Newton-Raphson method, and in the process of convergence, the partial derivatives from which the Jacobian of the mapping can be derived are obtained. Here, most of the steps are evaluated analytically. On the other hand, while in previous studies, the evolution of the poles are plotted after solving the eigenvalue problem of the Jacobian matrix or the monodromy matrix, here available command in commercial software are used. *Hence, the plot of the poles and zero can be obtained using the root-locus plots of most CAD programs.* Except from evaluating the matrix exponential, all the steps are performed analytically including the determination of the steady-state duty cycle, locating the fixed points $\mathbf{x}(DT)$ and evaluating the zdomain total loop.

6.6. A control-oriented frequency domain approach for predicting subharmonic oscillation

This section addresses the prediction of the period doubling boundary from a frequency domain standpoint with the final aim of tuning the system parameters. Having obtained the z-domain transfer function of the buck switching power converter $\mathcal{L}(z)$, its frequency response $\mathcal{L}(e^{j\omega T})$ can be easily derived by substituting, $z = e^{j\omega T}$ [2, 39, 41] therefore obtaining:

$$\mathcal{L}(e^{j\omega T}) = (-\mathbf{K} + \frac{W_i}{e^{j\omega T} - 1} \mathbf{J}_i)((e^{j\omega T}\mathbf{I} - \mathbf{\Phi})^{-1})\mathbf{J}_d$$
(40)

The subharmonic oscillation occurrence implies that -1 is a pole of the characteristic equation, i.e., $1 + H_m \mathcal{L}(-1) = 0$. In the frequency domain this condition can be expressed as follows: [39]:

$$H_m \mathcal{L}(-1) = -1 \Rightarrow \begin{cases} |\mathcal{L}(-1)| = \frac{1}{|H_m|} \\ \angle \mathcal{L}(-1) = 180^o - \angle H_m \end{cases}$$
(41)

Copyright © 2017 John Wiley & Sons, Ltd.



Figure 6. Frequency responses estimated from the switched model (dots), Bode plots obtained from the averaged model (dashes) and the discrete-time (solid) model of the buck converter before and after subharmonic oscillation takes place. Left: $H_m = 0.5$ before subharmonic oscillations develop, from both the small-signal discrete-time and the averaged models the gain and the phase margin are both positive. Right: $H_m = 0.54$ after subharmonic oscillations develop, from the averaged model, the system is stable and both the gain margin and the phase margin are positive. From the small signal discrete-time model, the gain margin $(g_m = -0.44 \text{ dB})$ is negative and phase margin φ_m is infinite. The discrepancies between the models increases in the vicinity of the Nyquist frequency $f_s/2$.

This will only occur at a crossover frequency $\omega_c = \pi/T = \omega_s/2$. Fig. 6 shows the Bode plot from the averaged (dashed) and the discrete-time (solid) models of the system before and just after subharmonic oscillation takes place. The frequency response estimated using numerical simulations from the switched model is also shown (dots).

While the plot obtained from the averaged model predicts always a stable system, the Bode plot from the discrete-time model and estimated from the switched model predict that the system has a negative gain margin after period doubling takes palace. This instability is in agreement with the root-locus analysis presented in the previous section and confirmed by the waveforms of the system obtained from the switched model and depicted in Fig. 7.

A careful examination of the different Bode plots close to one half the switching frequency reveals that:

- The crossover frequency predicted by the averaged model is smaller than the one predicted by the discrete-time model and estimated from the switched model.
- At the Nyquist frequency $f = f_s/2$, the maximum discrepancy is observed in the phase plot. The phase calculated from the discrete-time model is -180° while the phase predicted from the



Figure 7. Time domain responses from the switched model. Left: $H_m = 0.54$ after subharmonic oscillations develop. Right: $H_m = 0.5$, the system exhibits stable periodic behavior.

averaged model is higher. Close to the Nyquist frequency, the loop gain amplitude from the discrete-time model matches well with the switched model. The subharmonic instability takes place because the loop gain obtained from the discrete-time model has a negative gain margin at half the switching frequency. This is different from the slow time-scale instability that can be detected by the averaged model. When this instability takes place, the crossover frequency is smaller than $f_s/2$ and the phase margin is negative for both the averaged and the discrete-time models. This instability can be easily avoided by selecting the time constant of the PI integrator to be enough larger than the time constant RC [3].

- According to the Bode plot from the averaged model (dashed curve), when the gain is increased, the crossover frequency and the phase margin also increases. Hence, erroneously, the model predicts that the bigger the gain is the more stable the system is. However, according to the Bode plot from the discrete-time model, when the gain is increased the crossover frequency increases but the gain margin decreases and the plot correctly predict the subharmonic oscillation instability.
- According to the Bode plot from the averaged model (dashed curve), when the gain is increased, the crossover frequency and the phase margin also increases. Hence, erroneously, the model predicts that the bigger the gain is the more stable the system is. However, according to the Bode plot from the discrete-time model, when the gain is increased the crossover frequency increases but the gain margin decreases and the plot correctly predict the subharmonic oscillation instability.

• The plotted frequency responses beyond the Nyquist frequency $f_s/2$ has no relevance for both non averaged and averaged models. This is because the corresponding variables cannot change faster than one half the switching converter.

7. Conclusions

Conventional applications of switching converters require loop bandwidths much lower than the switching frequency and the average models works quite well under these circumstances. However, Many emerging switching converters applications are aggressively requiring faster DC-DC converters with the system bandwidth close to the switching frequency. In this case, designing and optimizing the performances is a challenging task. The compensation design typically involves various iterations of the controller using averaging procedures. This is not only time consuming, but is also inaccurate in a switching converter whose bandwidth and stability margin can be affected by many parameters. Determining accurately the performances of switching converters at the fast time-scale is considerably involved and crucial because of the strong switching nonlinearity at the switching time-scale. Except for switching converters under digital control, the existing conventional discrete-time models in the literature are of high level of abstraction and cannot be used for design purposes. In this paper, the basic concepts and methods of discrete-time control-oriented modeling of switching mode power converters with naturally sampled pulse width modulation and integrating feedback loop are presented. The main advantage of the proposed approach is its straightforwardness and accuracy. Moreover, the integral action in the feedback loop is explicitly taken into account without any singularity problem in determining the system steady-state operating point and its z-domain loop gain. The location of the open loop and closed loop poles and zeros and how these are affected by circuit parameters can be easily studied using standard CAD tools. This help to design accurate compensators and reduce inaccuracies at the fast time-scale. The buck converter under voltage mode control was used as an example and its corresponding model was validated against simulation results obtained by the circuitlevel switched model yielding very good agreement. In particular, the loop gain derived here agrees very well with the simulation. Unlike the design using the average model which is independent on the duty cycle in the buck converter, the loop gain depends on this variable and hence care must be taken for the design of the modulator, selection of switching frequency and feedback compensation. In particular, by treating the modulator as a gain depending on the operating point, in the new approach the discretetime model is formulated in such a way that standard control-oriented tools such as Bode diagrams and root-loci can be easily used. The same concepts can also be applied to other switching converter

Copyright © 2017 John Wiley & Sons, Ltd.

topologies and compensation schemes with the only modification that the matrices A_u and B_u will be different. The main difference between the presented approach and the existing methodology in predicting the behavior of the converter at the fast time-scale is that the proposed approach performs the system analysis using the open-loop model, which results in an analysis much similar to control systems techniques rather than nonlinear dynamical system approaches. Some important issues like crossover frequency, gain and phase margins, that are highly useful in control design, can be determined. A systematic computational realization, avoiding the numerical determination of the operating point is also possible for this kind of systems. The method and model presented in this work can help to compensate DC-DC converters more effectively which is especially challenging in switching regulators with a bandwidth close to the switching frequency such as in those under ripplebased voltage mode control strategies that use the output voltage ripple in the fast loop or in high power applications where the switching frequency could be relatively low.

Acknowledgments

This project was funded by the National Plan for Science, Technology and Innovation (MAARIFAH) - King Abdulaziz City for Science and Technology- the Kingdom of Saudi Arabia - award number (12-ENE3049-03). The authors also, acknowledge with thanks Science and Technology Unit, King Abdulaziz University for technical support.

REFERENCES

- 1. Erickson R. W. and Maksimovic D., Fundamentals of power electronics. Lluwer, 2001.
- 2. Kassakian J. G., Schlecht M. F., and Verghese G. C., Principles of Power Electronics. Boston, MA: Addison-Wesley, 1991.
- El Aroudi A., Rodriguez E., Leyva R. and Alarcon E., "A Design-Oriented Combined Approach for Bifurcation Prediction in Switched-Mode Power Converters," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 57, no. 3, pp. 218-222, 2010.
- Cortes J., Lu W. G., Svikovic V., Alou P., Oliver J. A., Cobos J. A., Wisniewski R., "Accurate analysis of subharmonic oscillations of V² and V²I_c controls applied to buck converter," *IEEE Transactions on Power Electronics*, vol. 30, no. 2, pp. 1005-1018, 2015.
- El Aroudi A., "A new approach for accurate prediction of subharmonic oscillation in switching regulators-part I: Mathematical derivations," *IEEE Transactions on Power Electronics*, vol. 32, no. 7, pp. 5651-5651, 2017.
- El Aroudi A., Garcia G., Al Hosani K., Al Syari N., Al-Numay M., "Analytical Multi-Parametric Stability Boundaries of DC-DC Buck Converters Under V¹ Control Concept," *International Journal of Circuit Theory and Applications, early* view, DOI:10.1002/cta.2338, 2017.
- 7. Cheng L., Ki W.-H., Yang F., Mok P. K. T., Jing X., "Predicting Subharmonic Oscillation of Voltage-Mode Switching

Copyright © 2017 John Wiley & Sons, Ltd.

Converters Using a Circuit-Oriented Geometrical Approach," *IEEE Transactions on Circuits and Systems-I: Regular Papers*, vol. 64, no. 3, 2017.

- Y. Zhou, C. K. Tse, S. S. Qiu, and F. C. M. Lau, "Applying resonant parametric perturbation to control chaos in the buck dc/dc converter with phase shift and frequency mismatch considerations," *International Journal on Bifurcation and Chaos*, vol. 13, no. 11, pp. 3459–3471, 2003.
- D. Giaouris, S. Banerjee, B. Zahawi, and V. Pickert, "Control of fast scale bifurcations in power-factor correction converters," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 54, no. 9, pp. 805–809, 2007.
- 10. L. Wei-Guo, Z. Luo-Wei, L. Quan-Ming and W. Jun-Ke, "Non-invasive chaos control of DC-DC converter and its optimization," *International Journal of Circuit Theory and Applications* vol. 39, no. 2, pp. 159-174, 2011.
- E. Rodriguez, E. Alarcón, H. H. C. Iu, and A. E. Aroudi, "A frequency domain approach for controlling fast-scale instabilities in switching power converters," *International Journal on Bifurcation and Chaos*, vol. 25, no. 11, p. 1550141, October 2015.
- Lu, W.-G., Lang, S., Zhou, L., Iu, H. H.-C. and Fernando, T.: 'Improvement of stability and power factor in PCM controlled boost PFC converter with hybrid dynamic compensation', *IEEE Transactions on Circuits and Systems – I*, vol. 62, pp. 320-328, 2015.
- W. G. Lu, S. Lang, A. X. Li, and H. H. C. Iu, "Limit-cycle stable control of current-mode dc-dc converter with zeroperturbation dynamical compensation," *International Journal of Circuit Theory and Applications*, vol. 43, no. 3, pp. 318– 328, 2015.
- W. G. Lu, F. Jing, L. Zhou, H. H. C. Iu, and T. Fernando, "Control of sub-harmonic oscillation in peak current mode buck converter with dynamic resonant perturbation," *International Journal of Circuit Theory and Applications*, vol. 43, no. 10, pp. 1399–1411, 2015.
- A. El Aroudi, K. Mandal, D. Giaouris, and S. Banerjee, "Self-compensation of DC-DC converters under peak current mode control," *Electronics Letters*, vol. 53, no. 5, pp. 345–346, 2017.
- Lehman B. and Bass R. M., "Switching Frequency Dependent Averaged Models for PWM DC-DC Converters," *IEEE Transactionson Power Electronics*, vol. 11, no. 1, pp. 89-98, 1996.
- Giaouris D., Banerjee S., Zahawi B., Pickert V., "Stability analysis of the continuous-conduction-mode buck converter via Filippov's method," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 55, no. 4, pp. 1084-1096, 2008.
- Ridley R. B. A new continuous-time model for current-mode control. *IEEE Transactions on Power Electronics*, vol. 6, no. 2, pp. 271-282, 1991.
- Mandal K., Banerjee S., and Chakraborty C., "A New Algorithm for Small-Signal Analysis of DC-DC Converters," *IEEE Transactions on Industrial Informatics*, vol. 10, no.1, pp. 628-636, 2014.
- 20. Li J. and Lee F. C., "Modeling of V² current-mode control," *IEEE Transactions on Circuits and Systems-I: Regular Papers*, vol. 57, no. 9, pp. 2552-2563, 2010.
- Li J. and Lee F., "New modeling approach and equivalent circuit representation for current-mode control," *IEEE Transactions on Power Electronics*, vol. 25, no. 5, pp. 1218-1230, 2010.
- 22. Yingyi Y., Lee F.C., Mattavelli P., "Analysis and design of average current mode control using a describing-function-based equivalent circuit model," *IEEE Transactions on Power Electronics*, vol. 28, no. 10, pp.4732-4741, 2013.
- Duan Y. and Jin H., "Digital controller design for switchmode power converters," *Fourteenth Annual Applied Power Electronics Conference and Exposition*, APEC '99, Dallas, TX, 1999, vol.2, pp. 967-973, 1999.
- Olalla C., Carrejo C., Leyva R., Alonso C., Estibals B., "Digital QFT robust control of DC-DC current-mode converters," *Electrical Engineering*, vol. 95, pp. 21-31, 2013.
- 25. Ki W.-H., "Analysis of subharmonic oscillation of fixed-frequency current-programming switch mode power converters," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 45, no. 1, pp. 104-108, 1998.
- 26. Fang, C. -C,. and Abed, E. -H., "Sampled-Data Modeling and Analysis of the Power Stage of PWM DC-DC Converters,"

Copyright © 2017 John Wiley & Sons, Ltd.

International Journal of Electronics, vol. 88, No. 3, pp. 347-369, 2001.

- Maksimovic D. and Zane R., "Small-signal discrete-time modeling of digitally controlled DC-DC converters," *Proc. IEEE COMPEL*, Troy, NY, 2006, pp. 231-235.
- Maksimovic D., Zane R., "Small-Signal Discrete-Time Modeling of Digitally Controlled PWM Converters," *IEEE Transactions on Power and Electronics*, vol. 22, no. 6, pp. 2552-2556, 2007.
- 29. Packard D. J., "Discrete modeling and analysis of switching regulators," Ph.D. dissertation, California Institute of Technology, Pasadena, 1976.
- Van den Sype D. M., De Gusseme K., Van den Bossche A. P. M., and Melkebeek J. A., "Small-signal z-domain analysis of digitally controlled converters," *IEEE Transactions on Power Electronics*, vol. 21, no. 2, pp. 470-478, 2006.
- Verghese G. C., Elbuluk M. E., and Kassakian J. G., "A general approach to sampled-data modeling of power electronic circuits," *IEEE Transactions on Power Electronics*, vol. PE-1, no. 1, pp. 76-89, 1986.
- Sira-Ramirez H., Garcia-Esteban M. and Perez-Moreno R., "Design of pulse width modulation controllers for stabilization and tracking in derived DC-to-DC power converters," *International Journal of Control*, vol. 64, no. 2, pp. 301-3018, 2007.
- Kim M.-G, "Proportional-Integral (PI) compensator design of duty-cycle-controlled buck LED driver," *IEEE Transactions* on *Power Electronics*, vol. 30, no. 7, pp. 3852-3859, 2015.
- Min R., Zhang, Tong Q., Zou X., Chen X., and Liu Z., "Multiloop Minimum Switching Cycle Control based on nonaveraged current discrete-time model for buck converter," *IEEE Transactions on Power Electronics*, vol. 32, no. 4, pp. 3143-3153, 2017.
- Fossas E. and Olivar G. "Study of chaos in the buck converter," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 43, no. 1, pp. 13–25, 1996.
- Miladi Y., Feki M. and Derbel N., "Optimal control of a single-phase H-bridge DC-AC inverter," *International Journal of Circuit Theory and Applications*, vol. 44, no. 4, pp. 744-758, 2016.
- Morcillo J., Burbano D., Angulo F, "Adaptive Ramp Technique for controlling chaos and sub-harmonic oscillations in DC-DC power converters," *IEEE Transactions on Power Electronics*, vol. 57, no. 6, pp. 1987-1997, 2016.
- Yfoulis C., Giaouris D., Stergiopoulos F., Ziogou C., Voutetakis S., Papadopoulou S., "Robust constrained stabilization of boost DC-DC converters through bifurcation analysis," *Control Engineering Practice*, vol. 35, pp. 67-82, 2015.
- Rodriguez E., El Aroudi A., Alarcon E., "Chaos in Switching Converters for Power Management: Designing for Prediction and Control", Springer, 2012.
- 40. Ogata K., Discrete-time control systems. Prentice-Hall, Inc. Upper Saddle River, NJ, USA, 1987.
- 41. Oppenheim A. V., Willsky A. S., Hamid N. and Hamid S., "Signals and systems," Pearson Education, 1998.

24