Newcastle University

Power and Compute Codesign for “Little Digital” Electronics

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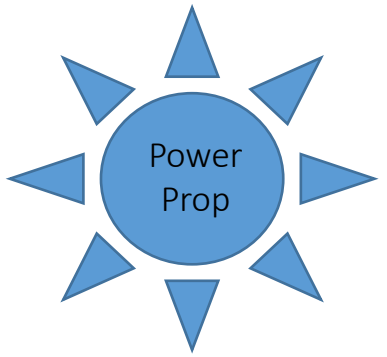
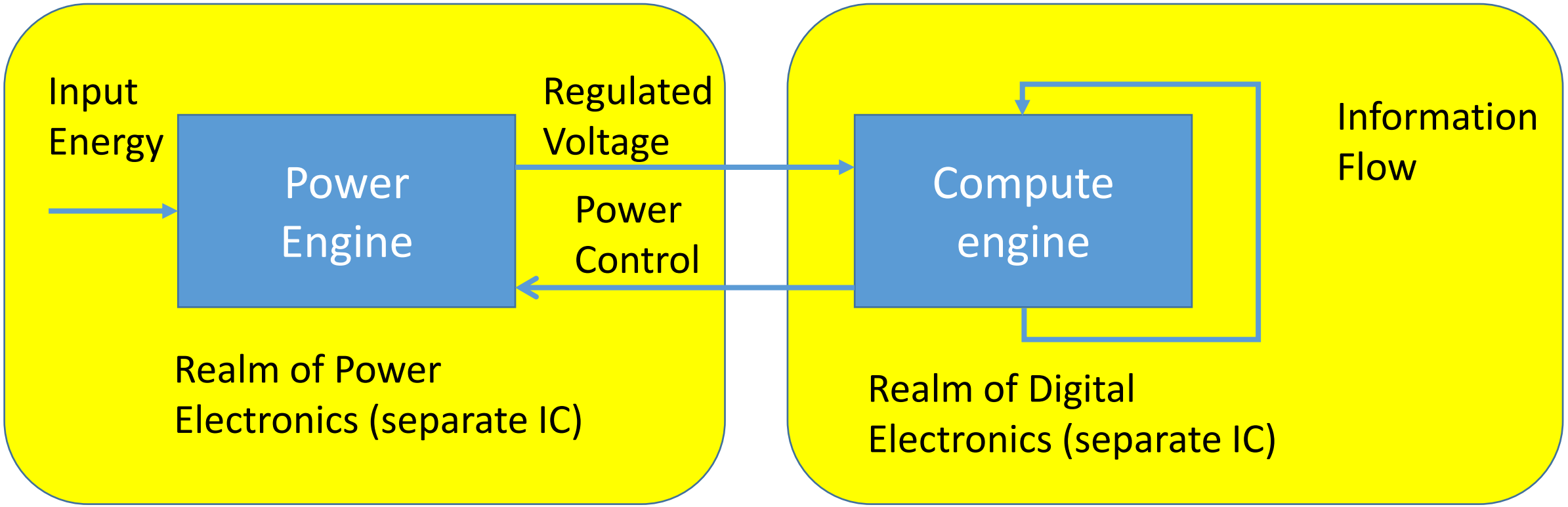


The more you get
The more you give!

ARM Research Summit,
Cambridge
15 September 2016

Traditional Power-Compute Divide



Separate optimization cycles

Miniaturised electronics and ‘real world’ working conditions

Energy-constrained systems

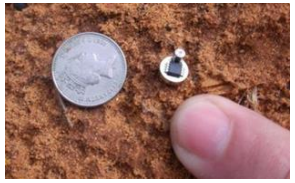
- Solar energy, intermittent supply, small/no batteries, …

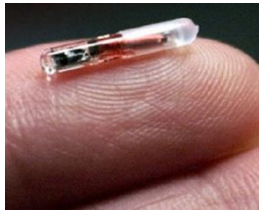
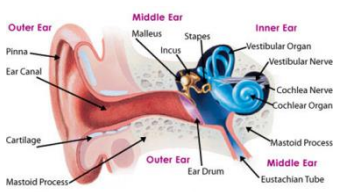
Unreliable power supply

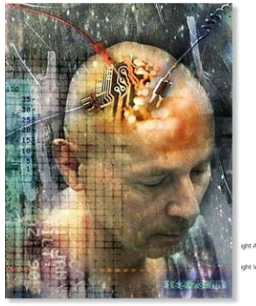
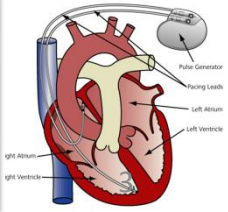
- Voltage fluctuations, low battery, …

Hostile environments

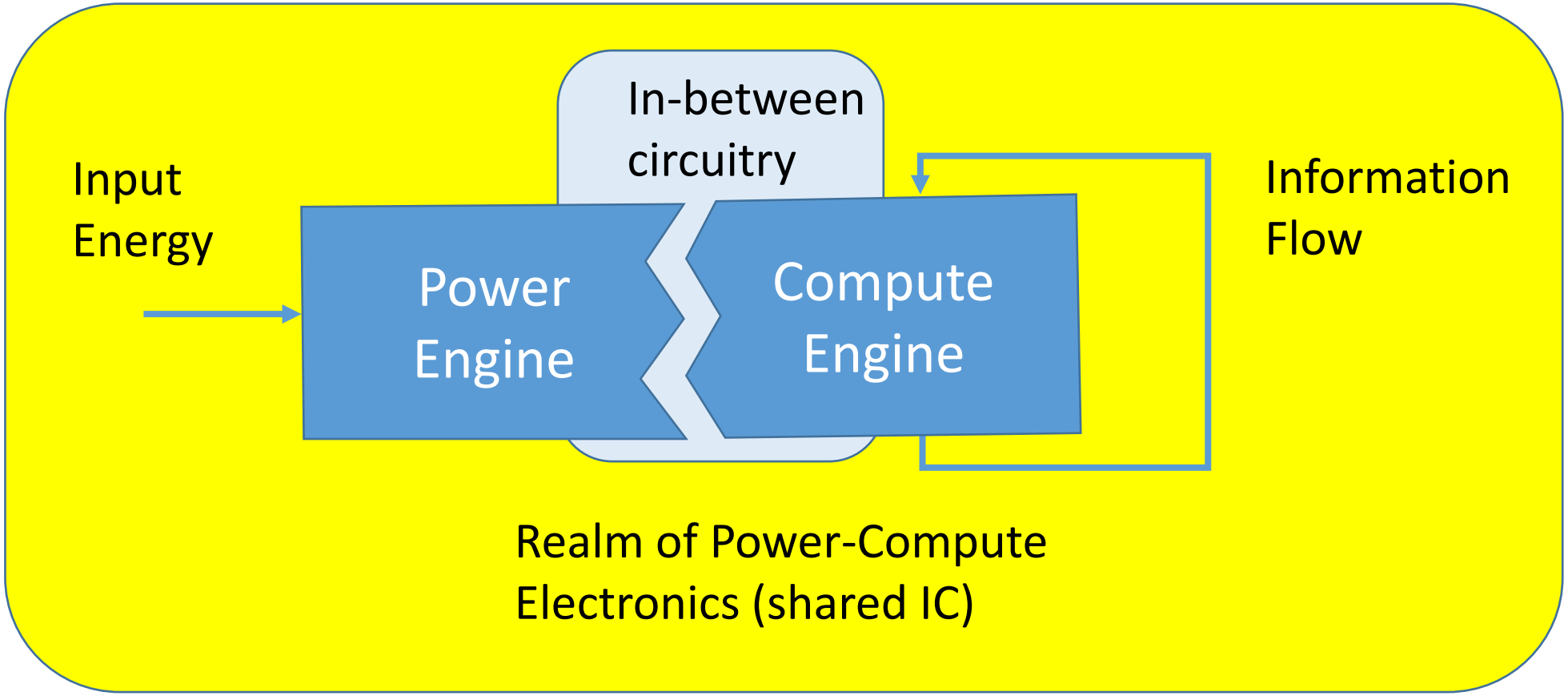
- High/low temperatures, noise, …

Power-Compute Co-design



Co-optimization cycle

Problem definitions:

- For a given silicon area and given data processing functions, find the best way of allocating silicon to power and compute elements
- More specifically, for a given supply rate and given computational demands, which of the following system designs is better:
  1) **Power supply**: capacitor bank (CB) for storing energy and investing energy into charging and discharging flying caps; **Compute**: capable of sustaining high fluctuations of Vcc (e.g. asynchronous logic)
  2) **Power supply**: switched cap converter (SCC) to supply power at stable Vcc; **Compute**: more stable (voltage/timing) processing; extra energy costs: voltage regulator control
- In order to decide between these organisations, one would need to model these designs and characterise them in terms of energy utilisation and delivery of performance for given computation demands
- At present, there are no good ways for co-optimising power and compute!

Power ‘regulation’ for intermittency

Will power and data processing finally converge?

SAVVIE: Staying alive in variable, intermittent, low-power environments

(EPSRC grant, 2013-16, collaboration with Bristol Univ, Dr Bernard Stark)

Capacitors: two operating modes

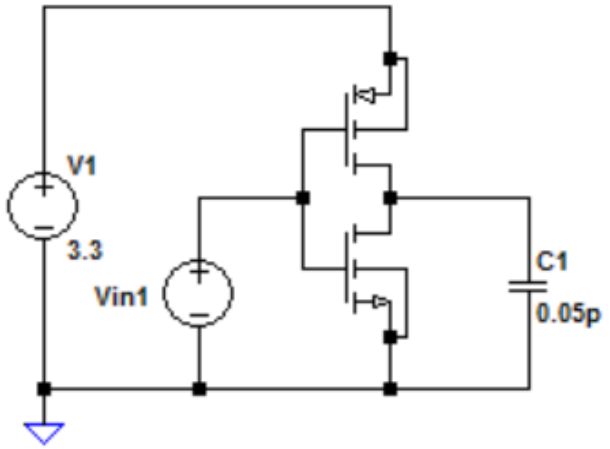
- Complete charge (CC) → information processing
- Almost no charge (NC) → power conversion

TSMC 0.18um

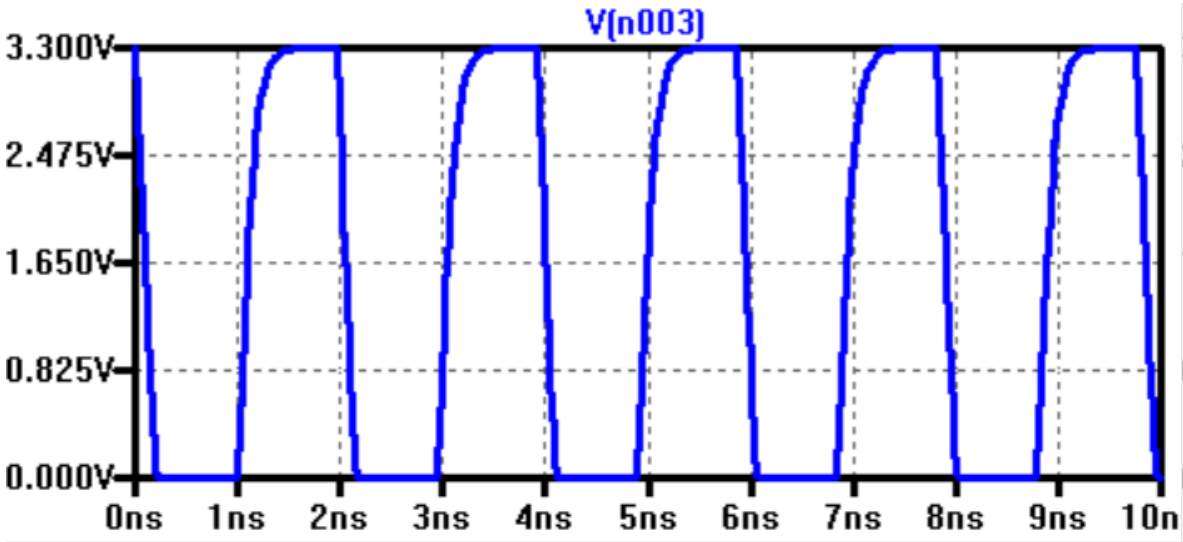
W_n=0.5um, W_p=1.9um

V_{dd}=3.3V

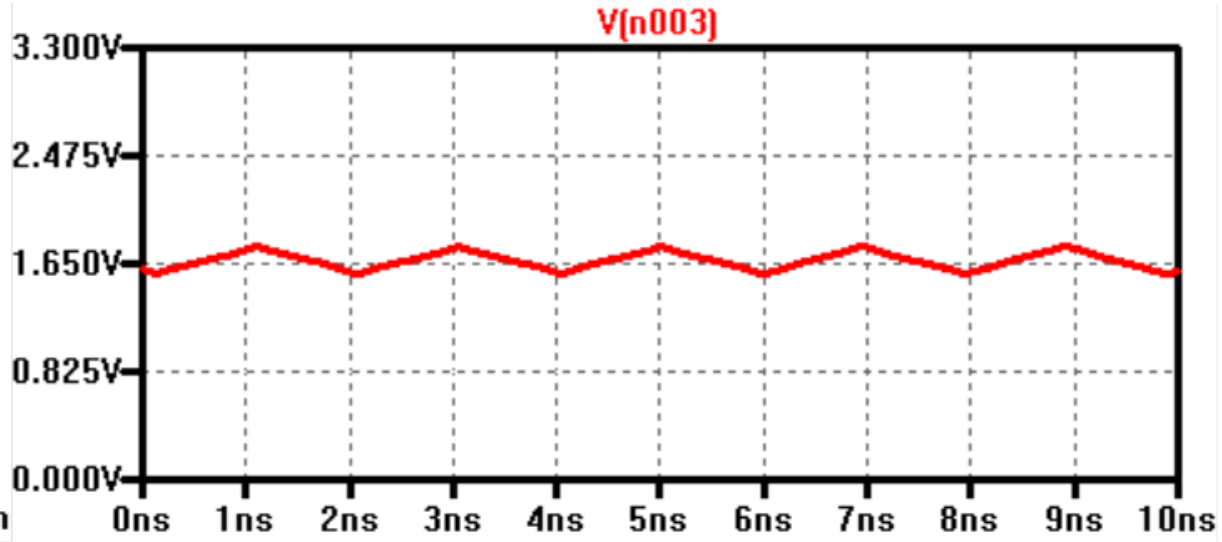
f_{clk}=512MHz



C1=0.05pF



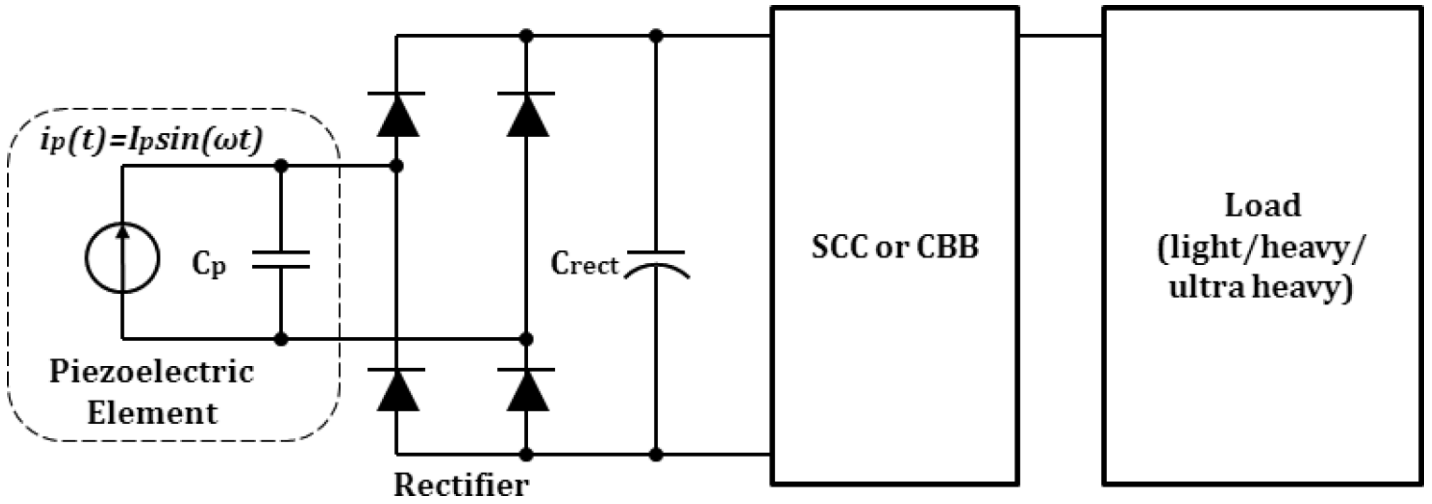
C1=5pF



What if …

- We allow ourselves to work in the intermediate mode:
  - Partial Charge/Discharge of flying caps, but
  - Reduce the amount of switching activity in power control
- We will use self-timed (async) logic for compute engine to cope with variation, and we can also use async for power control

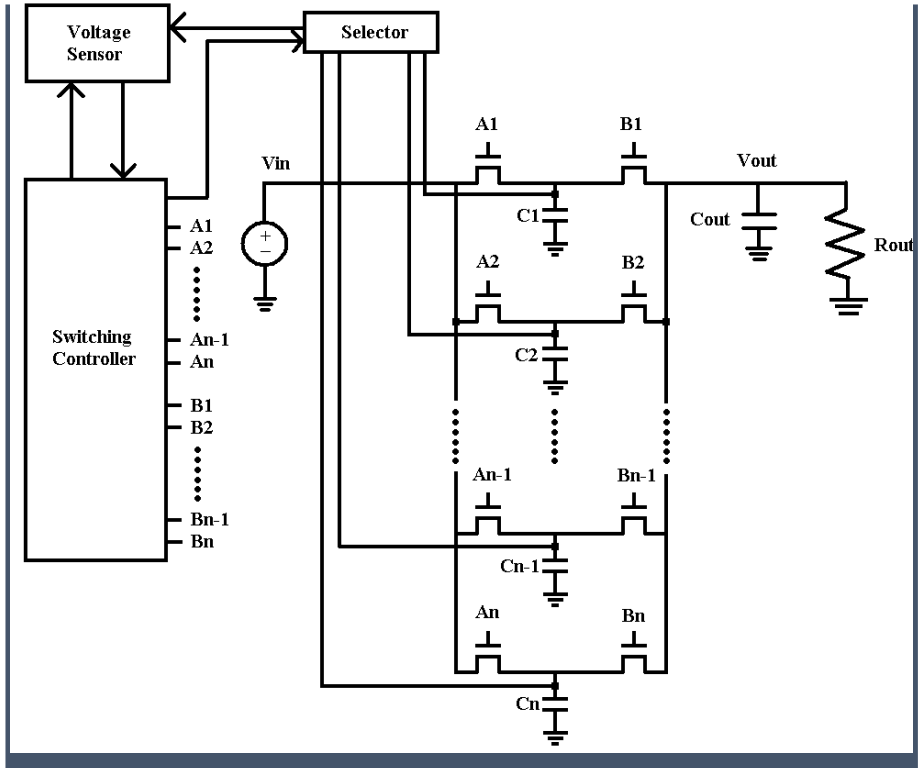
Preliminary study performed for:

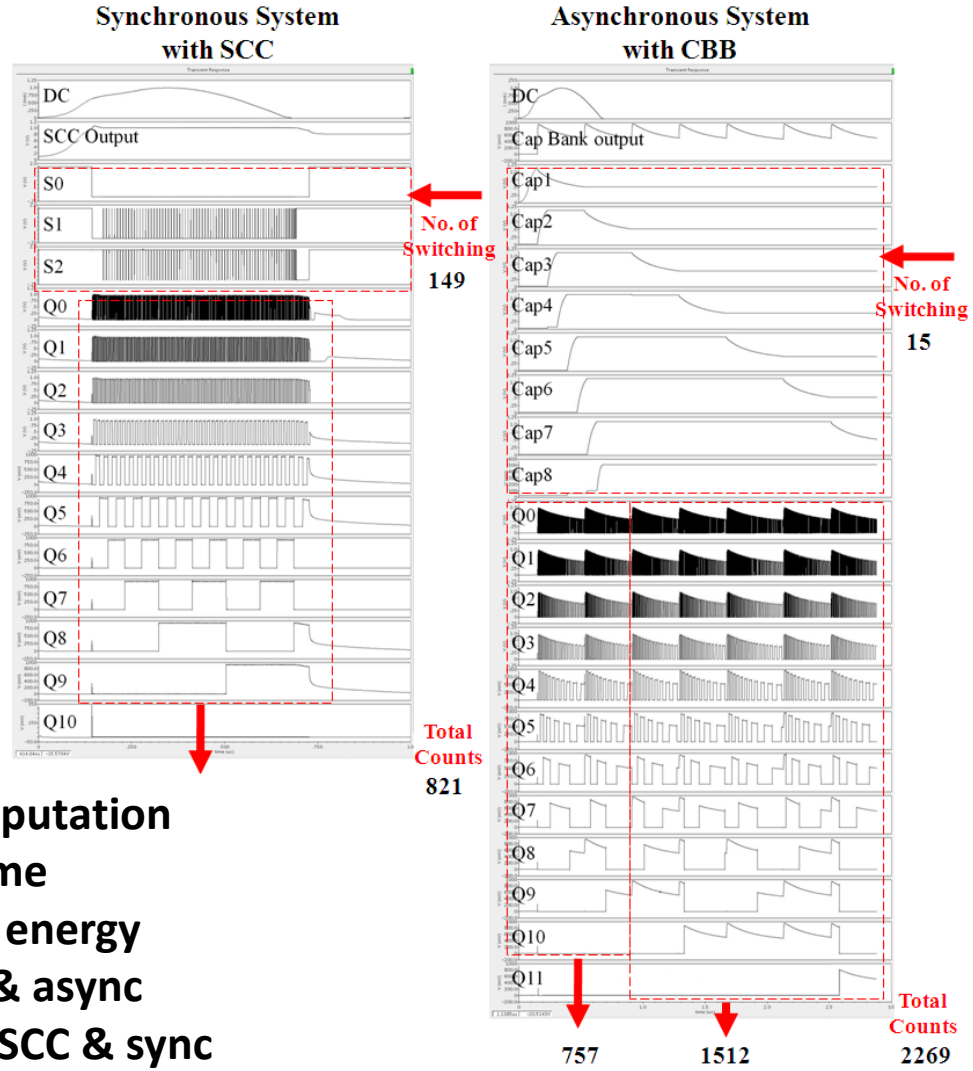


X. Zhang, D. Shang, F. Xia, A. Yakovlev, A Novel Power Delivery Method for Asynchronous Loads in Energy Harvesting Systems, ACM JETC, vol. 7, no. 4, pp. 16.1-16.22 (Dec. 2011).

Switch Cap Converter vs Cap Bank

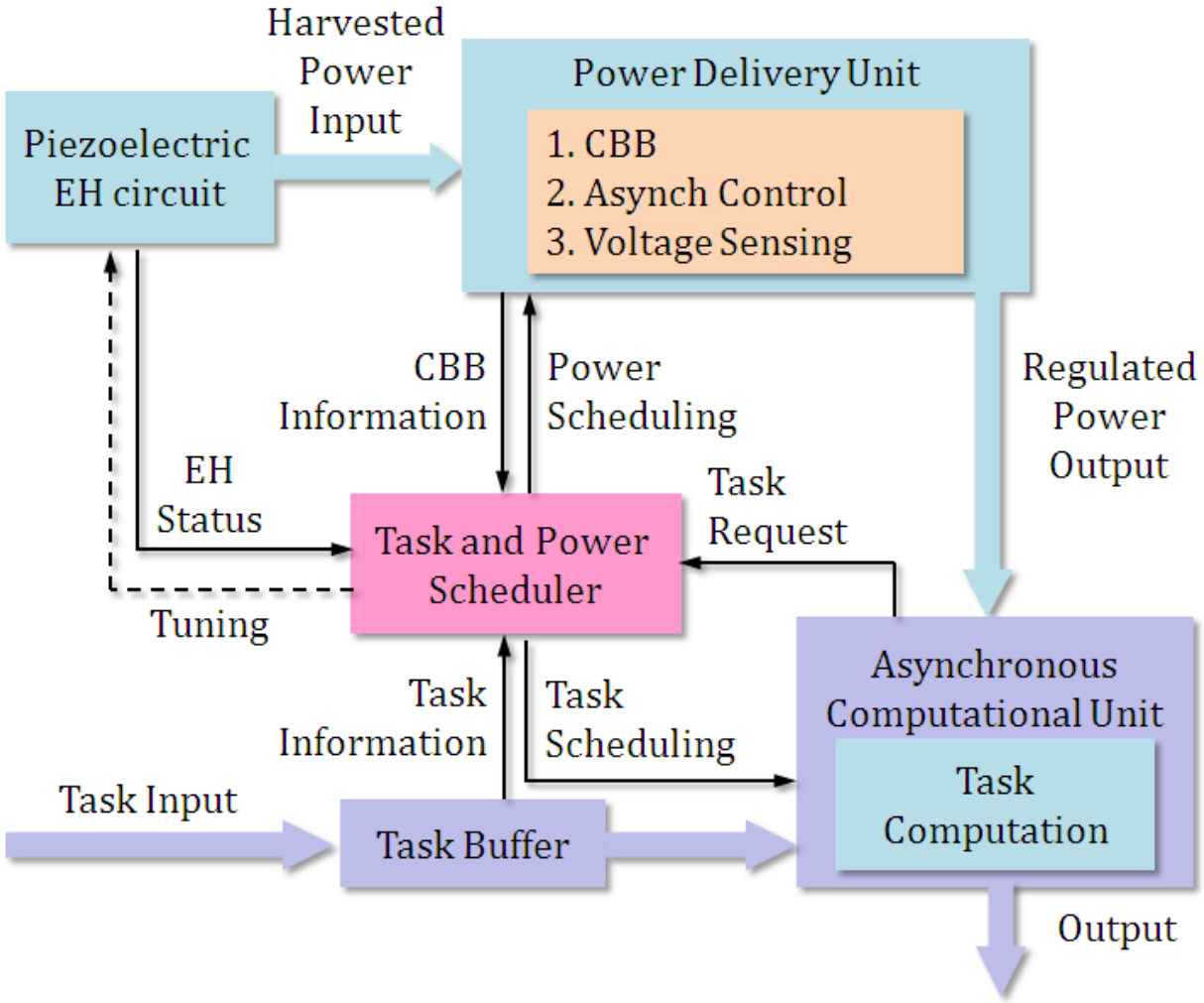
Power control based on capacitor bank blocks (CBBs) instead of DC-DC based on switched capacitor converter (SCC)





More computation for the same harvested energy with CBB & async load than SCC & sync load

Holistic View on Energy Harvesting Powered System



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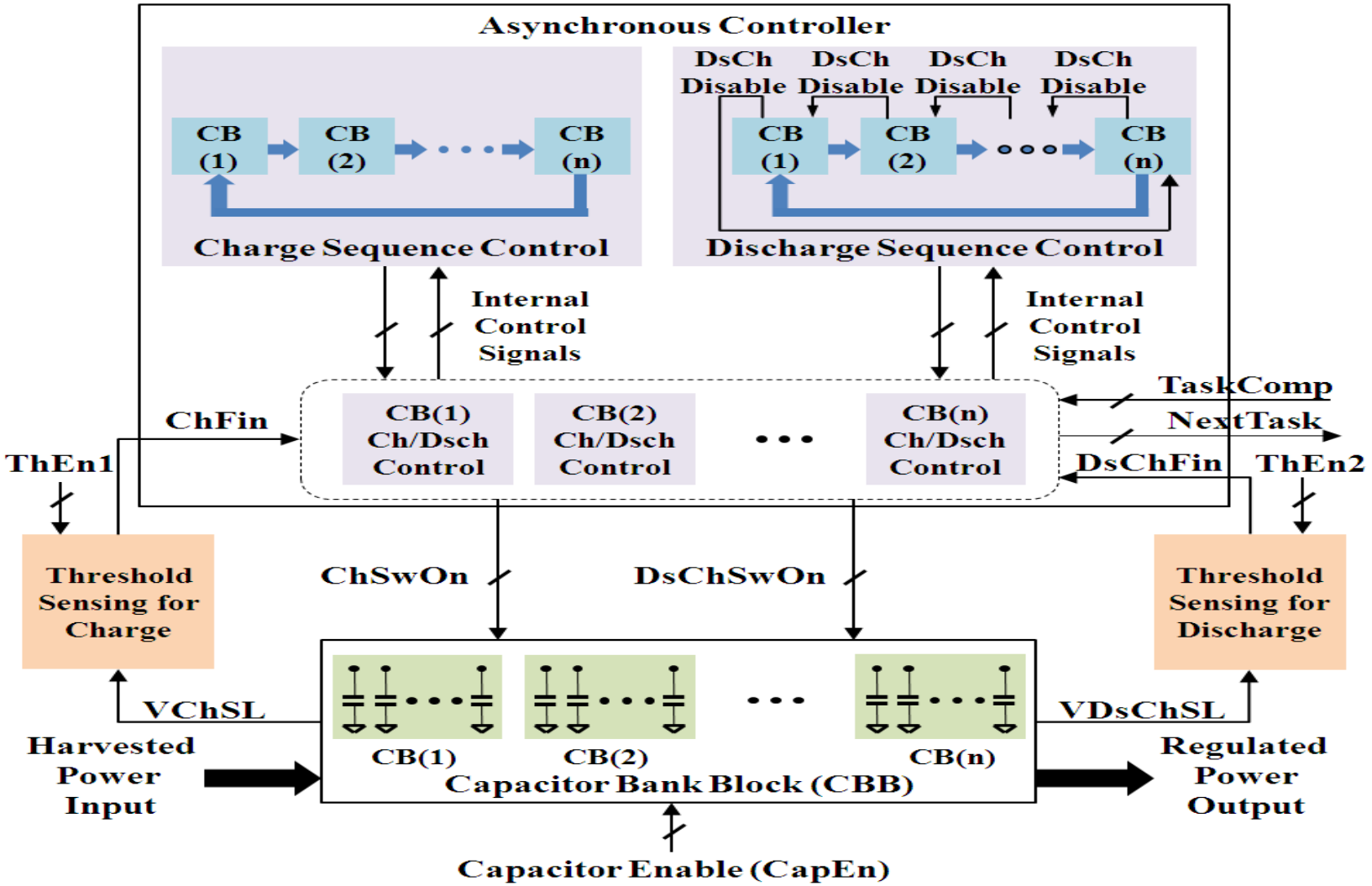
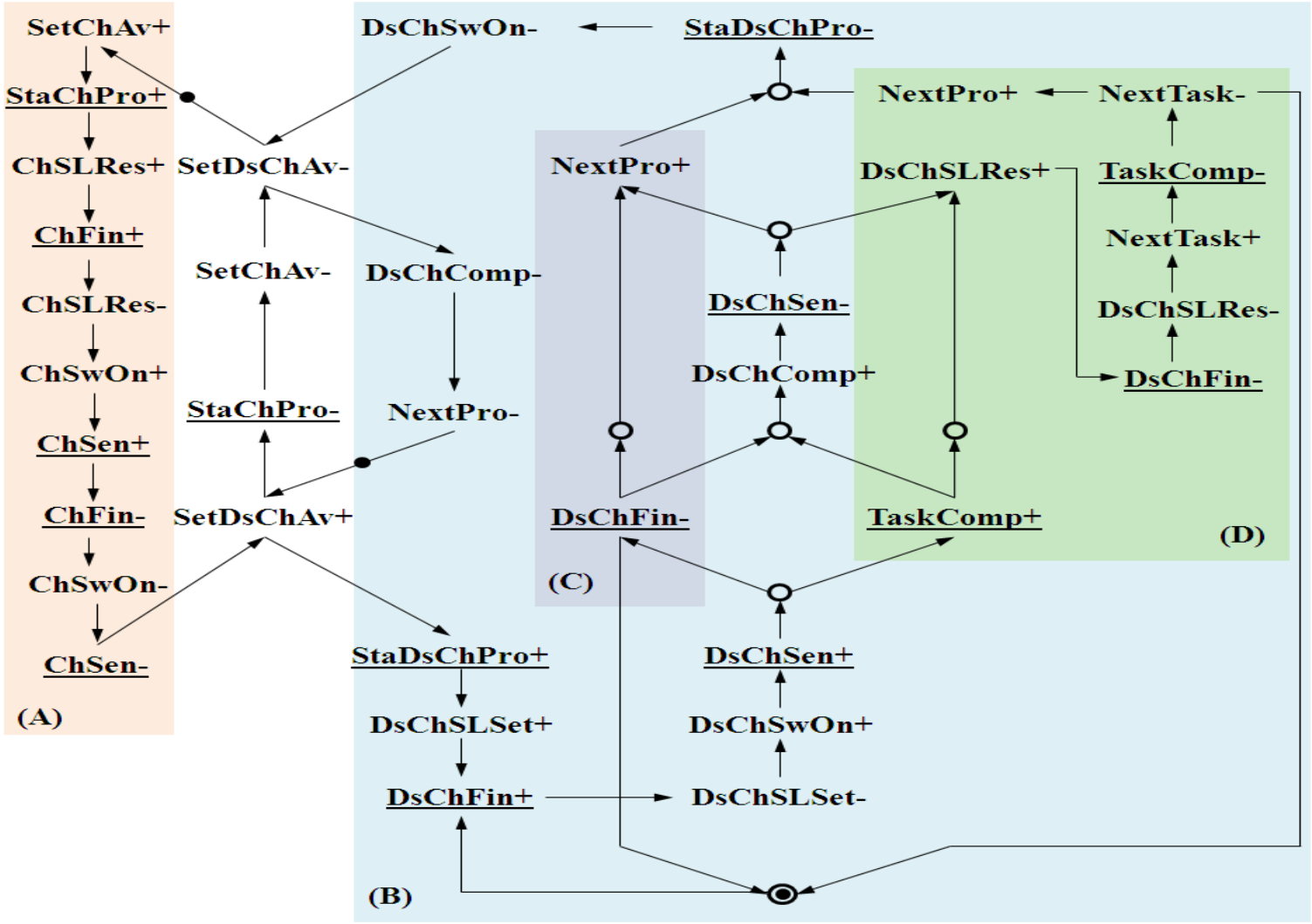
Asynchronous Control For Cap Bank



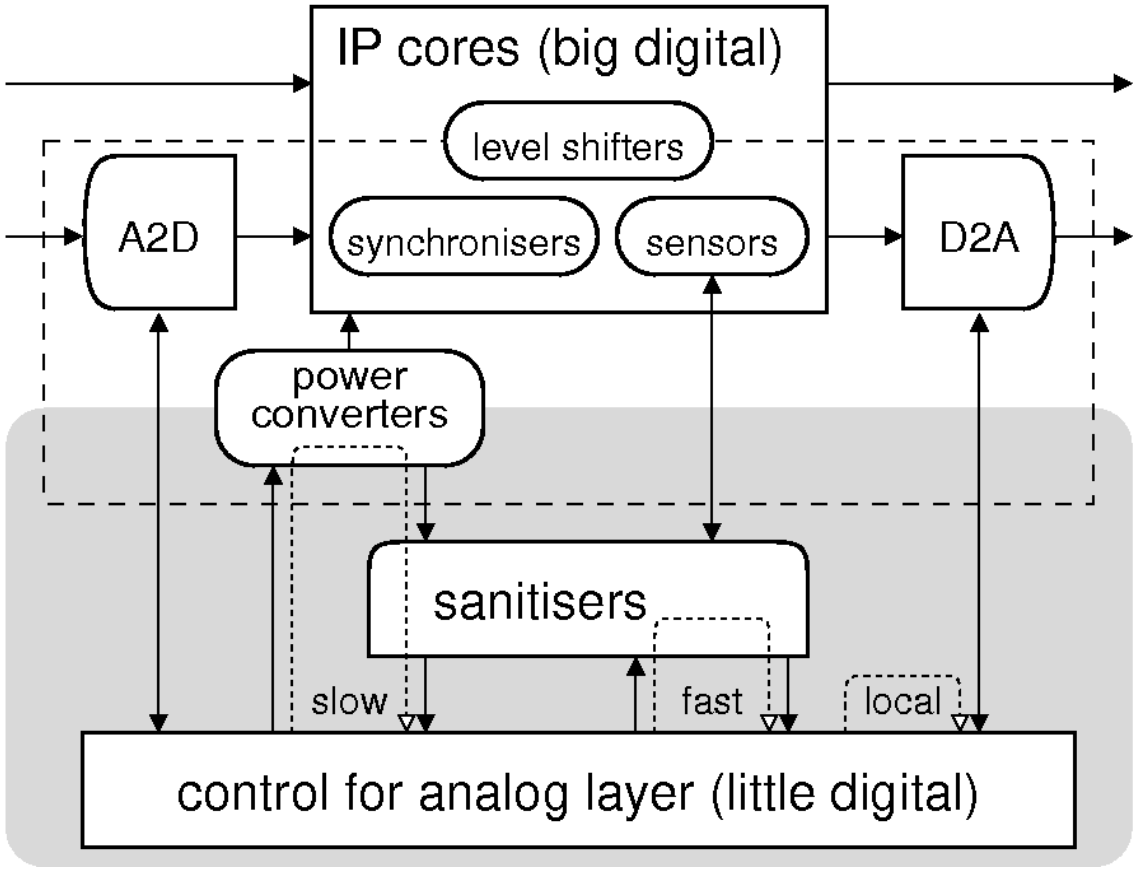
Asynchronous Control Specification (fragment)

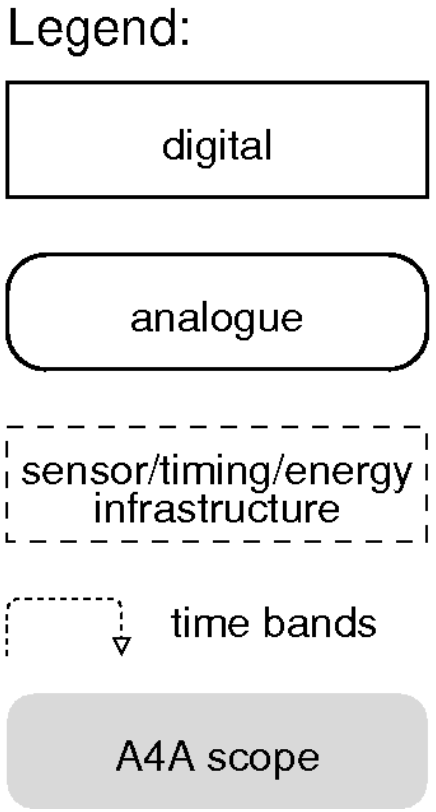


Bigger picture: “Little Digital”

We seem to have layers of digital and analogue electronics; computing-resourcing-controlling …

Emergence of “little digital” and its design





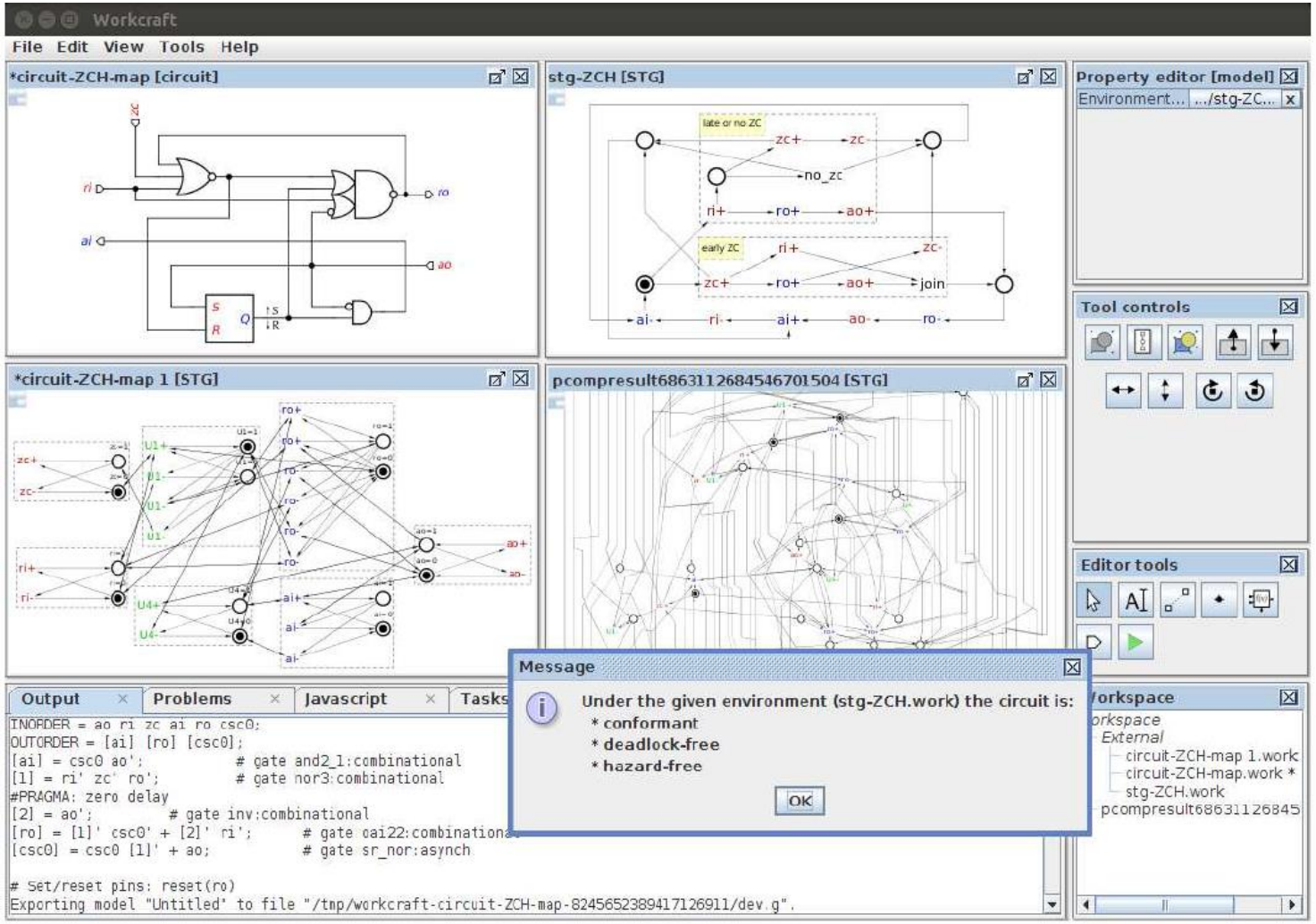
- Analogue and digital electronics are becoming more intertwined
- Analogue domain becomes more complex and itself needs digital control
- Asynchronous design is most likely option for little digital

A4A: Asynchronous for Analogue (EPSRC grant, 2014-17, collaboration with Dialog Semiconductor)

EDA support for “little digital”

- Poor EDA support at present:
  - Mostly supports flow from schematic capture rather than behavioural capture
  - Synthesis from behavioural (RTL) is optimized for data processing logic and supports only synchronous – *OK big digital*
  - *Manual* and *ad hoc* solutions are prone to errors and hard to verify (weeks of simulations)
- Big challenge is EDA for asynchronous (hence our A4A project)
- Next step: codesign of analogue and asynchronous (forthcoming grant application “AxA”) – focus on automated specification generation, synthesis of async for DSM (<=45 nm), formal verification of mixed signal designs, ‘tiered relative timing’ verification

Tool support: Workcraft

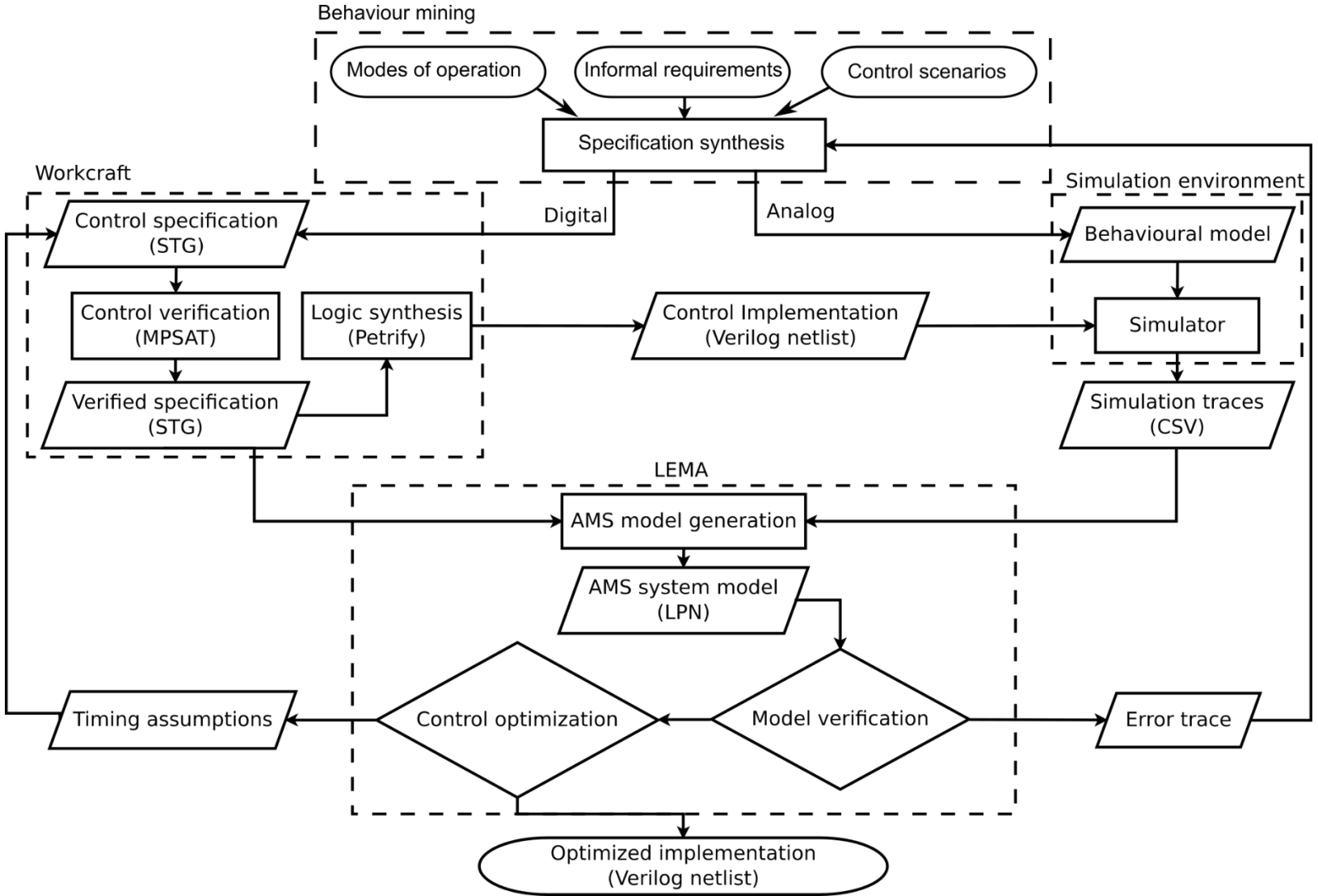


- Framework for interpreted graph models (STGs, Circuits, FSMs, data flow structures, xMAS networks)
  - Interoperability between modes
  - Elaborate GUI
- Includes many backend tools, e.g.
  - Petrify: STG and circuit synthesis
  - MPSAT: unfolding based verifier and synthesizer
- Public domain: workcraft.org
- Documentation, tutorials and exercises available

Vision for the Future

Approaches to designing ‘little digital’ electronics of the future will be based on event-driven, pulse-based, ultra-wide band techniques … appropriate physical and mathematical models will be needed!

Future: Async-Analog (AxA) codesign: possible future flow

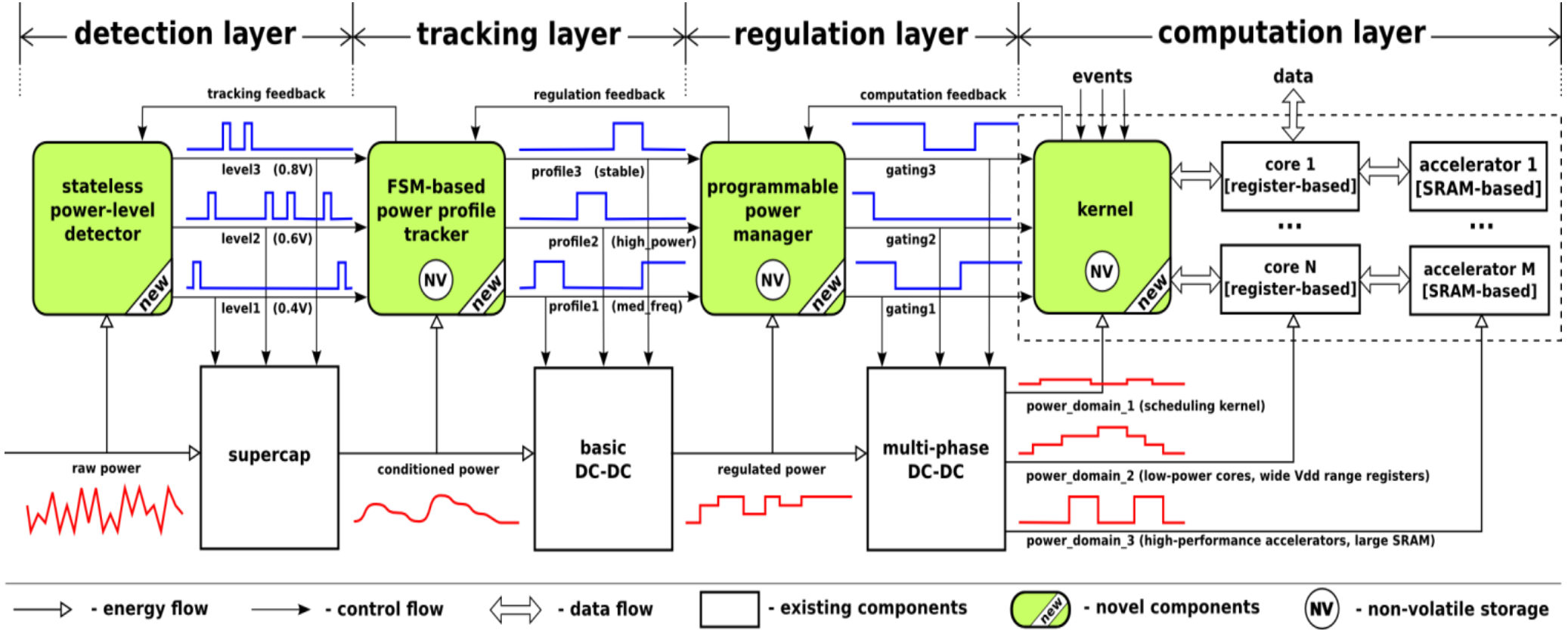


Collaboration with:

- Dialog Semiconductor
- Prof Chris Myers (Uni of Utah) on AMS model generation and LEMA tools
- Prof Jordi Cortadella (UPC, Barcelona) on specification synthesis and Petrify

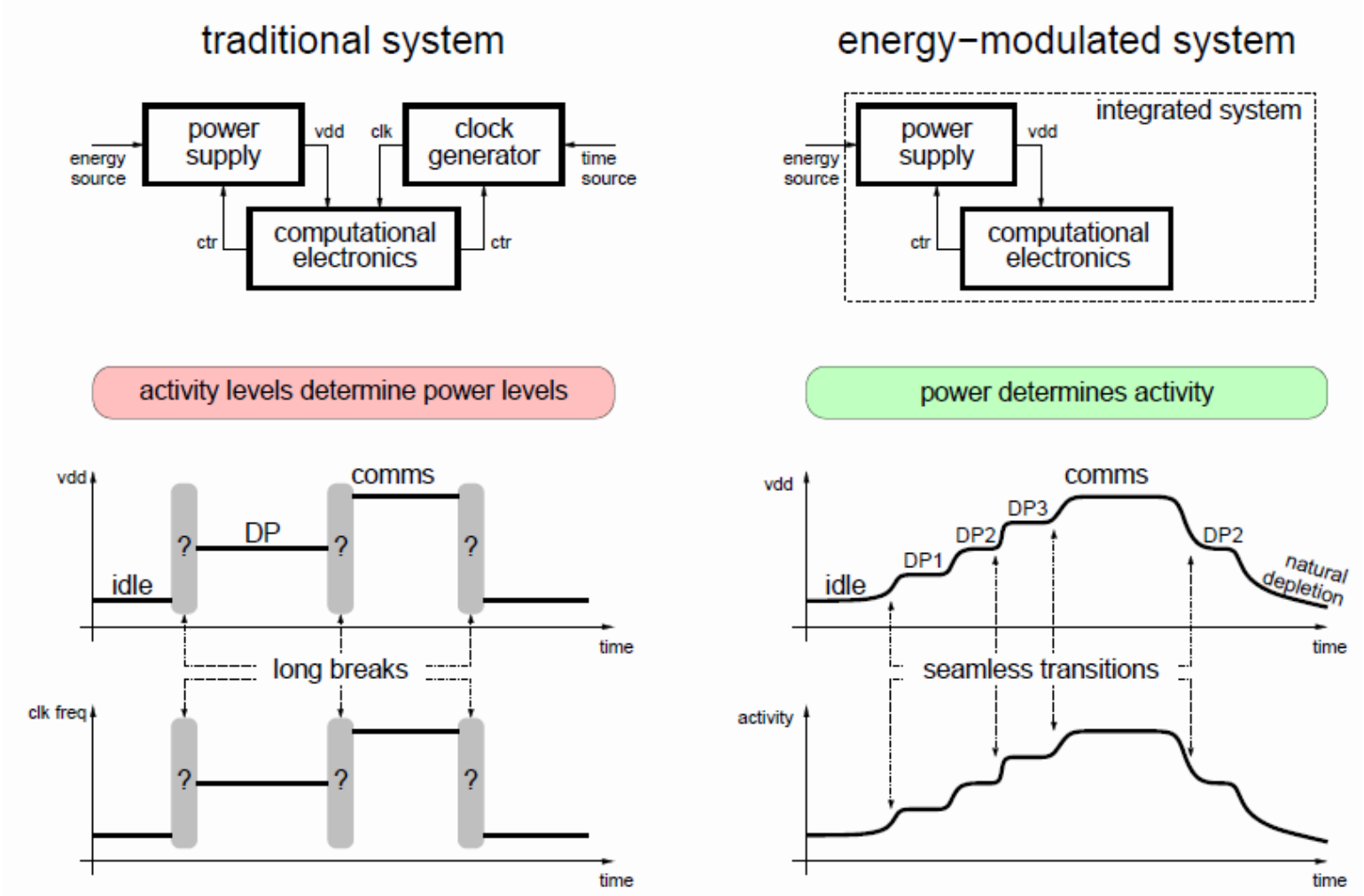
V. Dubikhin; C. J. Myers; A. Yakovlev; D. Sokolov, "Design of Mixed-signal Systems with Asynchronous Control," in IEEE Design & Test, 33 (5), Oct. 2016.

Future: Intermittently powered system: layered approach with non-volatile storage



Backup slides

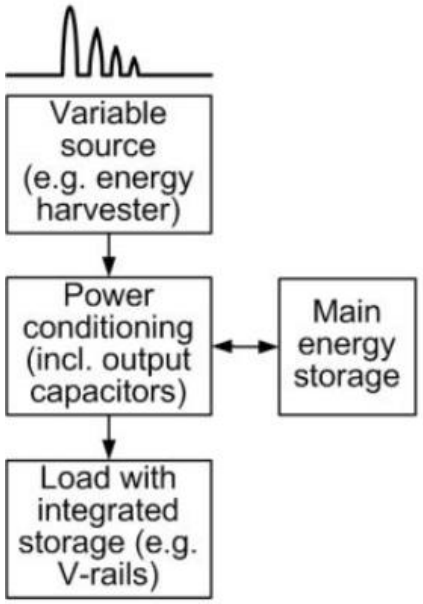
Power-Data Convergence: Energy-modulated computing

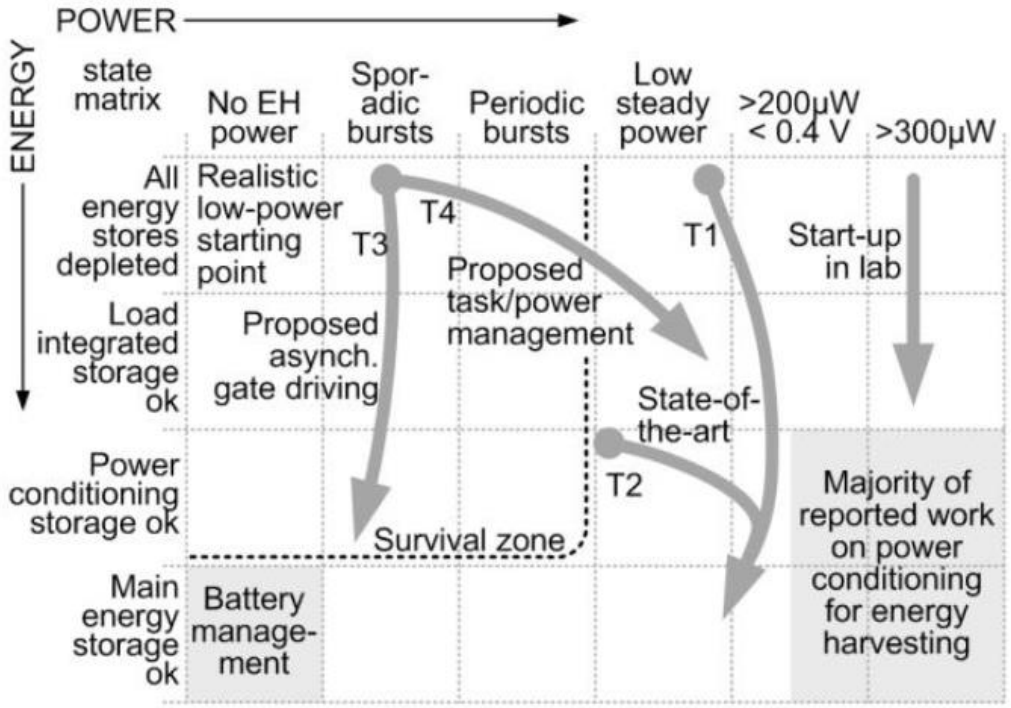


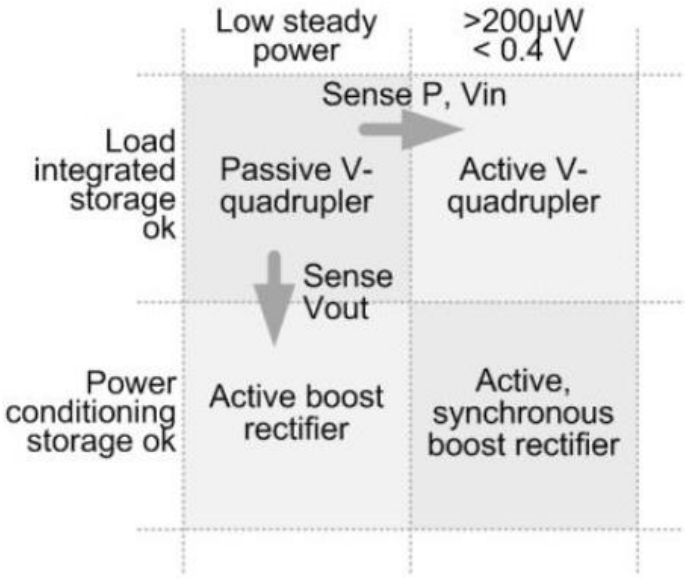
A. Yakovlev: Energy-modulated computing, DATE 2011

SAVVIE Project (EPSRC-funded), Bristol and Newcastle

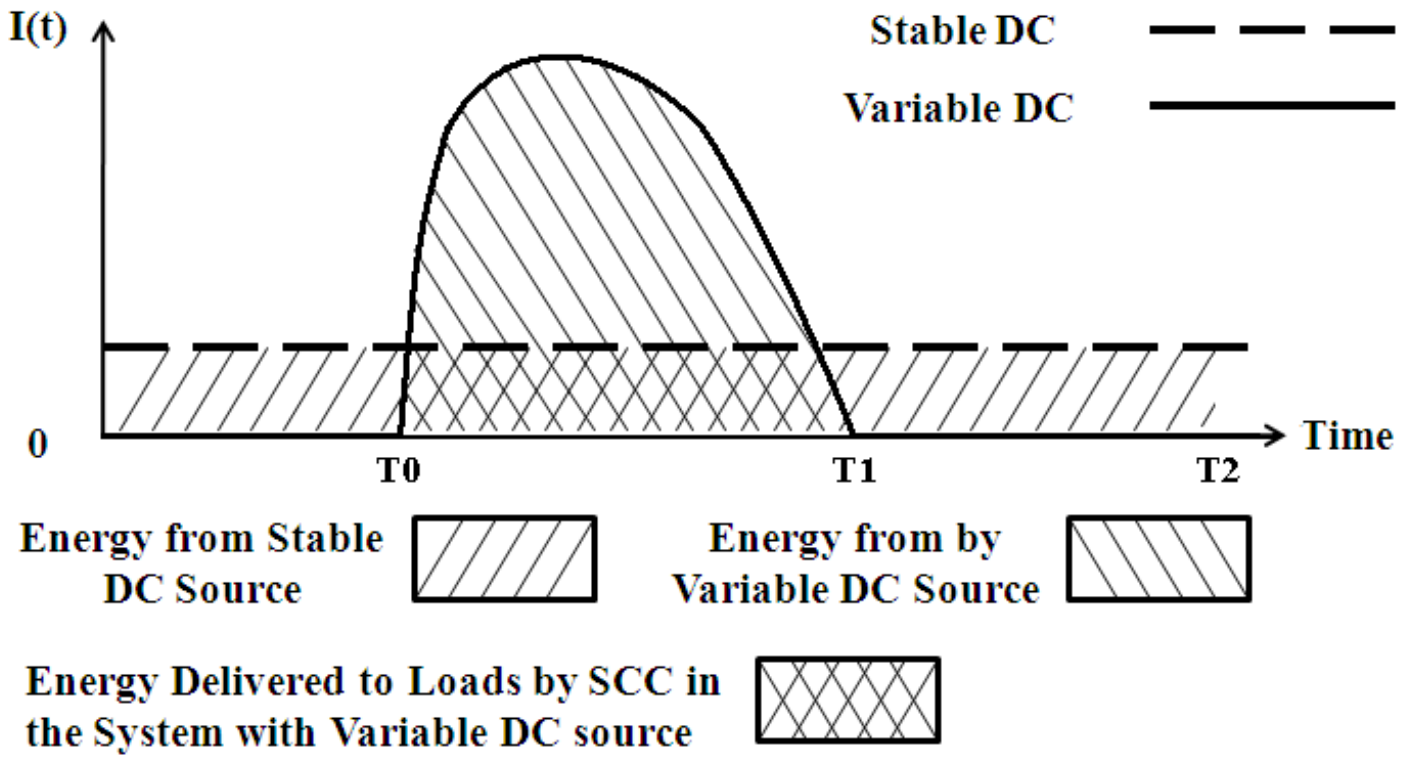
Staying alive in variable, intermittent, low-power environments







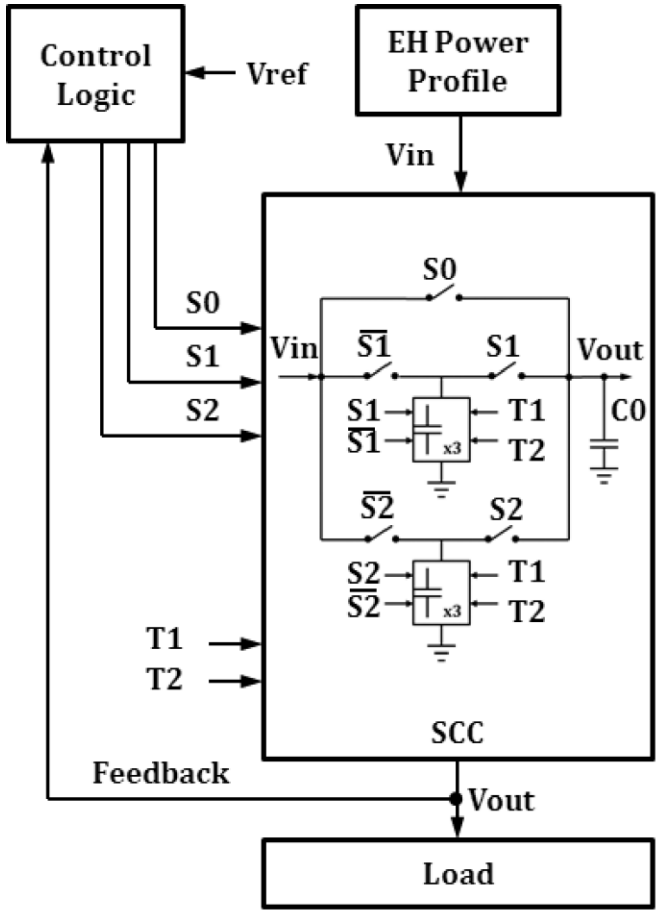
Energy harvesting and power intermittency

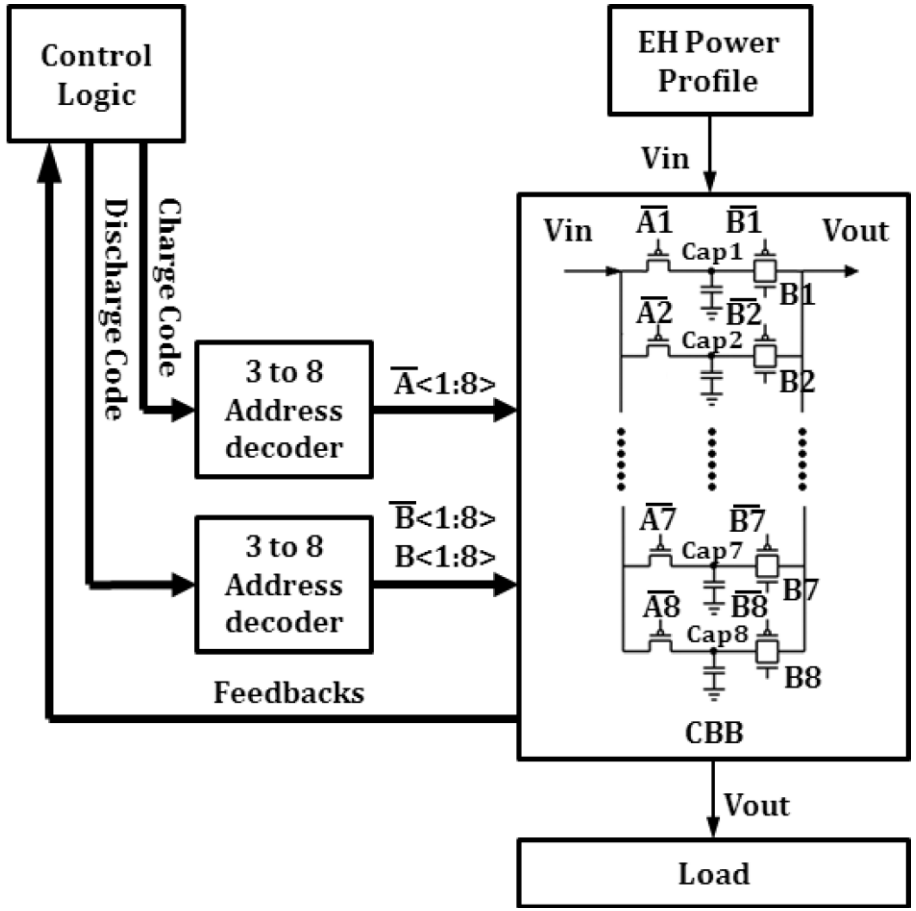


SAVVIE: Staying alive in variable, intermittent, low-power environments

(EPSRC grant, 2013-16, collaboration with Bristol Univ, Dr Bernard Stark)

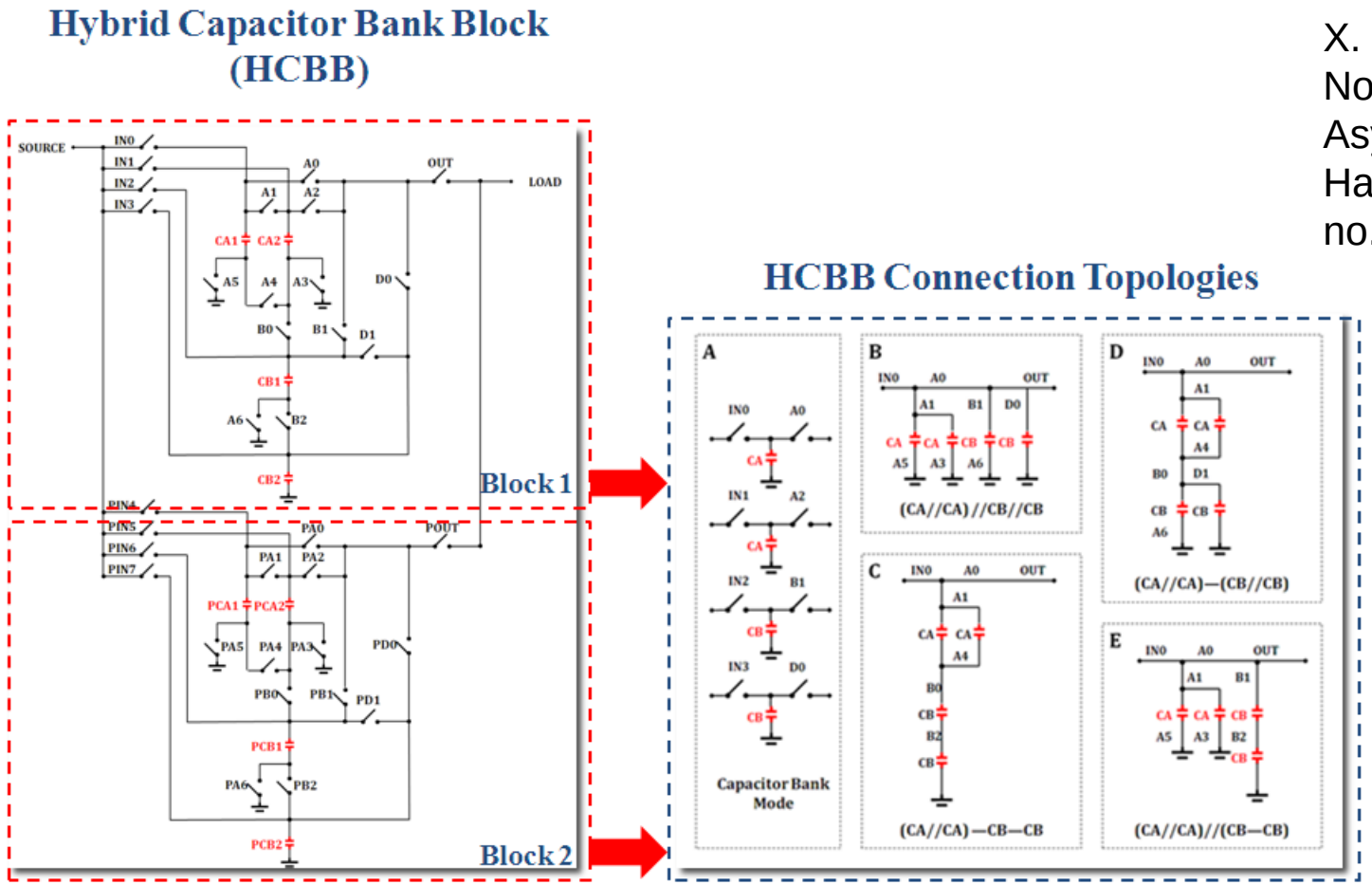
Switch Cap Converter vs Cap Bank Block





Switched capacitor power delivery

- HCBB design can be dynamically configured to work in CBB or SCC mode



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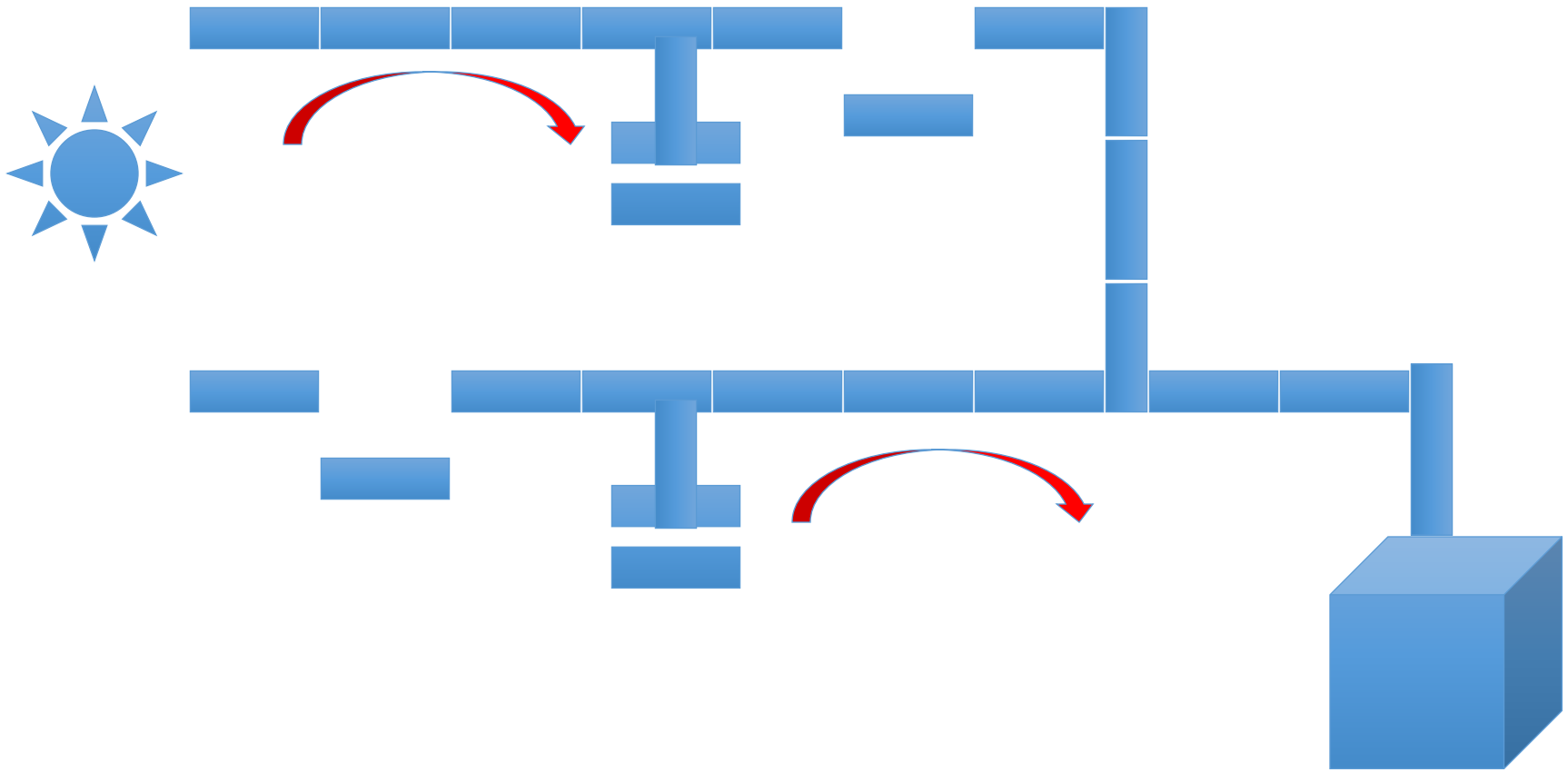
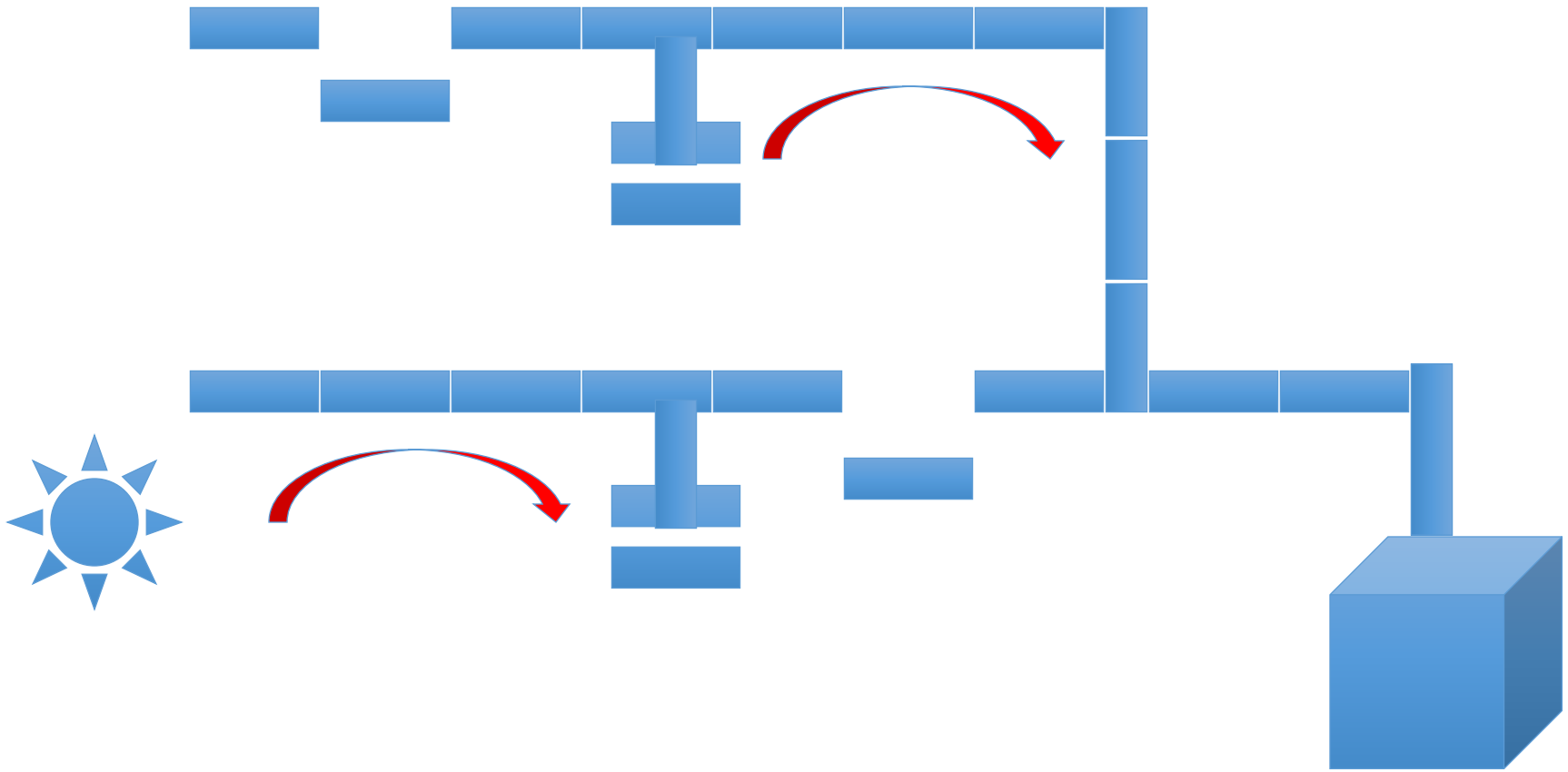
The principle of Capacitor Bank Block

In Principle

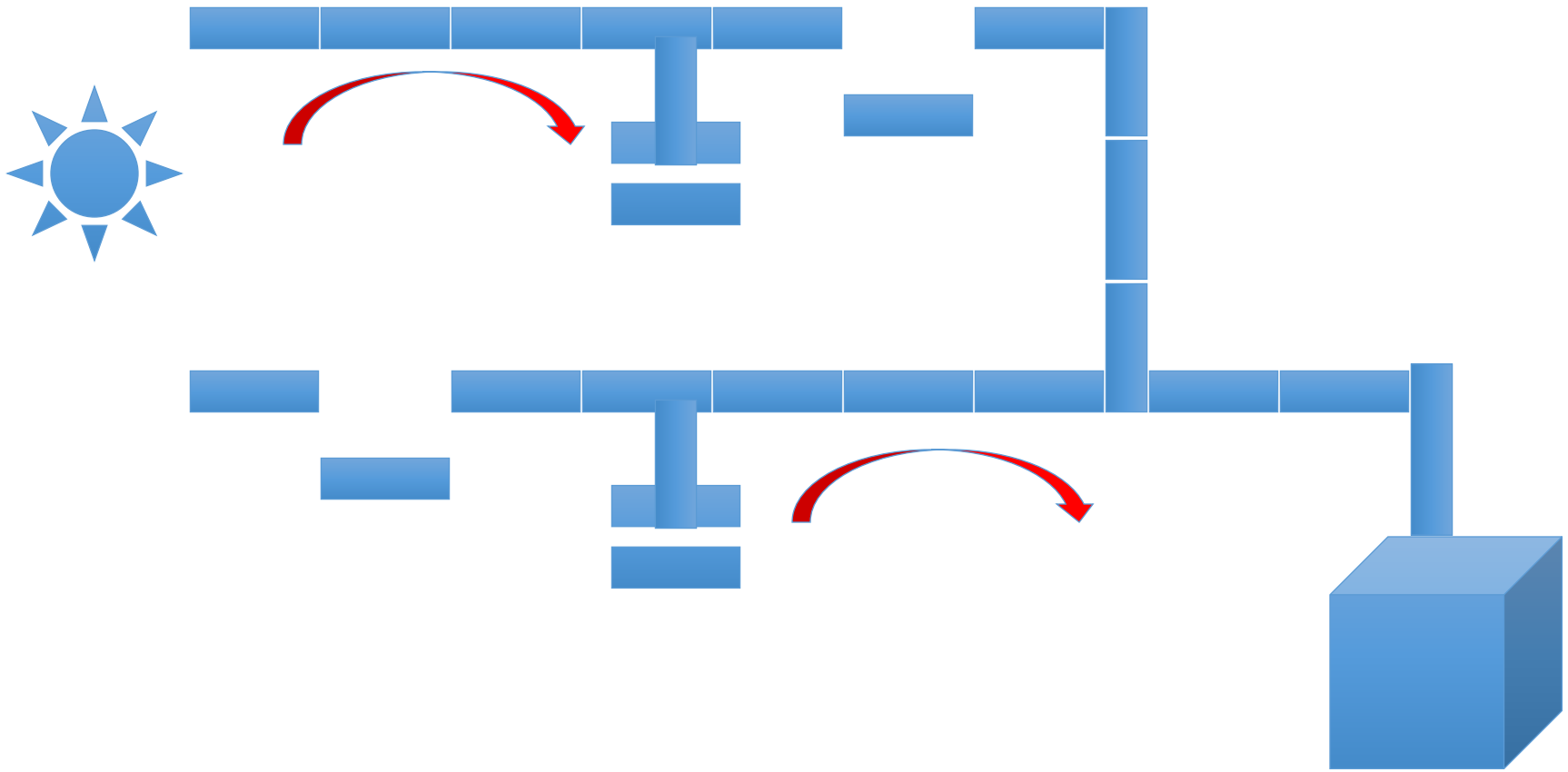
CBB Working Mechanism



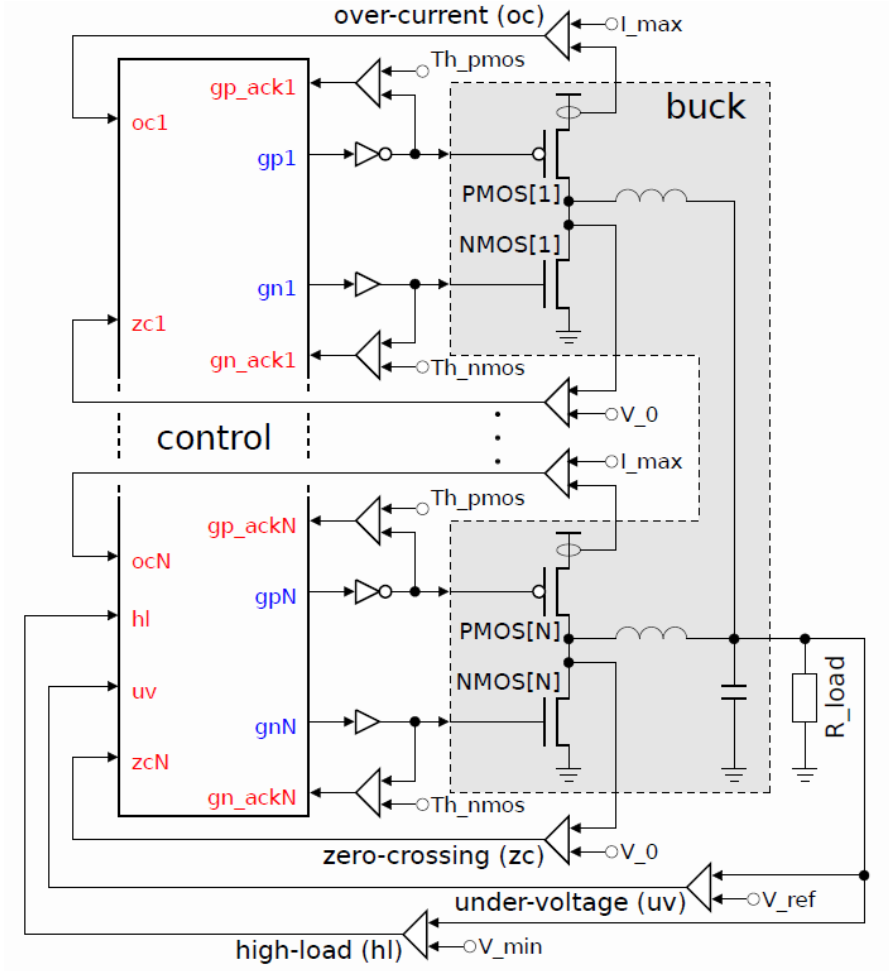
CBB Working Mechanism



CBB Working Mechanism

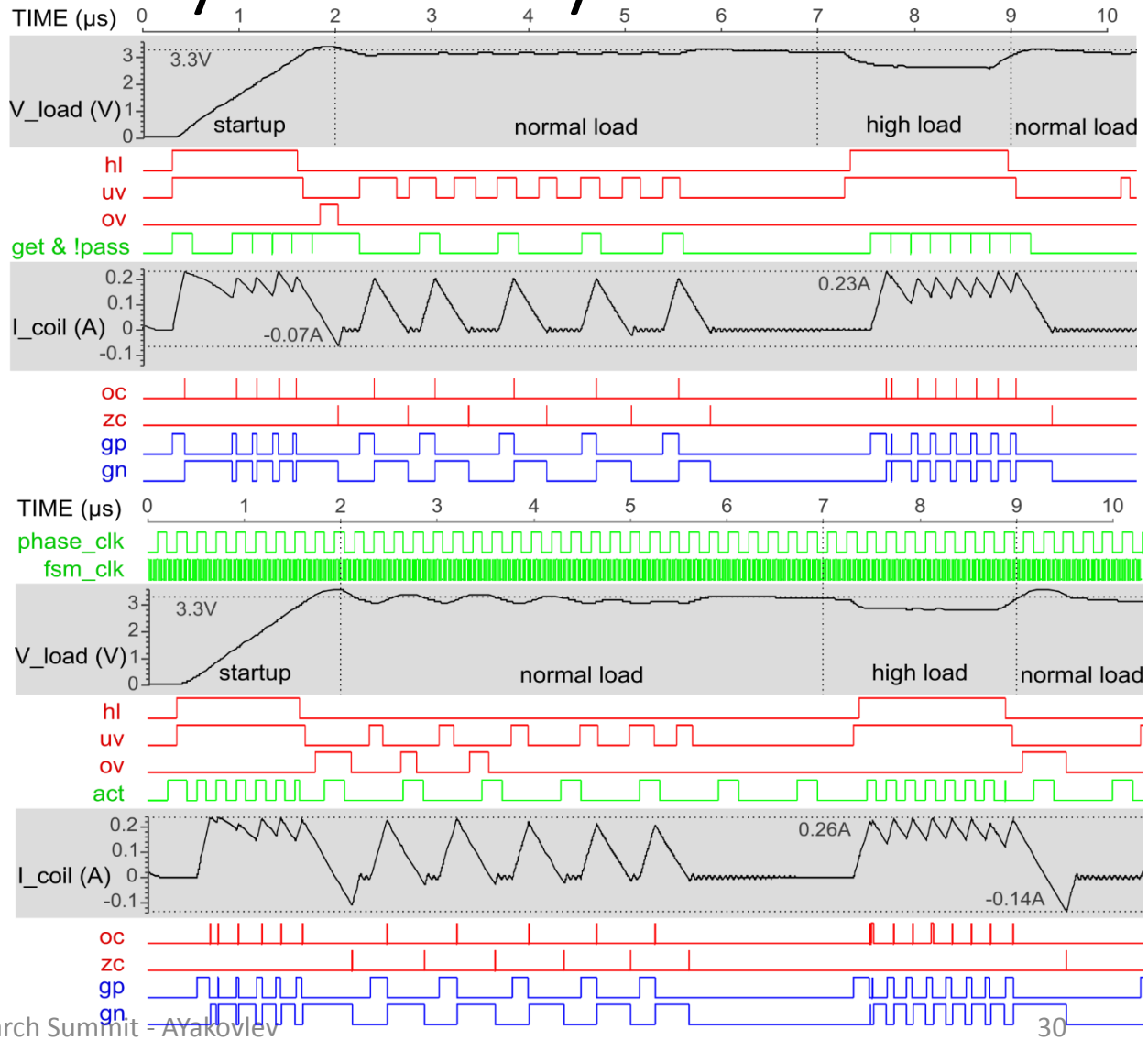


Example of buck DC-DC: sync vs async



Async

Sync



Holistic comparison: Async buck vs Sync buck

- Significantly lower switching activity (no high-frequency sampling clock);
- Faster reaction to changes in sensor readings, which leads to:
  - Lower current ripple (240mA vs 400mA @ 4.7uH)
    -- this can be traded off for coil size (e.g. async can achieve 300mA peak-to-peak current with 1.8uH coil while sync needs 6.8uH);
  - Smaller voltage overshoot;
  - Shorter resolution time for OV and UV conditions;
- Smaller losses and higher efficiency (10% on).