Stacked Asynchronous Circuits

or

Elements of Circuit Theory involving digital circuits as impedances

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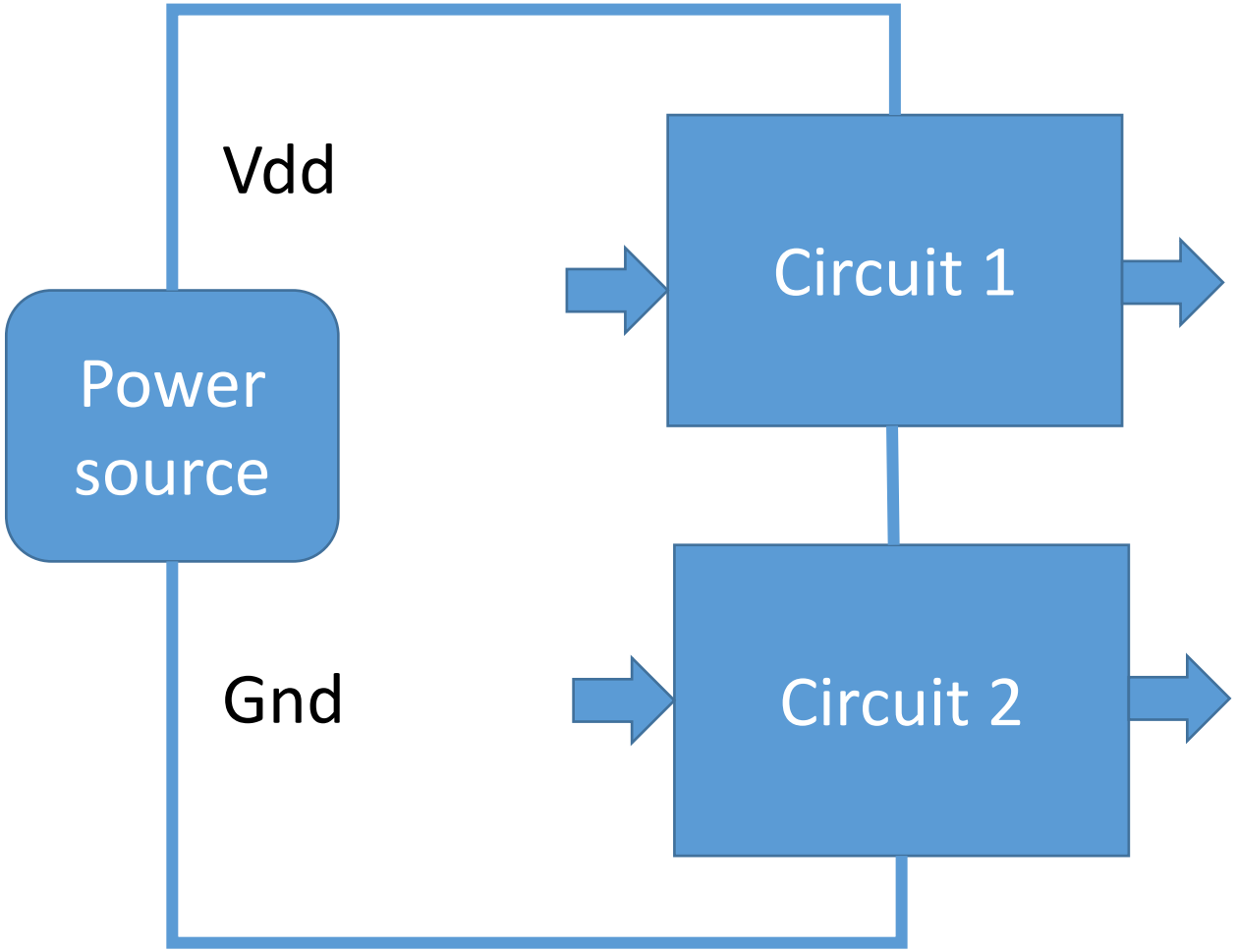
Stacking asynchronous circuits:



Why would we want to stack them?

- One possible motivation is to gain power efficiency, because: Power ~ Vdd^2, while speed ~ 1/Vdd
- The other motivation is purely theoretical, to see what kind of behaviour we can have for different power sources
- Basically what sort of impedances are asynchronous circuits?!

Related work

- Some work on stacking QDI circuits was reported at University of Arkansas:

  Suchanek, Andrew Lloyd, "Asynchronous Circuit Stacking for Simplified Power Management" (2018). Theses and Dissertations. 2805. Supervisor: Prof Jia Di.

  https://www.flintbox.com/public/project/57790/

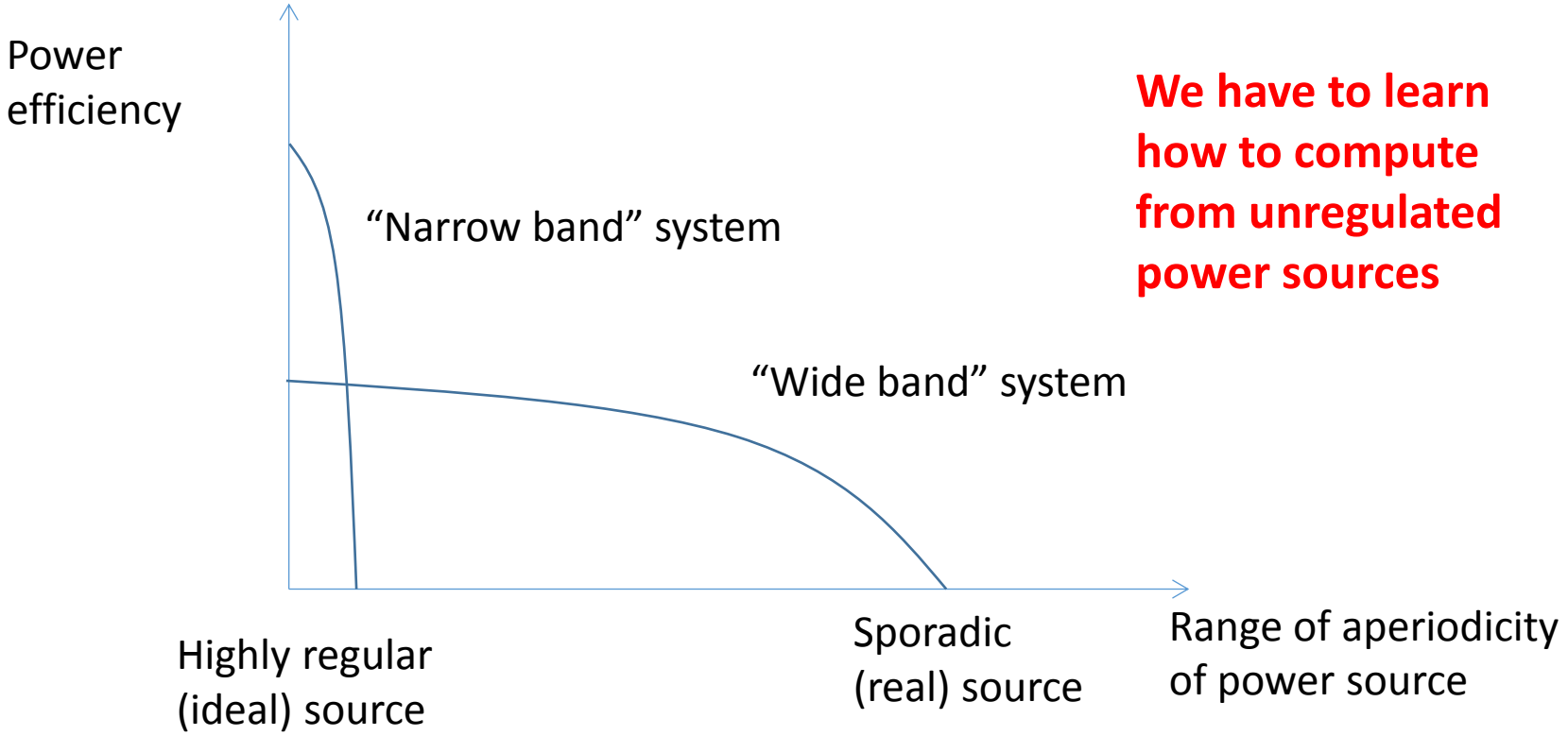
- In our work we mainly focus on VCO (inverter rings), which offer interesting applications by themselves.
- And we came across stacking from a “side view” ….

Outline

- **Example: Reference-free voltage sensor**
- **Understanding computational loads**
- **Asynchronous circuits as voltage controlled oscillators (VCO)**
- **Discharging a capacitor via a VCO – VCO as a switched capacitor circuit!**
- **Stacking VCOs for capacitor discharge: theory and experiments**
- **Stacking VCOs for DC voltage sources**
- **Applications:**
  - **Frequency mirrors**
  - **PWM control**

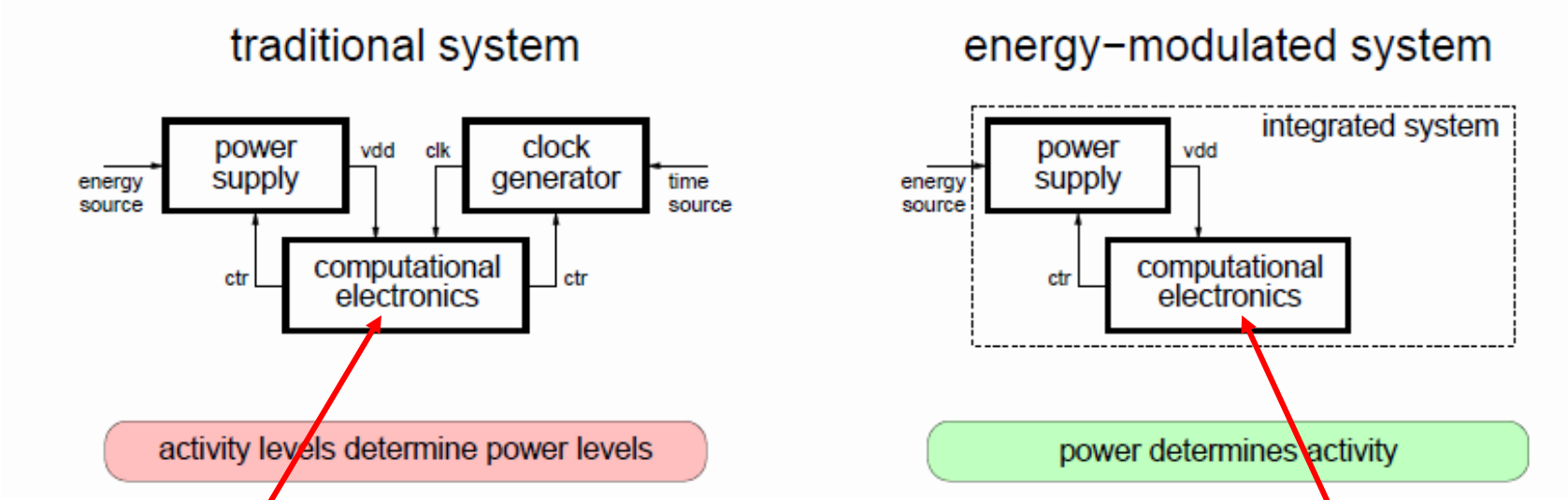
Power efficiency and regularity

- Modern systems rely on highly regular (periodic) power sources – they "invest" some power into power regulation
- Future systems will have to operate in a wide dynamic range, paying the price in efficiency in a particular band



We have to learn how to compute from unregulated power sources

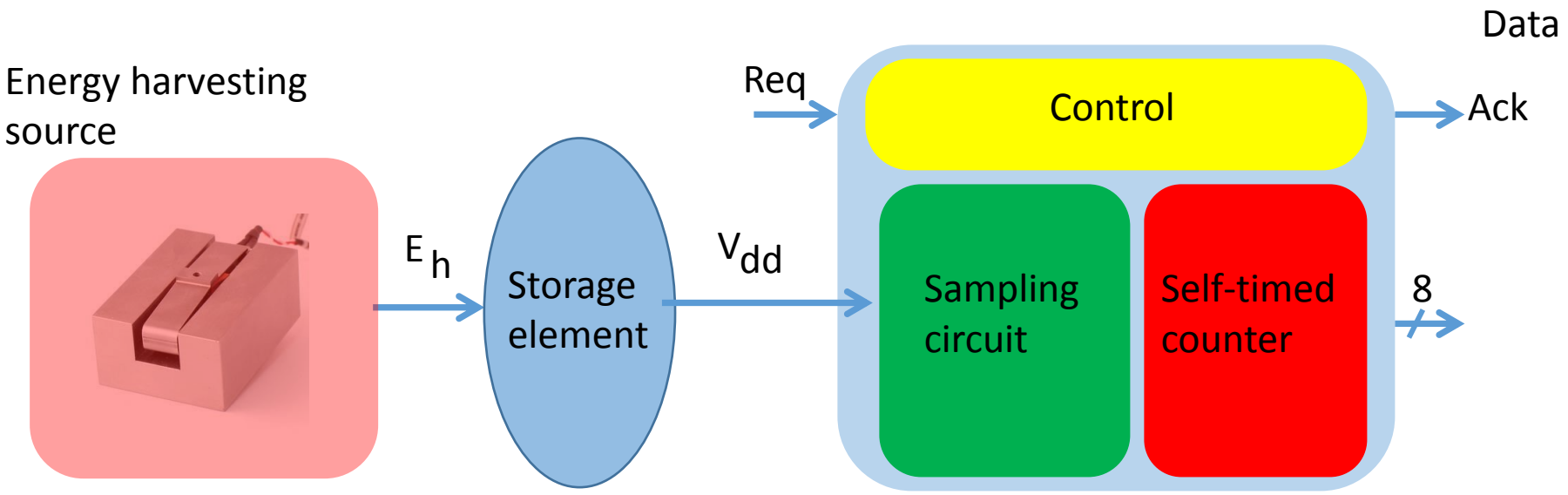
Traditional vs energy-modulated view



Activity-controlled impedance (potentiometer)

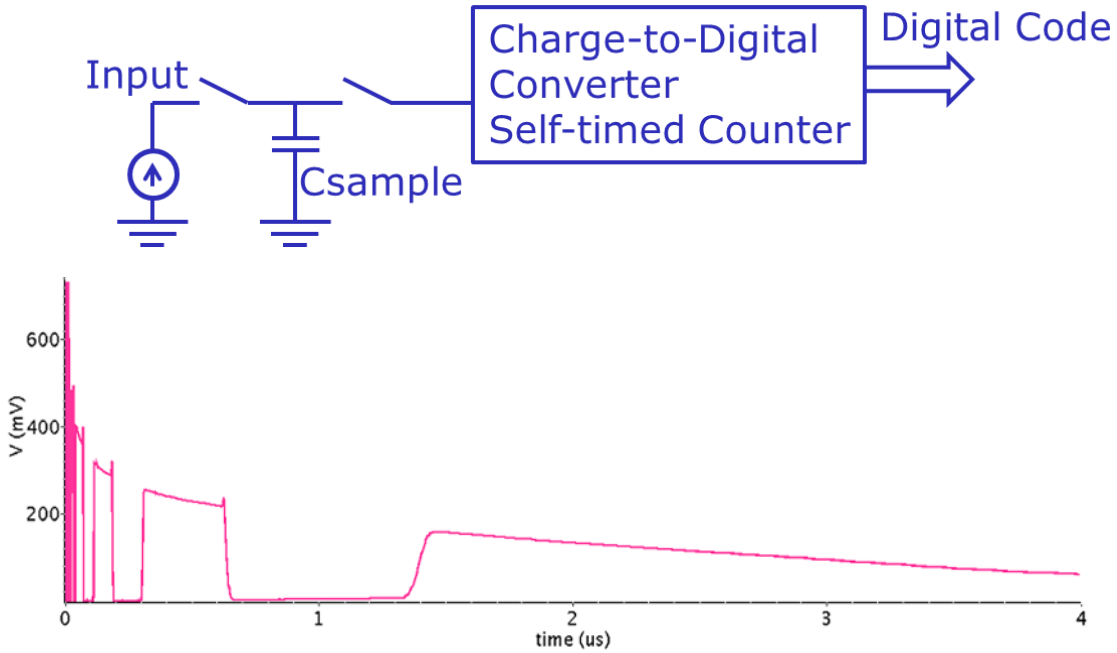
Voltage-controlled oscillator

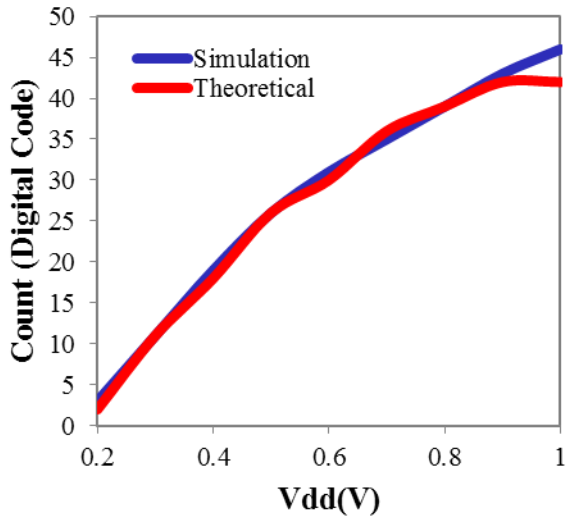
Example: Reference-free voltage sensor



Reference-free voltage sensing

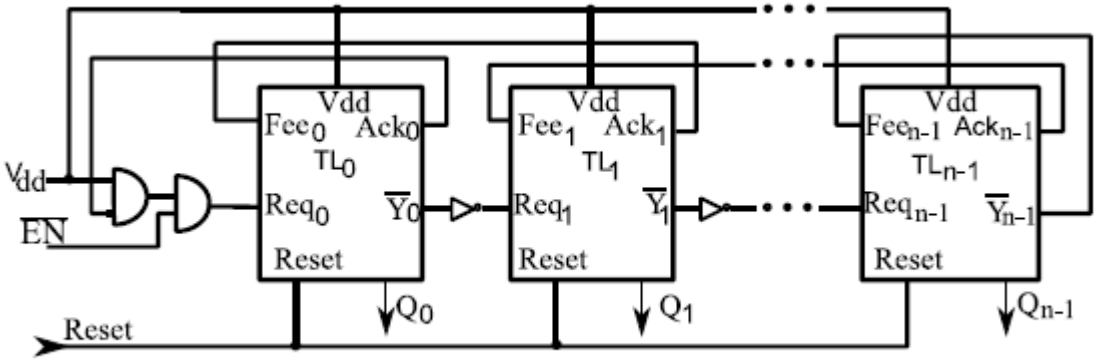
- Voltage sensor requiring only timing reference



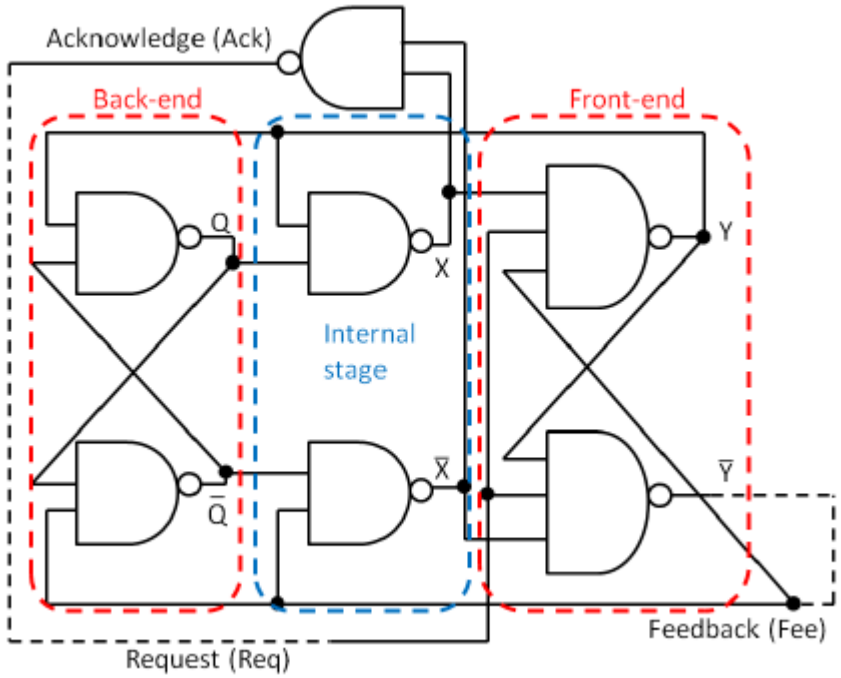


Apparatus and method for voltage sensing, Newcastle University, GB Patent Number 2479156, 30 March 2010.

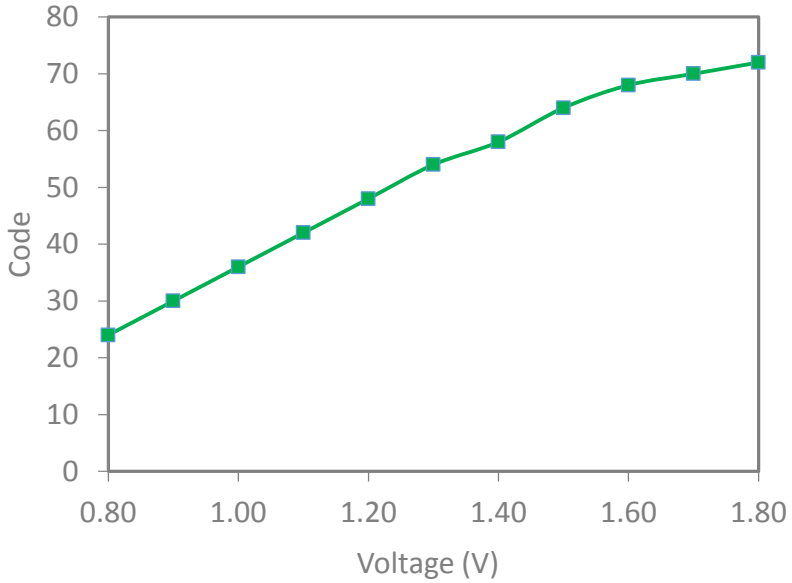
Self-timed counter

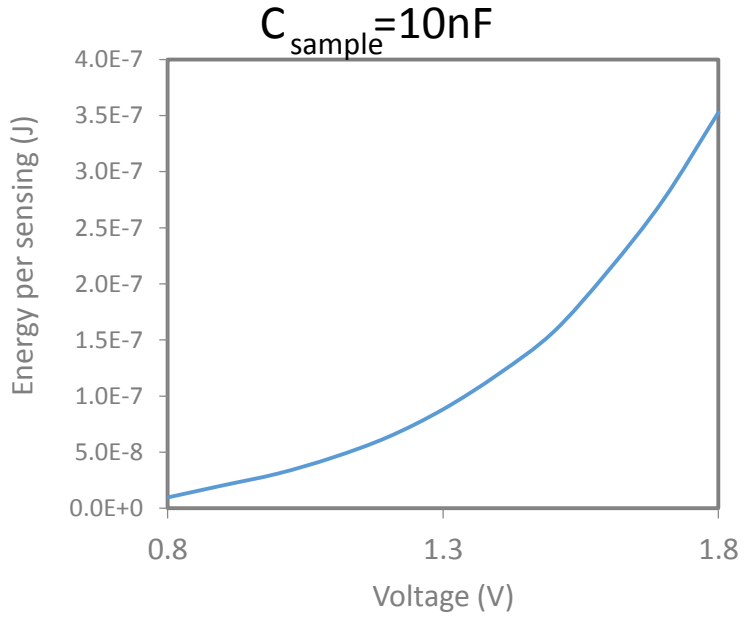


Toggle

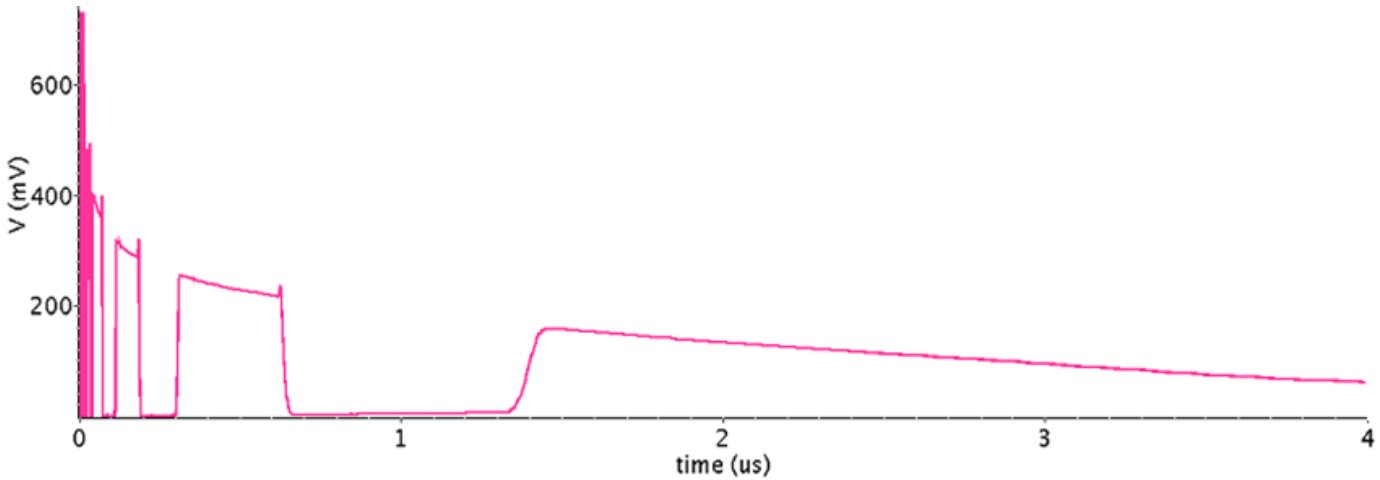


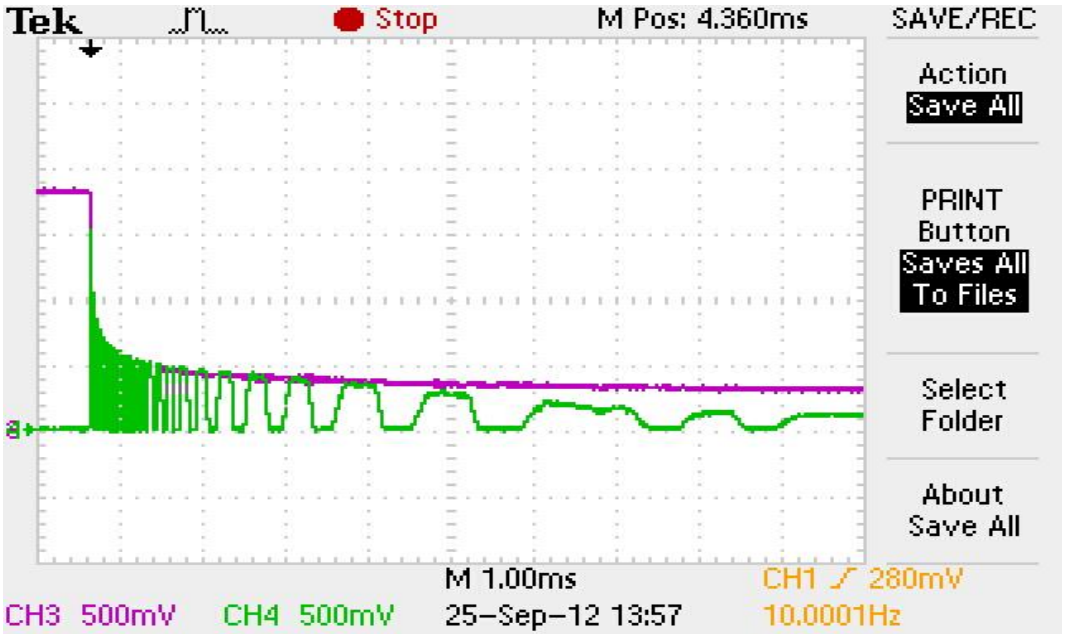
Output count and energy consumption





But the curious thing was this discharge:

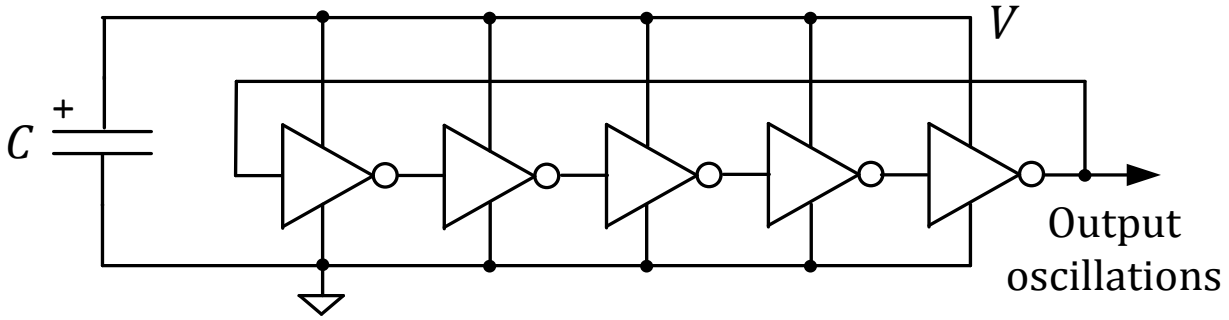




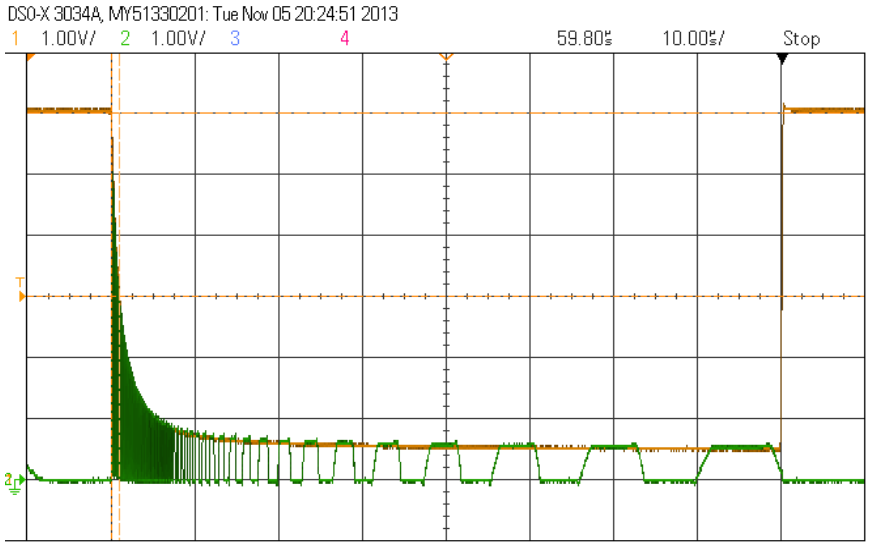
It didn't look exponential at all!

So, what was it?

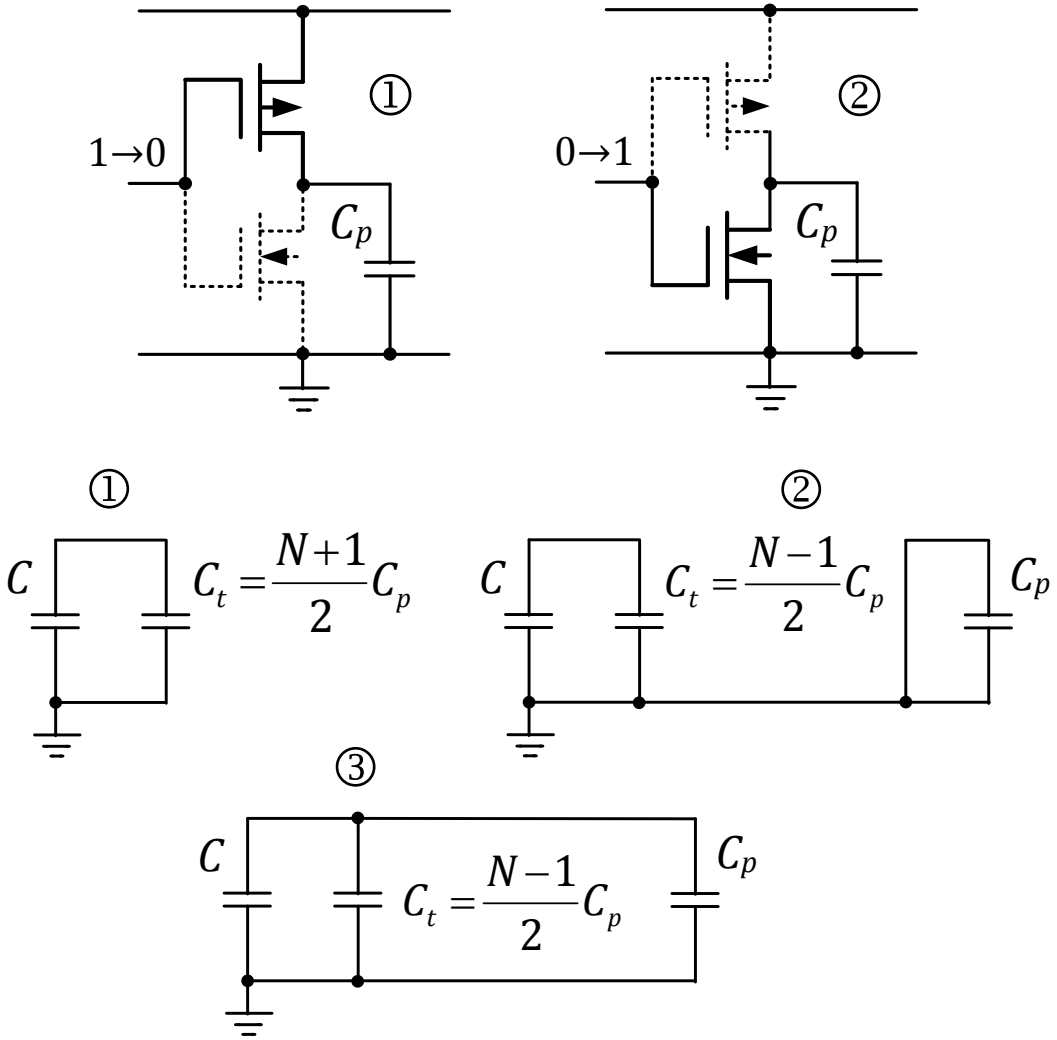
What is Computational Load?



- Use a capacitor as an elementary finite energy storage, and a ring-oscillator to serve as a digital circuit load.
- The Ring-oscillator can closely mimic the switching behaviour of many closed loop self-timed circuits.



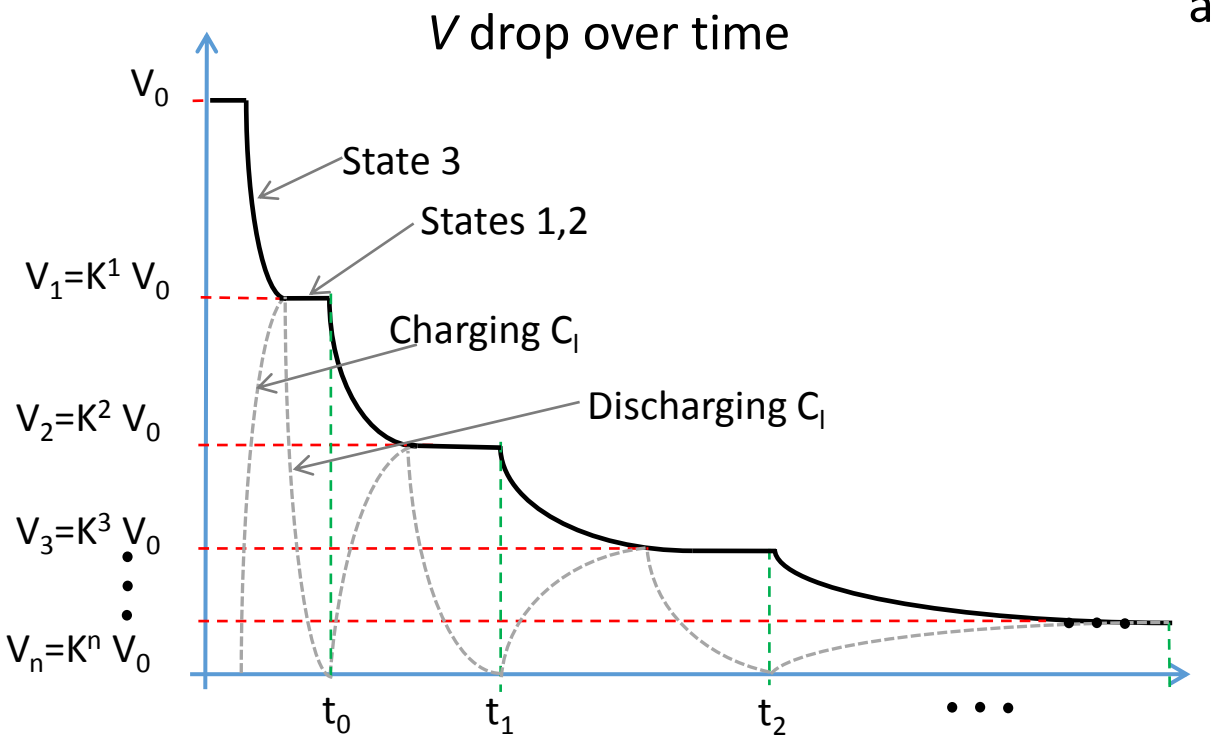
Circuit model



It's a switched capacitor model.

Three states, 1->2->3 are repeated, where the role of Cp is played by every new inverter's output cap

Circuit Model: switching process



Charge equilibrium can be applied:

$$V_1 = V_0 \frac{C}{C + C_l}$$

$$K = \frac{C}{C + C_l}$$

$$V = K^n V_0$$

$$V_N = K^n$$

Realistic value of K: $K \lesssim 1$, *say 0.99, as* $C_l \ll C$

Solution for Super-threshold

A valid assumption: in super-threshold region we can assume that the propagation delay is inversely proportional to the voltage, so we have:

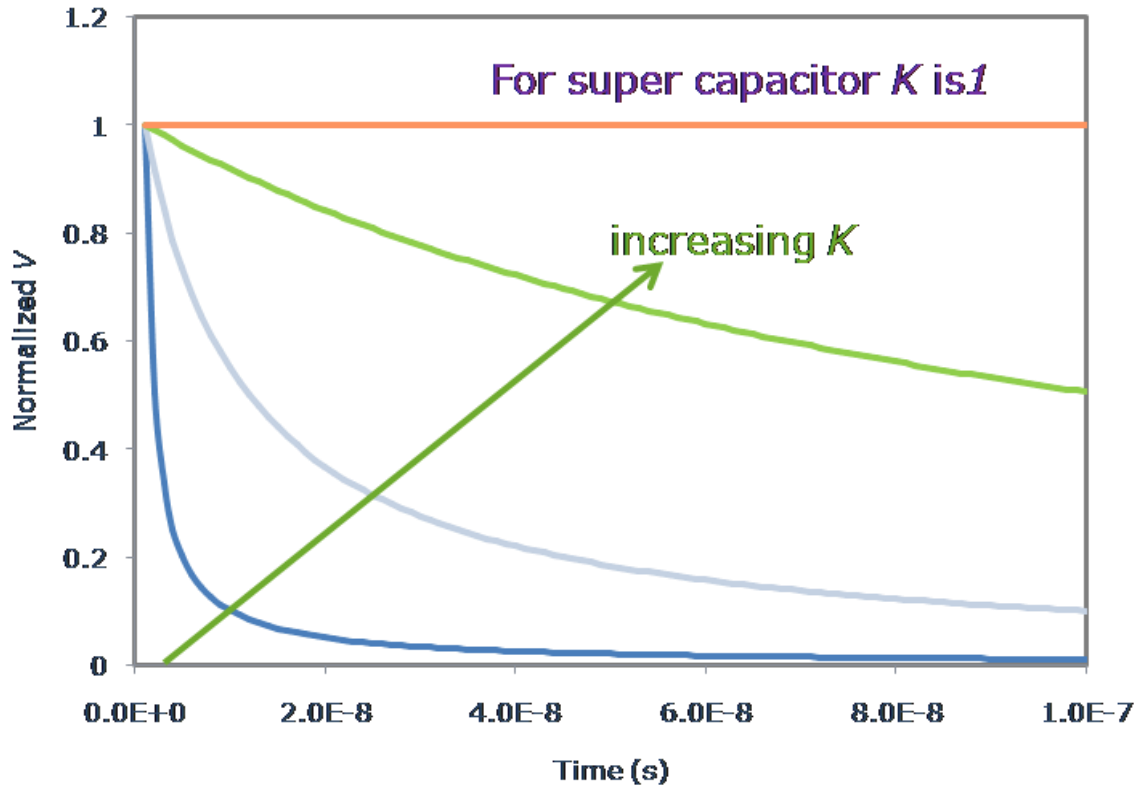
Switching index	V_N	$t_s = \frac{A}{V}$	Physical time (t)
0	K^0	$\frac{A}{K^0}$	$\frac{A}{K^0}$
1	K^1	$\frac{A}{K^1}$	$\frac{A}{K^0}+\frac{A}{K^1}$
2	K^2	$\frac{A}{K^2}$	$\frac{A}{K^0}+\frac{A}{K^1}+\frac{A}{K^2}$
…			
n	K^n	$\frac{A}{K^n}$	$\sum_{i=0}^{n}\frac{A}{K^i}$

Using sum of geometric progression, we can find the solution relating *V* and *t*

Solution for Super-threshold

$$V_N = \frac{AK}{t(1-K)+AK}$$

Hyperbolic function of time

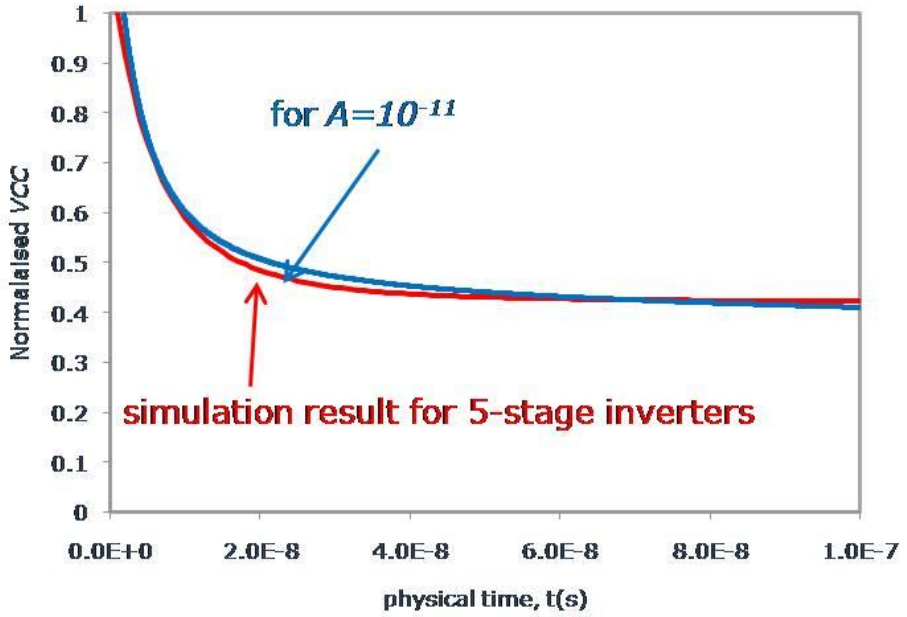


Realistic value of $K \lesssim 1$

More accurate solution for Super-threshold

A general model of gate delay propagation [1] is used:

$$t_p = \begin{cases} t_{p1} = \dfrac{pc_l V}{(V - V_{TH})^{\alpha}} \\ t_{p2} = \dfrac{pc_l V}{I_0 e^{\frac{V - V_{TH}}{N_s}}} \end{cases}$$



Assuming $\alpha = 1.3$

$$\int_0^n \frac{AK^i}{(K^i - V_{THN})^{\alpha}} di = V_{THN} + \left(\frac{-\frac{10}{3}A}{\ln K \cdot (t - B \cdot A)}\right)^{3.33}, B = \frac{\frac{10}{3}}{\ln K \cdot (1 - V_{THN})^{0.3}}$$

[1] “Sub-threshold Design for Ultra Low Power Systems”, A.Wang, B. H. Calhoun, A. P. Chandrakasan

Analysis of hyperbolic decays

- For super-threshold and α=2:

$$V_N = \frac{AK}{(1-K)t + AK} = \frac{1}{at+1};$$

where $A = 2pC_p$ *and* $a = \frac{1-K}{AK}$; ***a* is a decay rate – an important parameter!**

(cf. "inverse of time constant")

- For arbitrary α:

$$V_N = \frac{1}{(at+1)^{1/(\alpha-1)}} \text{ and } a = \frac{1-K^{\alpha-1}}{AK^{\alpha-1}}$$

- Differential equation:

$\frac{dV}{dt} = -aV^{\alpha}$; for α=2, we can see that $\frac{dV}{dt} = \frac{-a}{(at+1)^2} = -aV^2$

The oscillator is a voltage (and time)-varying resistor:

$R(V) = \frac{2p}{V}$ or $R(t) = 2p(at+1)$

Analysis of hyperbolic decay rates

- For stack and parallel configurations we then apply Kirchhoff's laws (KVL and KCL), based on:

$$i_C = C\frac{dV_C}{dt} = -aCV_C{}^{\alpha}$$

- For stack:

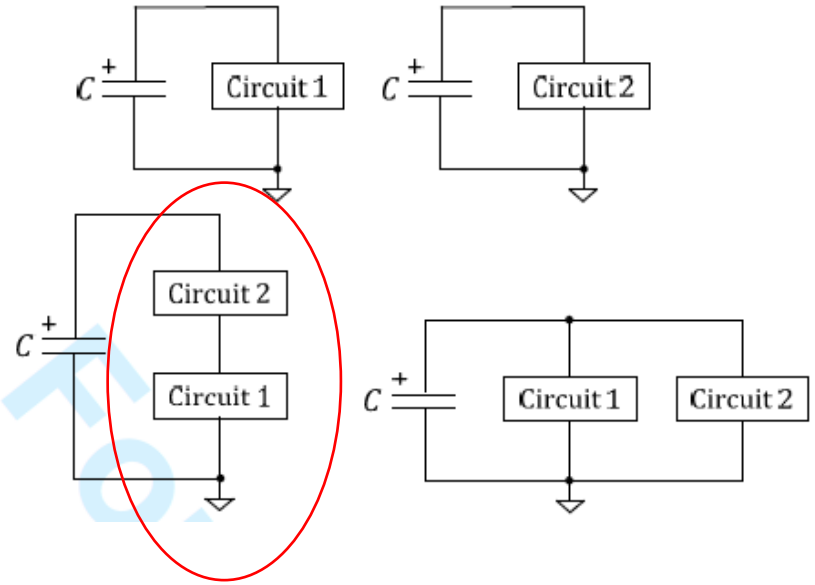
$$\begin{cases} V = V_1 + V_2 \\ C\dfrac{dV}{dt} = C_1\dfrac{dV_1}{dt} = C_2\dfrac{dV_2}{dt} \end{cases}$$

And since $C = C_1 = C_2$

$$\begin{cases} V = V_1 + V_2 \\ aV^{\alpha} = a_1V_1{}^{\alpha} = a_2V_2{}^{\alpha} \end{cases}$$

We have: $\left(\frac{1}{a}\right)^{\frac{1}{\alpha}} = \left(\frac{1}{a_1}\right)^{\frac{1}{\alpha}} + \left(\frac{1}{a_2}\right)^{\frac{1}{\alpha}}$

Series (stack) and parallel configurations:



stack

Analysis of hyperbolic decay rates

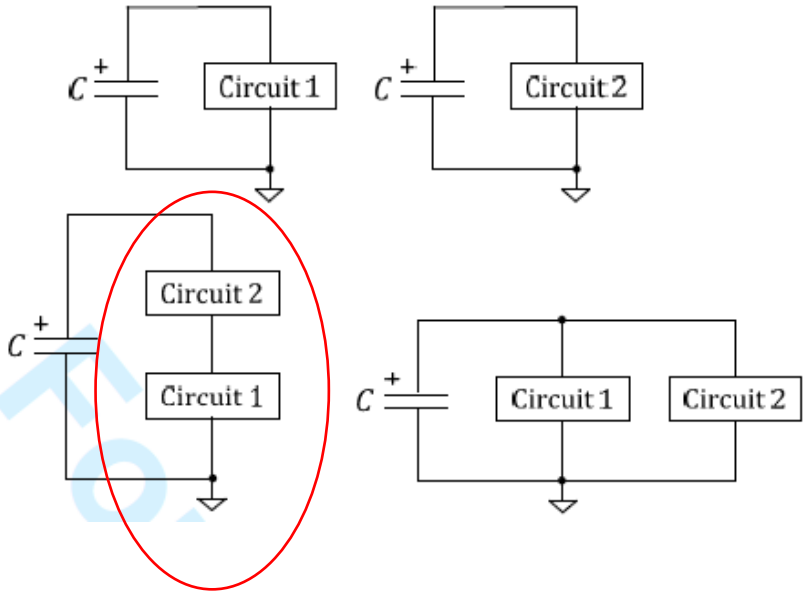
- For stack:

$$\left(\frac{1}{a}\right)^{\frac{1}{\alpha}} = \left(\frac{1}{a_1}\right)^{\frac{1}{\alpha}} + \left(\frac{1}{a_2}\right)^{\frac{1}{\alpha}} \text{ or}$$

$$a = \frac{a_1 a_2}{\left(\sqrt[\alpha]{a_1} + \sqrt[\alpha]{a_2}\right)^{\alpha}}$$

- For parallel: $a = a_1 + a_2$
- Confirmed by physical experiments with discrete CMOS components:
  - ***The value of alpha is 1.5***
  - ***The discharging process for a stack of two identical circuits is nearly 3 times slower than for a standalone circuit***

Series (stack) and parallel configurations:



stack

By the way .....

- For stack:

$$\left(\frac{1}{a}\right)^{\frac{1}{\alpha}} = \left(\frac{1}{a_1}\right)^{\frac{1}{\alpha}} + \left(\frac{1}{a_2}\right)^{\frac{1}{\alpha}} \text{ or}$$

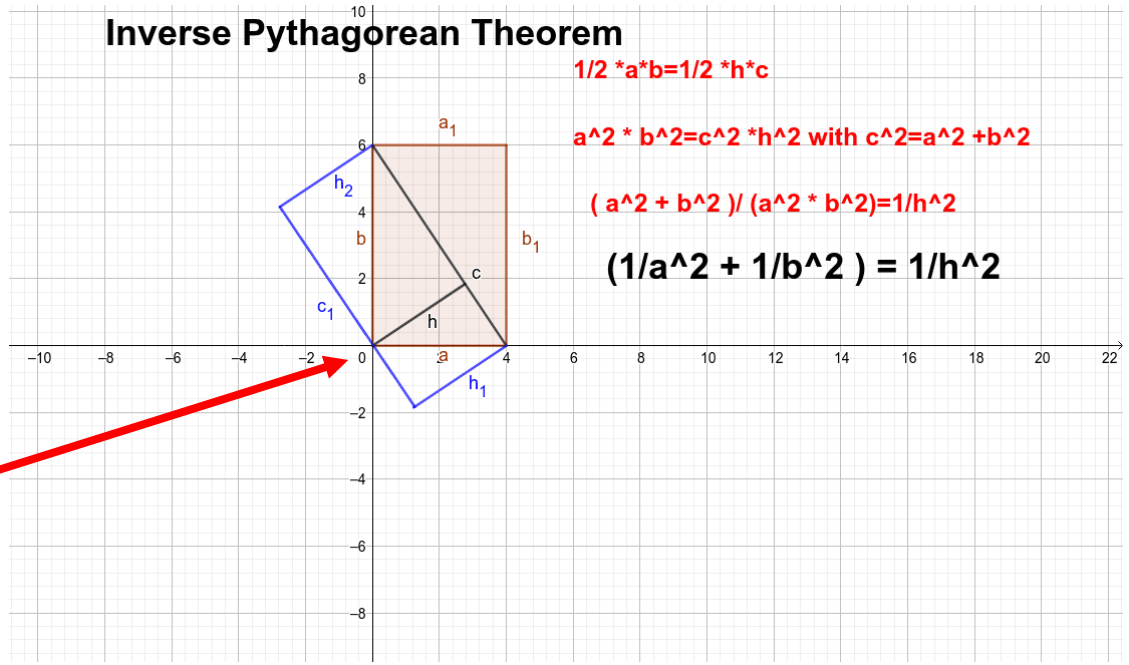
$$a = \frac{a_1 a_2}{\left(\sqrt[\alpha]{a_1} + \sqrt[\alpha]{a_2}\right)^{\alpha}}$$

For α = 2:

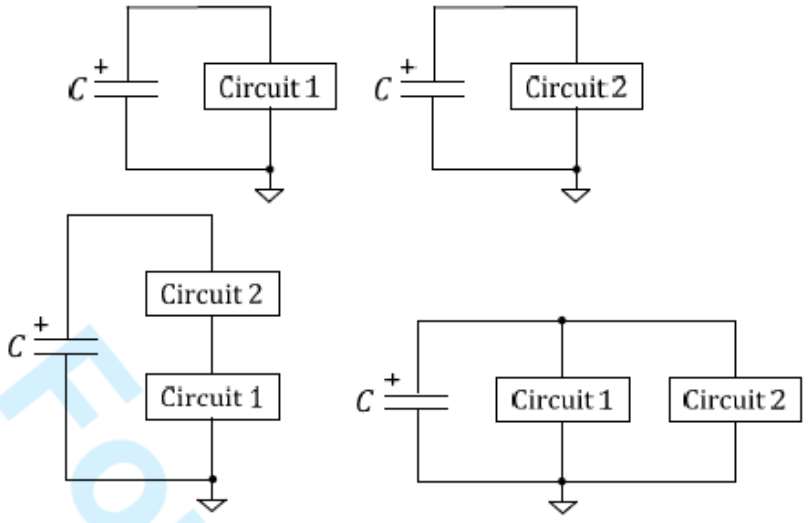
$$\left(\frac{1}{a}\right)^{\frac{1}{2}} = \left(\frac{1}{a_1}\right)^{\frac{1}{2}} + \left(\frac{1}{a_2}\right)^{\frac{1}{2}} \text{ or}$$

$$a = \frac{a_1 a_2}{\left(\sqrt[2]{a_1} + \sqrt[2]{a_2}\right)^{2}}$$

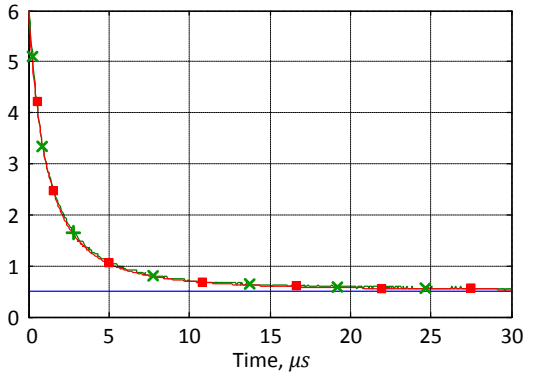
Series (stack): discharge rate follows the law of the inverse Pythagorean!



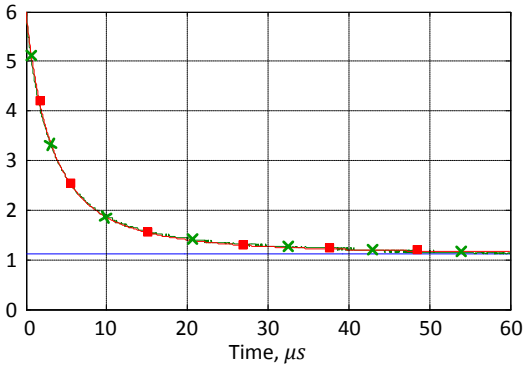
Capacitor discharge experiments



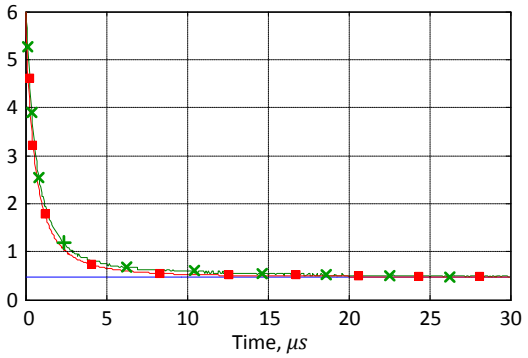
Standalone



Stack



Parallel



More details can be found in:

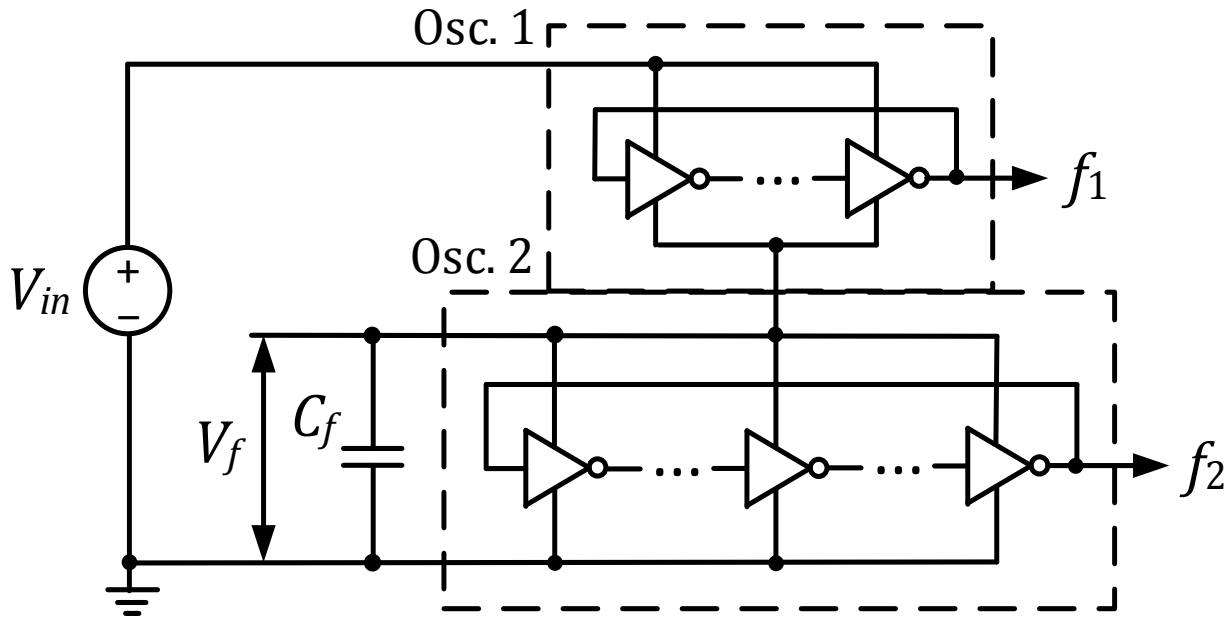
A. Yakovlev, A. Kushnerov, A. Mokhov and R. Ramezani, On hyperbolic laws of capacitor discharge through self-timed digital loads, Int. J. Circ. Theor. Appl., vol. 43, No. 10, pp. 1243-1262, October 2015; doi: 10.1002/cta.2010

Including:

- Derivations of the main theoretical results,
- Analysis of charge sharing modes due to partial overlap of switching in the top and bottom of the stack,
- Simulations and physical experiments using discrete components, and comparisons between experimental and theoretical predictions, as well as
- Experimental measurement of the alpha-parameter, which was around 1.5

Stacking Voltage-Controlled Oscillators in DC powered circuits: Analysis and Application

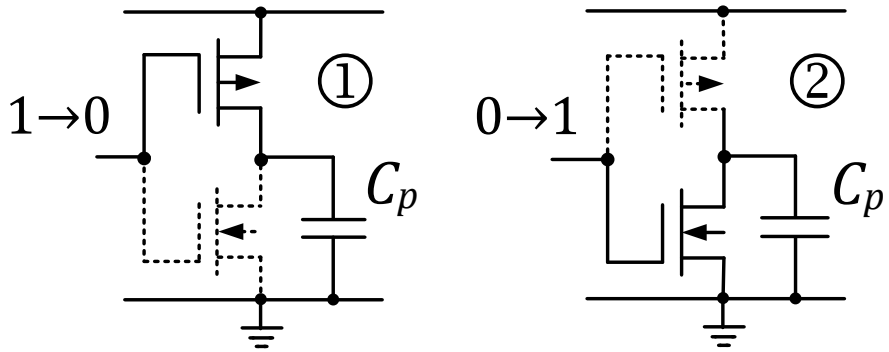
Stack connection of two ring oscillators

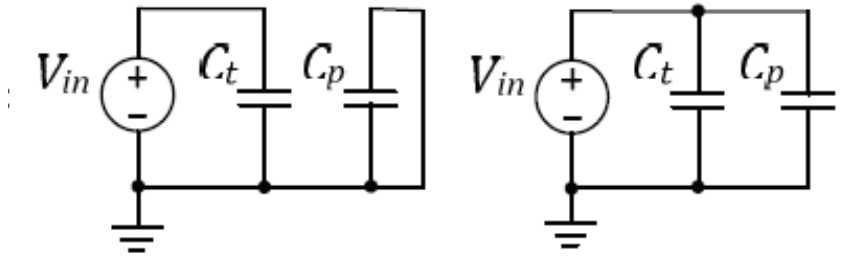


- We are talking about DC, i.e. about average value of V_f in steady state
- In practice due to short-circuit currents V_f is close to $0.5V_{in}$ and does not depend on the number of inverters

Model of an inverter

Topologies of the ring oscillator

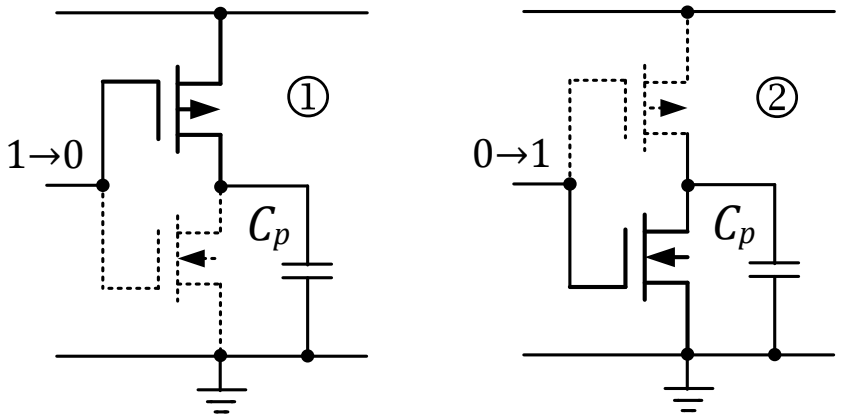


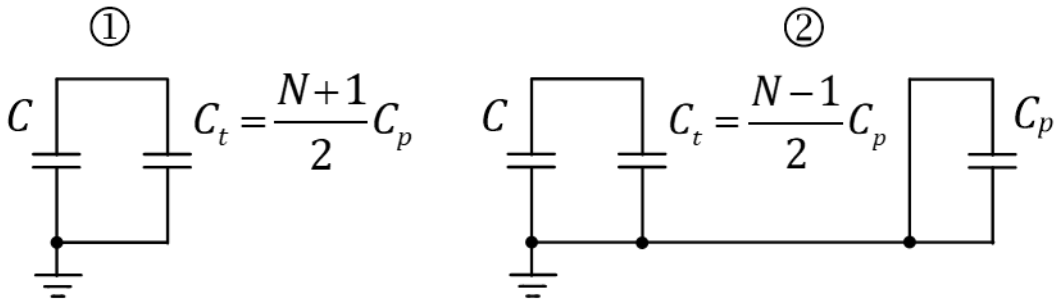


- The model does not take into account short circuit current and leakage

- The capacitance of $C_t = C_p\,(n-1)/2$ increases with increase of the number of inverters, n

Reminder:
Circuit model with the discharging cap





This is a model of a circuit with constantly switching capacitors!

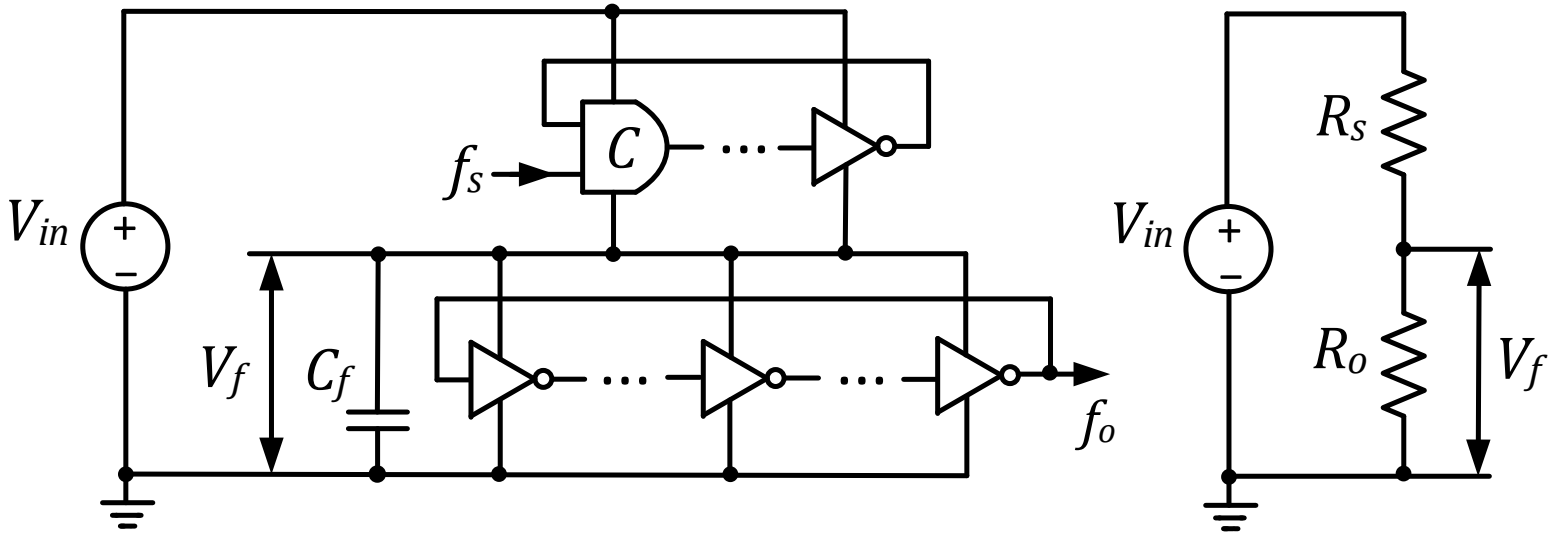
The role of a switched cap C_p is played by every inverter in turn.

So in the equivalent switching cap circuit C_p is an "effective switching cap"

The effective impedance of the circuit becomes $R_{switch} = \frac{1}{f_{switch} C_p}$ where f_{switch}=1/2 t_{su},

t_{su} is propagation delay of an inverter

Externally clocked stack



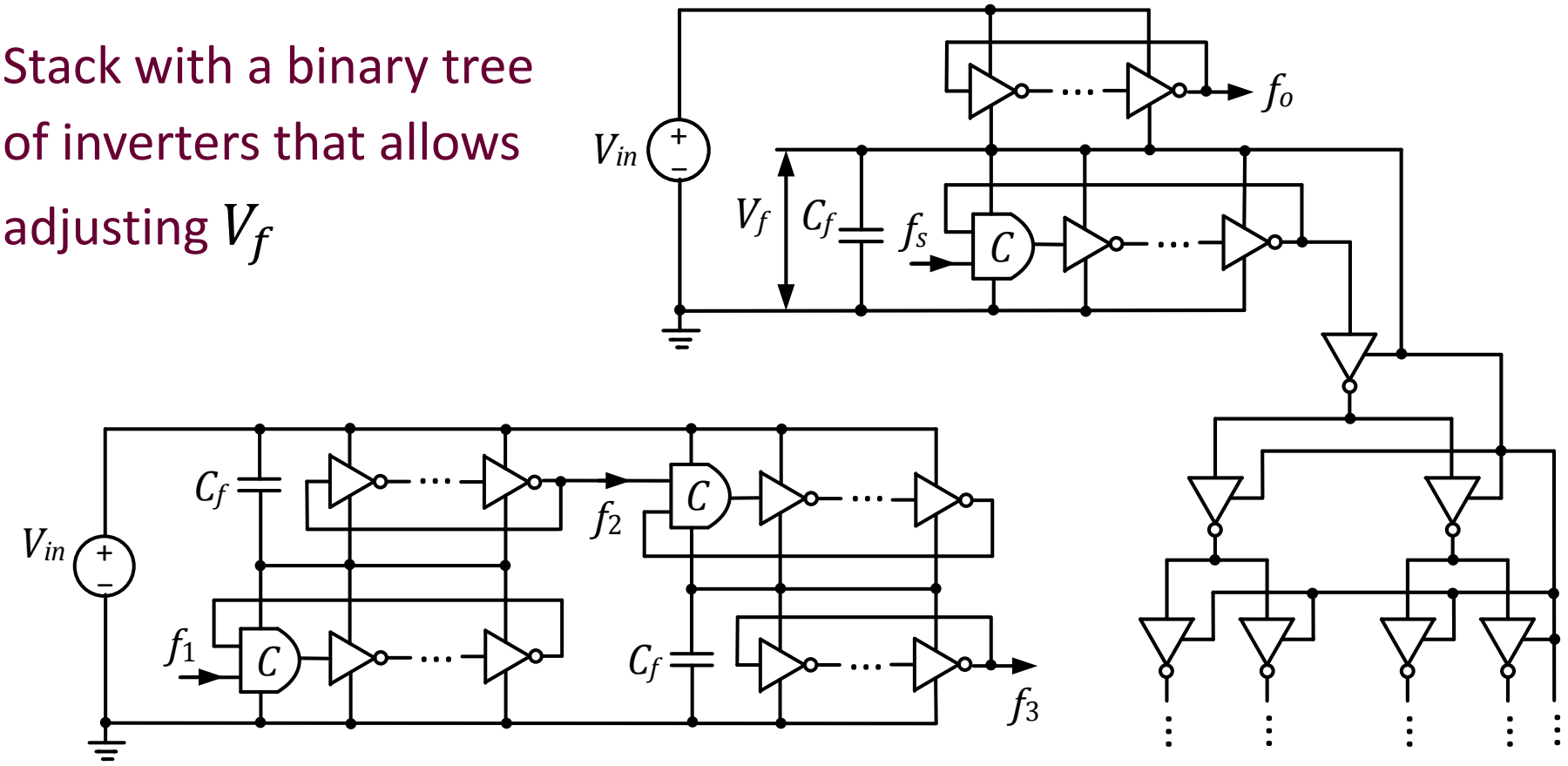
Muller C-element: $y = x_1 x_2 + (x_1 + x_2)y$

- After some transient the system will reach steady-state defined by

$$R_s = \frac{1}{f_s C_p}; \quad R_o = \frac{1}{f_o C_p}; \quad \frac{V_f}{V_{in} - V_f} = \frac{R_o}{R_s} = \frac{f_s}{f_o}$$

Possible applications

- Stack with a binary tree of inverters that allows adjusting V_f



- Cascade of two clocked stacks **(frequency mirror)** that decouples the control frequency from the ground.

Main Effects in the Proposed Circuit

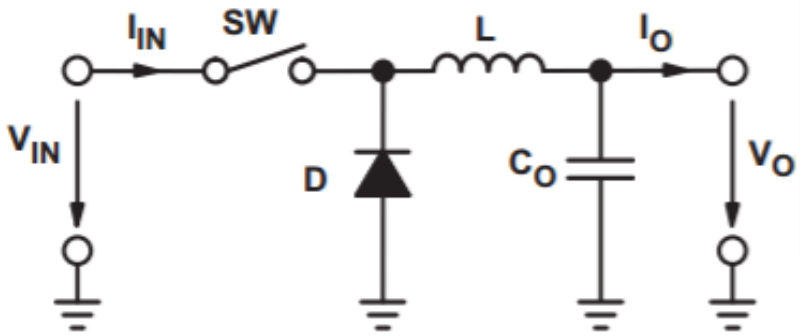
- Transient, caused by the frequency change and followed by stabilization via the internal feedback “voltage–frequency–impedance–voltage”

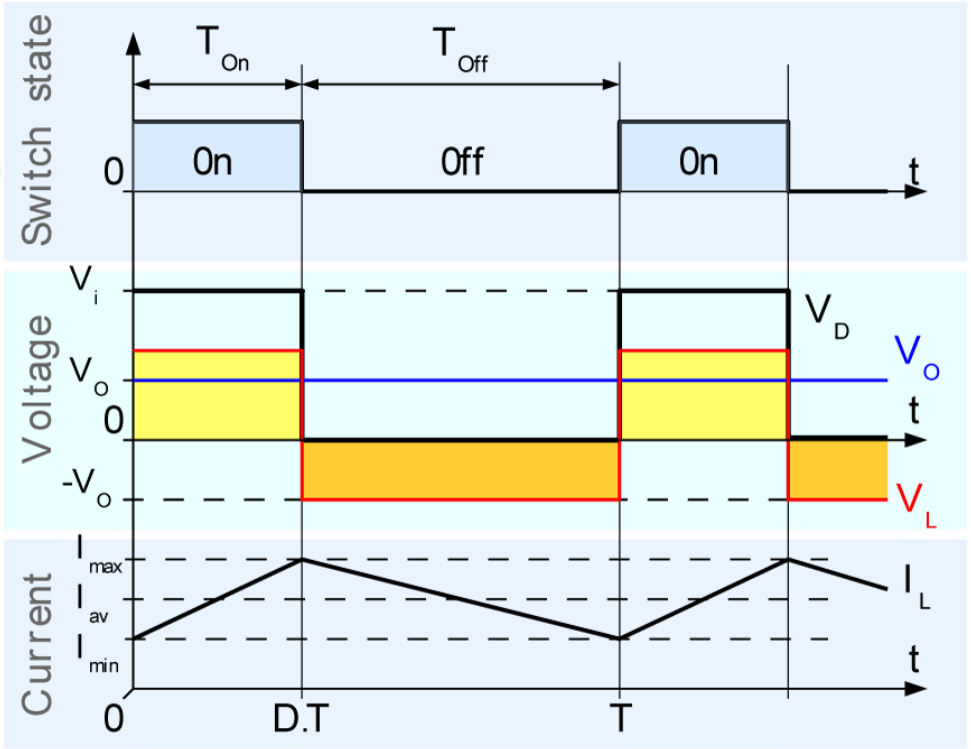
- Steady state with some ripple, whose level depends on how the oscillators interact and on how well the products of this interaction are averaged

Application: Pulse Width Modulation (PWM)

- The general purpose of PWM is to control power delivery

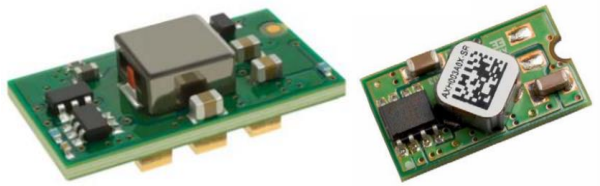
Example: step-down (buck) converter



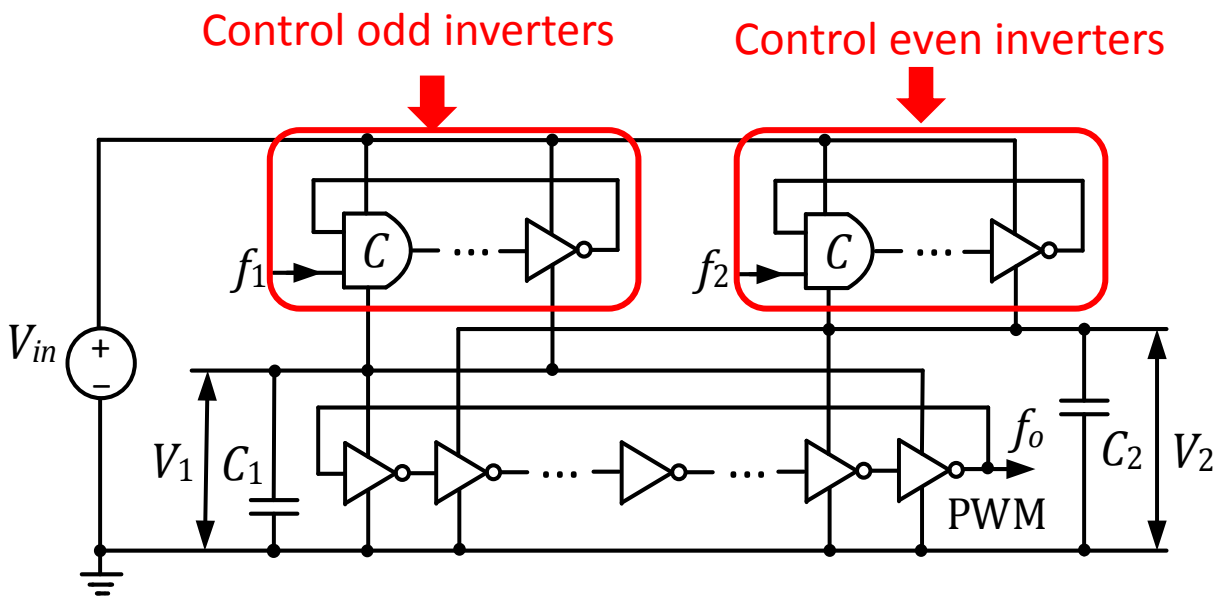


Duty cycle: $D = \frac{T_{on}}{T_{off}}$

$V_o = DV_{in}$



Frequency controlled PWM circuit



- Since we control the impedances, the transfer function will be nonlinear
- Let the initial state of the output be logical "1"
- Denote the propagation delays of odd and even inverters by t_{su1} and t_{su2} respectively, then

$$t_{on} = (n-1)t_{su2}$$

Controlled by even inverters (i.e. by f2)

$$t_{off} = (n+1)t_{su1}$$

Controlled by odd inverters (i.e.by f1)

The idea is analogous to current-starved PWM control from:

I. Vaisband, M. Azhar, E. G. Friedman and S. Köse, "Digitally controlled pulse width modulator for on-chip power management," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 22, no. 12, pp. 2527-2534, 2014.

Deriving the transfer function

- In a distinctive super-threshold region the propagation delay of an inverter is:

$$t_{su} = \frac{pC_pV_{dd}}{(V_{dd} - V_{th})^{\alpha}}$$

- Assuming $\alpha = 2$ and $V_{th} \ll V_{dd}$, we approximate $t_{su} \approx \frac{k}{V_{dd}}$

$$t_{on} = (n-1)t_{su2}; \quad t_{off} = (n+1)t_{su1}$$

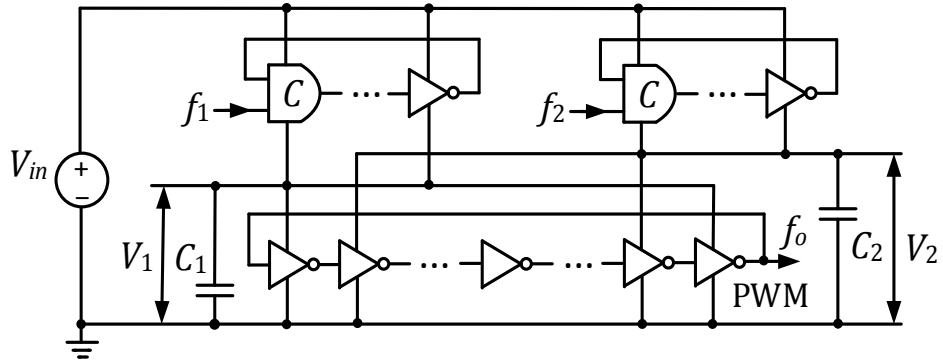
$$f_o = \frac{1}{t_{on} + t_{off}} = \frac{V_1V_2}{k[(n-1)V_1 + (n+1)V_2]}$$

$$D = t_{on}f_o = \frac{(n-1)V_1}{(n-1)V_1 + (n+1)V_2}$$

- It is evident that f_o depends on $k \approx V_{dd}t_{su}$, which should be found experimentally

Deriving the transfer function

$$D = \frac{(n-1)V_1}{(n-1)V_1 + (n+1)V_2}$$



- In the case of $V_1 = V_2$

$D = \frac{n-1}{2n}$ and tends to 0.5 for $n \to \infty$

- The condition of $V_1 = V_2$ also allows us to write

$$\frac{V_1}{V_{in} - V_1} = \frac{V_2}{V_{in} - V_2} = \frac{f_s}{f_o}; \quad f_s = \frac{2nf_1}{n+1} = \frac{2nf_2}{n-1}$$

such that

$$V_1 = \frac{2nf_1V_{in}}{2nf_1 + (n+1)f_o}; \quad V_2 = \frac{2nf_2V_{in}}{2nf_2 + (n-1)f_o}$$

Deriving the transfer function

Substituting $V_1 = \dfrac{2nf_1V_{in}}{2nf_1 + (n+1)f_o}$ and $V_2 = \dfrac{2nf_2V_{in}}{2nf_2 + (n-1)f_o}$ into $f_o = \dfrac{V_1V_2}{k[(n-1)V_1 + (n+1)V_2]}$ and $D = \dfrac{(n-1)V_1}{(n-1)V_1 + (n+1)V_2}$

we obtain a *quadratic equation for the switching frequency*

$$f_o^2 + pf_o - q = 0$$

where $p = \dfrac{4n^2f_1f_2}{(n-1)^2f_1 + (n+1)^2f_2}$; $q = \dfrac{2nf_1f_2V_{in}}{k[(n-1)^2f_1 + (n+1)^2f_2]}$

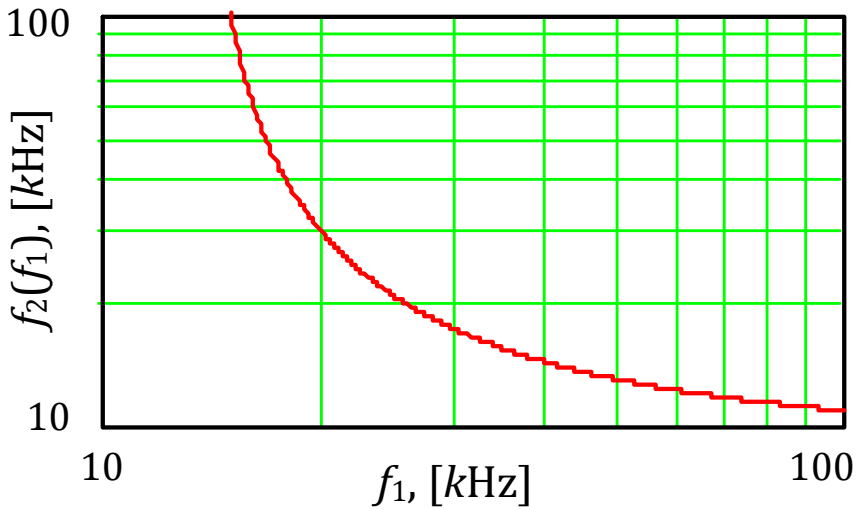
and the duty cycle depends on f_o as

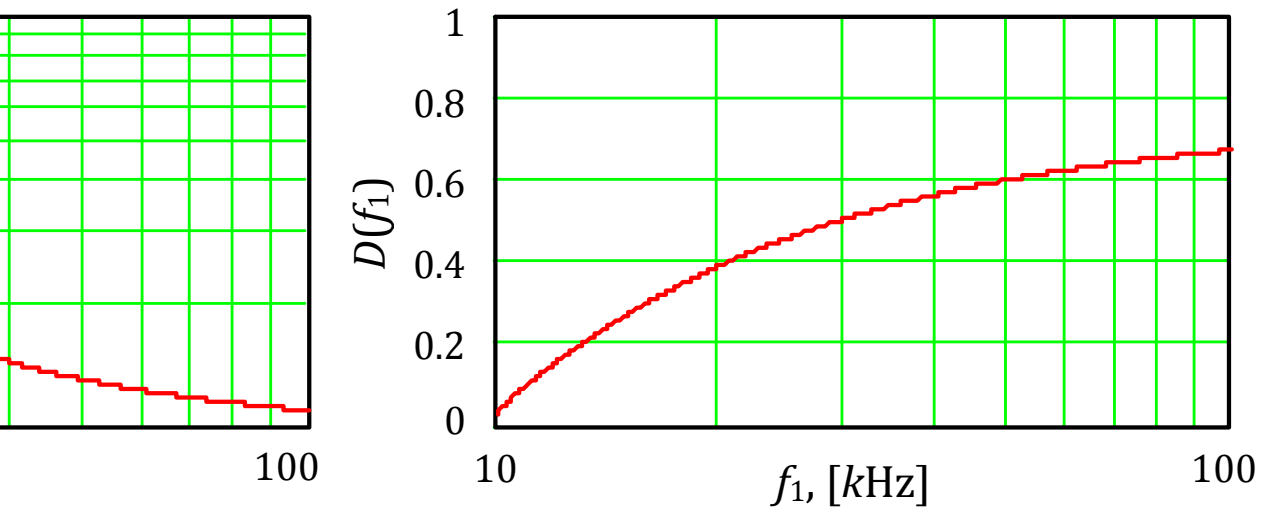
$$D = \frac{(n-1)^2f_1f_o + 2n(n-1)f_1f_2}{[(n-1)^2f_1 + (n+1)^2f_2]f_o + 4n^2f_1f_2}$$

Keeping the output frequency constant

- The disadvantage of the considered circuit is that changing D, we change f_o
- Let $f_o = const$ and express f_2 through f_1

$$f_2(f_1) = \frac{k(n-1)^2 f_o^2 f_1}{2n(V_{in} - 2knf_o)f_1 - k(n+1)^2 f_o^2}; \quad D(f_1) = \frac{2n(V_{in} - (n+1)kf_o)f_1 - (n+1)^2 f_o^2}{2n(V_{in} - 2kf_o)f_1 - 2(n+1)kf_o^2}$$



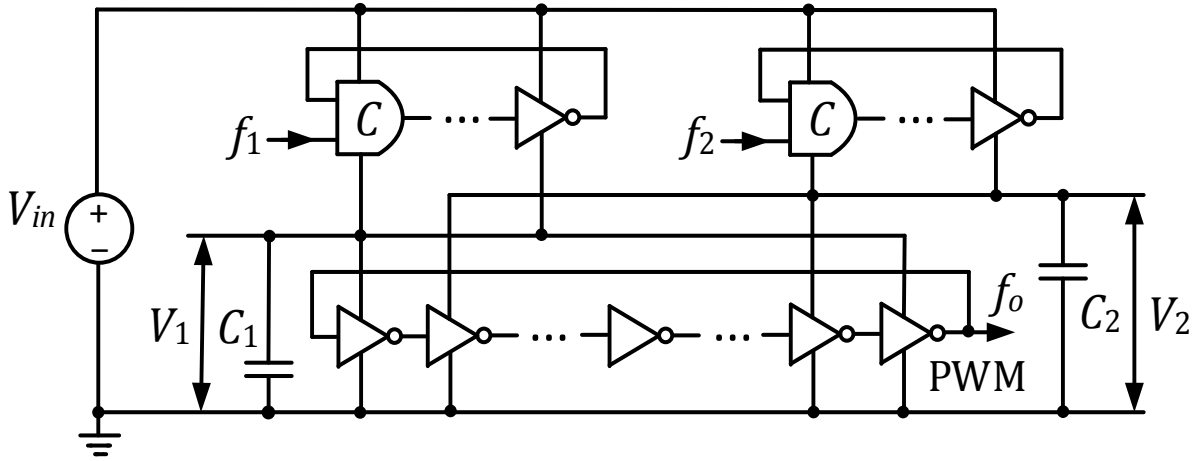


$$f_o = 50k\text{Hz}$$

Simulation Results

$$t_{su} = \frac{pC_pV_{dd}}{(V_{dd} - V_{th})^{\alpha}}$$

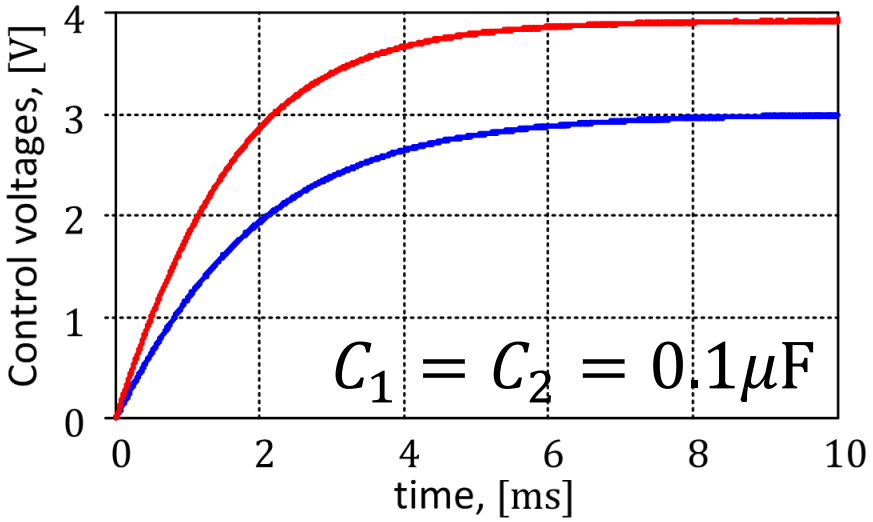
$$t_{su} \approx \frac{k}{V_{dd}}$$

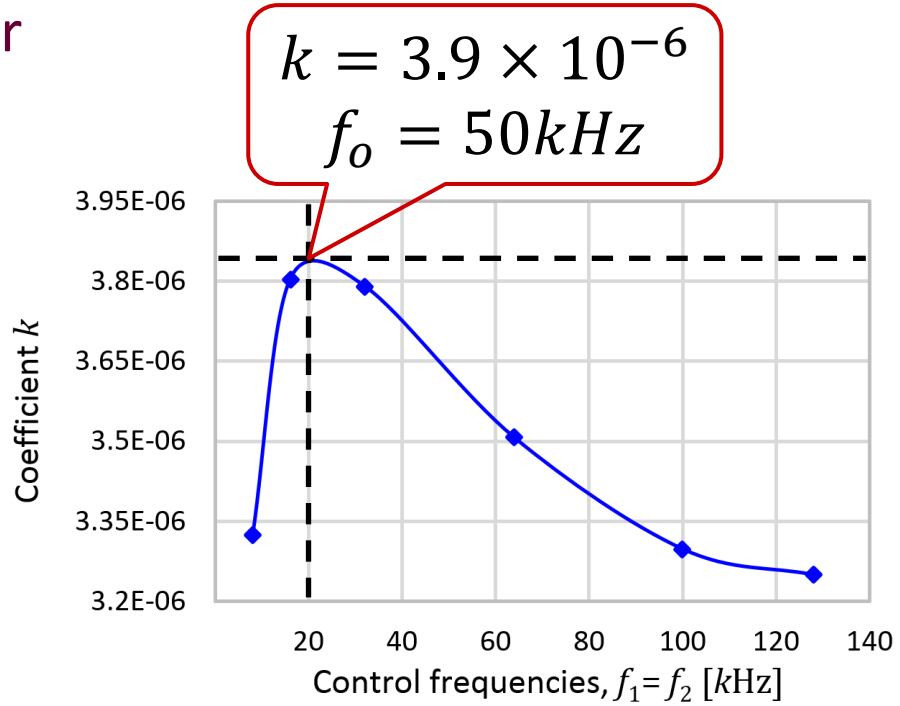


- To provide $\alpha \approx 2$ and $V_{dd} \gg V_{th}$ we used the standard CMOS inverter 74LVC04 with $V_{in} = 9V$
- To provide high switching speed, we used the so-called static C-element
- Each of the C-elements is connected to one inverter, while the footer consists of $n = 11$ inverters

Simulation Results

- Stabilization of the voltages for $f_1 = 64k\text{Hz}$ and $f_2 = 32k\text{Hz}$





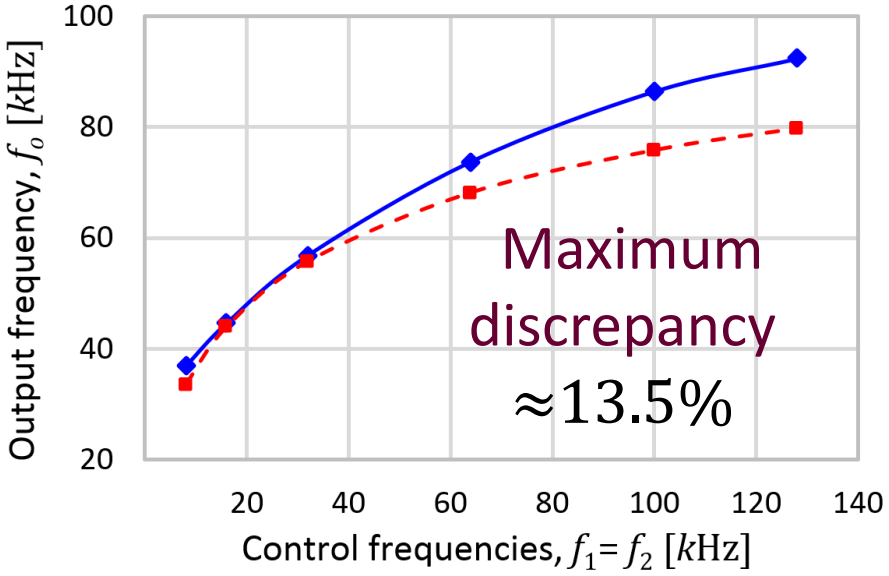
- To calculate the values of f_o and D, we need to find k

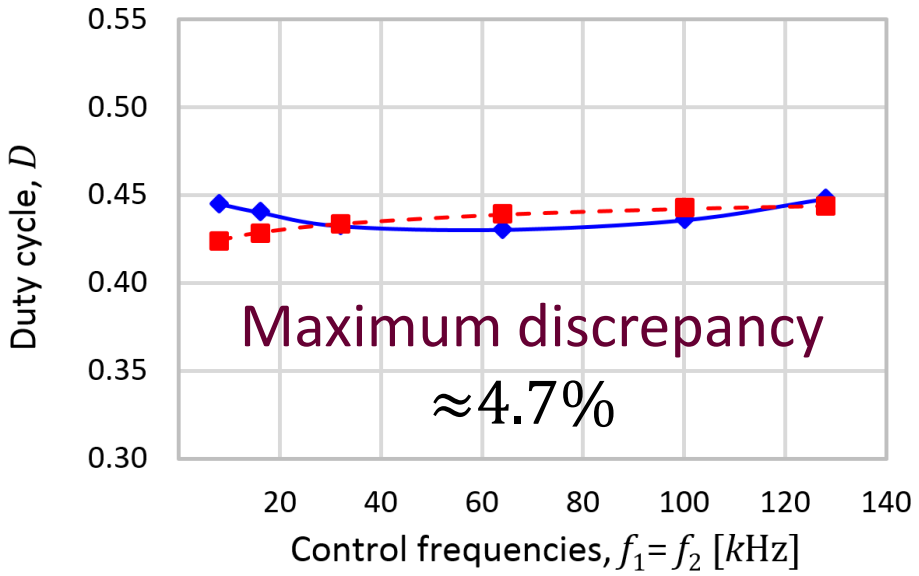
$$k = \frac{V_{in}}{\left[\left(n + \frac{1}{n}\right)\frac{f_o}{f} + 2n\right] f_o}$$

where $f = f_1 = f_2$ is the control frequency

Simulation Results

Output frequency and duty cycle as a function of two equal control frequencies





Dashed line: calculated as a solution of

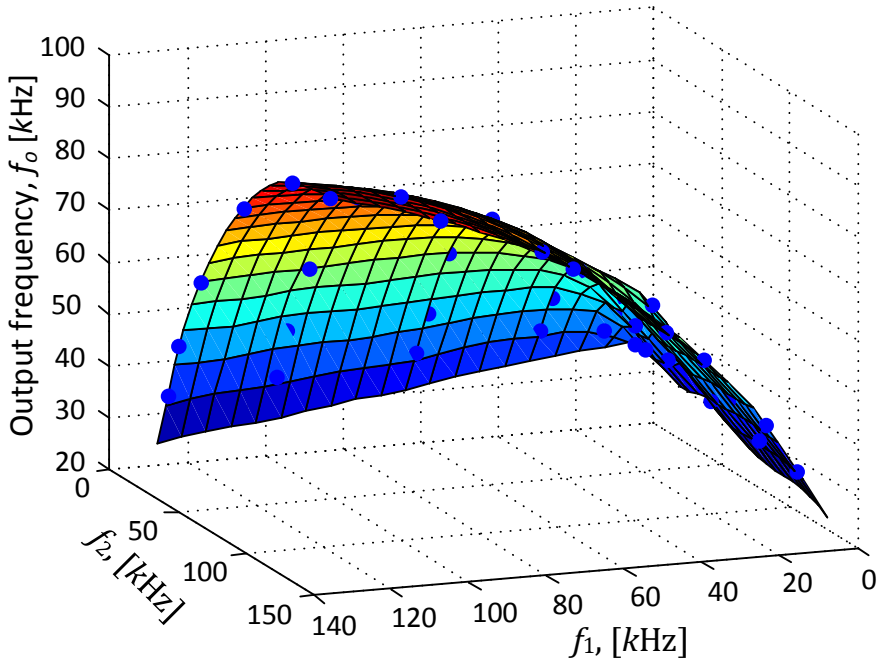
$$f_o^2 + pf_o - q = 0$$

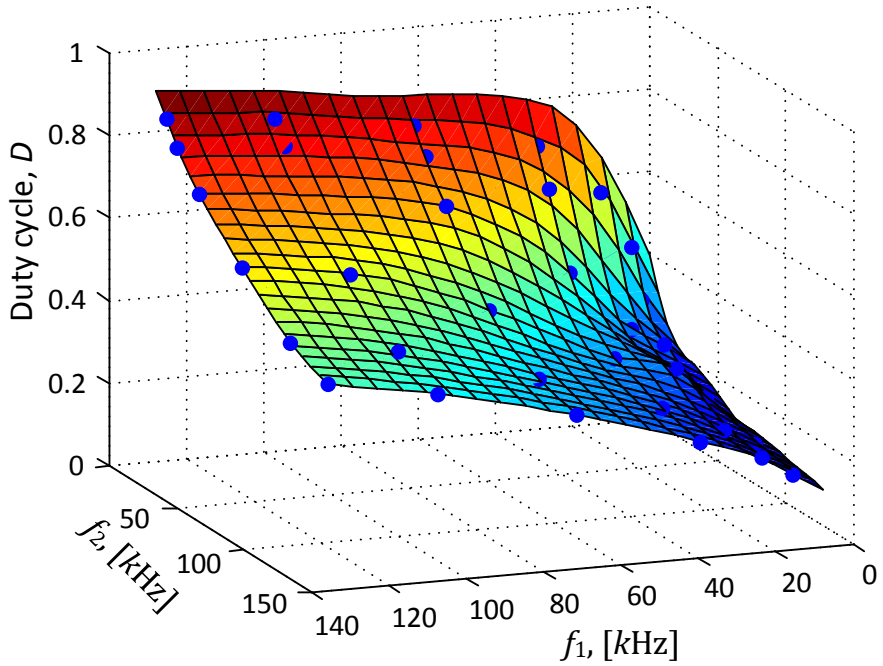
Dashed line: calculated by

$$D = \frac{(n-1)^2 f_1 f_o + 2n(n-1) f_1 f_2}{[(n-1)^2 f_1 + (n+1)^2 f_2] f_o + 4n^2 f_1 f_2}$$

Simulation Results

Output frequency and duty cycle as a function of two different control frequencies





- Both of the surfaces are built using a set of theoretically calculated points

Conclusions

- In capacitor-powered systems asynchronous load causes hyperbolic (rather than exponential!) discharge – it is much slower than exponential
- Stacking in series allows to extend the life-time at the cost of greater delay
- Stack of two ring oscillators is a self-adjusting system
- Large filter capacitances make the interaction between oscillators weak and defined as the ratios of their quasi-static impedances
- To keep the output frequency of the PWM circuit constant we need to adjust one of the control frequencies
- It would be advantageous to have inverting elements with delay strictly reciprocal to V_{dd}
- An interesting direction is to develop frequency insensitive computational elements, where the information is represented by duty cycle (phase) – we have built a perceptron based on PWM (paper at DATE 2019 and Royal Soc Transactions, under review)

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Thank you
for your attention!