Stacked Asynchronous Circuits

or

Elements of Circuit Theory involving digital circuits as impedances

Alex Yakovlev, microSystems,
School of Engineering, Newcastle University
async.org.uk
www.ncl.ac.uk/engineering/research/eee/microsystems/

2nd Workshop Hardware Design and Theory,
Budapest 18 Oct 2019
Stacking asynchronous circuits:

Why would we want to stack them?
- One possible motivation is to gain power efficiency, because: Power \( \sim V_{dd}^2 \), while speed \( \sim 1/V_{dd} \)
- The other motivation is purely theoretical, to see what kind of behaviour we can have for different power sources
- Basically what sort of impedances are asynchronous circuits?!
Related work

• Some work on stacking QDI circuits was reported at University of Arkansas:
  https://www.flintbox.com/public/project/57790/

• In our work we mainly focus on VCO (inverter rings), which offer interesting applications by themselves.

• And we came across stacking from a “side view” ....
Outline

• Example: Reference-free voltage sensor
• Understanding computational loads
• Asynchronous circuits as voltage controlled oscillators (VCO)
• Discharging a capacitor via a VCO – VCO as a switched capacitor circuit!
• Stacking VCOs for capacitor discharge: theory and experiments
• Stacking VCOs for DC voltage sources
• Applications:
  • Frequency mirrors
  • PWM control
Power efficiency and regularity

- Modern systems rely on highly regular (periodic) power sources – they “invest” some power into power regulation.
- Future systems will have to operate in a wide dynamic range, paying the price in efficiency in a particular band.

We have to learn how to compute from unregulated power sources.
Traditional vs energy-modulated view

Activity-controlled impedance (potentiometer) vs Voltage-controlled oscillator.
Example: Reference-free voltage sensor
Reference-free voltage sensing

• Voltage sensor requiring only timing reference

Apparatus and method for voltage sensing, Newcastle University, GB Patent Number 2479156, 30 March 2010.
Self-timed counter
Output count and energy consumption

\[ C_{\text{sample}} = 10 \text{nF} \]
But the curious thing was this discharge:

It didn’t look exponential at all!

So, what was it?
What is Computational Load?

- Use a capacitor as an elementary finite energy storage, and a ring-oscillator to serve as a digital circuit load.
- The Ring-oscillator can closely mimic the switching behaviour of many closed loop self-timed circuits.
Circuit model

It’s a switched capacitor model.

Three states, 1->2->3 are repeated, where the role of Cp is played by every new inverter’s output cap.
Circuit Model: switching process

Charge equilibrium can be applied:

\[ V_1 = V_0 \frac{C}{C + C_l} \]

\[ K = \frac{C}{C + C_l} \]

\[ V = K^n V_0 \]

\[ V_N = K^n \]

Realistic value of \( K \): \( K \approx 1 \), say 0.99, as \( C_l \ll C \)
Solution for Super-threshold

A valid assumption: in super-threshold region we can assume that the propagation delay is inversely proportional to the voltage, so we have:

Using sum of geometric progression, we can find the solution relating $V$ and $t$

<table>
<thead>
<tr>
<th>Switching index</th>
<th>$V_N$</th>
<th>$t_s = \frac{A}{V}$</th>
<th>Physical time ($t$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>$K^0$</td>
<td>$\frac{A}{K^0}$</td>
<td>$\frac{A}{K^0}$</td>
</tr>
<tr>
<td>1</td>
<td>$K^{-1}$</td>
<td>$\frac{A}{K^1}$</td>
<td>$\frac{A}{K^0} + \frac{A}{K^1}$</td>
</tr>
<tr>
<td>2</td>
<td>$K^{-2}$</td>
<td>$\frac{A}{K^2}$</td>
<td>$\frac{A}{K^0} + \frac{A}{K^1} + \frac{A}{K^2}$</td>
</tr>
<tr>
<td>...</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$n$</td>
<td>$K^{-n}$</td>
<td>$\frac{A}{K^n}$</td>
<td>$\sum_{j=0}^{n} \frac{A}{K^j}$</td>
</tr>
</tbody>
</table>
Solution for Super-threshold

\[ V_N = \frac{AK}{t(1 - K) + AK} \]

Hyperbolic function of time

For super capacitor $K \approx 1$

Realistic value of $K \lesssim 1$
More accurate solution for Super-threshold

A general model of gate delay propagation [1] is used:

\[
\begin{align*}
    t_p &= \begin{cases} 
    t_{p1} = \frac{pc_1V}{(V-V_{TH})^\alpha} \\
    t_{p2} = \frac{pc_1V}{V-V_{TH}} \left( \frac{1}{I_0 e^{N_s}} \right)
    \end{cases}
\end{align*}
\]

Assuming \( \alpha = 1.3 \)

\[
\int_0^n \frac{AK^i}{(K^i-V_{THN})^\alpha} di = V_{THN} + \left( \frac{-10A}{3 \ln K \cdot (t - B \cdot A)} \right)^{3.33}, B = \left( \frac{10}{3 \ln K \cdot (1-V_{THN})^0.3} \right)
\]

Analysis of hyperbolic decays

• For super-threshold and $\alpha=2$:

$$V_N = \frac{AK}{(1-K)t + AK} = \frac{1}{at + 1};$$

where $A = 2pC$ and $a = \frac{1-K}{AK}$; $a$ is a decay rate – an important parameter!

(cf. “inverse of time constant”)

• For arbitrary $\alpha$:

$$V_N = \frac{1}{(at+1)^{1/(\alpha-1)}} \text{ and } a = \frac{1-K^{\alpha-1}}{AK^{\alpha-1}}$$

• Differential equation:

$$\frac{dV}{dt} = -aV^\alpha; \text{ for } \alpha=2, \text{ we can see that } \frac{dV}{dt} = \frac{-a}{(at+1)^2} = -aV^2$$

The oscillator is a voltage (and time)-varying resistor:

$$R(V) = \frac{2p}{V} \text{ or } R(t) = 2p(at + 1)$$
Analysis of hyperbolic decay rates

• For stack and parallel configurations we then apply Kirchhoff’s laws (KVL and KCL), based on:

\[ i_c = C \frac{dV_c}{dt} = -aCV_c^\alpha \]

• For stack:

\[
\begin{cases}
V = V_1 + V_2 \\
\frac{dV}{dt} = C_1 \frac{dV_1}{dt} = C_2 \frac{dV_2}{dt}
\end{cases}
\]

And since \( C = C_1 = C_2 \)

\[
\begin{cases}
V = V_1 + V_2 \\
aV^\alpha = a_1V_1^\alpha = a_2V_2^\alpha
\end{cases}
\]

We have: \( \left( \frac{1}{a} \right)^\alpha = \left( \frac{1}{a_1} \right)^\alpha + \left( \frac{1}{a_2} \right)^\alpha \)
Analysis of hyperbolic decay rates

• For stack:

\[
\left( \frac{1}{a} \right)^{\frac{1}{\alpha}} = \left( \frac{1}{a_1} \right)^{\frac{1}{\alpha}} + \left( \frac{1}{a_2} \right)^{\frac{1}{\alpha}} \quad \text{or} \quad a = \frac{a_1 a_2}{(\sqrt{\alpha a_1} + \sqrt{\alpha a_2})^\alpha}
\]

• For parallel: \( a = a_1 + a_2 \)

• Confirmed by physical experiments with discrete CMOS components:
  
  • The value of alpha is 1.5
  
  • The discharging process for a stack of two identical circuits is nearly 3 times slower than for a standalone circuit
By the way ..... 

• For stack:

\[
(\frac{1}{a})^{\frac{1}{\alpha}} = (\frac{1}{a_1})^{\frac{1}{\alpha}} + (\frac{1}{a_2})^{\frac{1}{\alpha}} \quad \text{or}
\]

\[
a = \frac{a_1 a_2}{(\sqrt[\alpha]{a_1} + \sqrt[\alpha]{a_2})^\alpha}
\]

For \( \alpha = 2 \):

\[
(\frac{1}{a})^{\frac{1}{2}} = (\frac{1}{a_1})^{\frac{1}{2}} + (\frac{1}{a_2})^{\frac{1}{2}} \quad \text{or}
\]

\[
a = \frac{a_1 a_2}{(\sqrt{a_1} + \sqrt{a_2})^2}
\]

Series (stack): discharge rate follows the law of the inverse Pythagorean!
Capacitor discharge experiments

Standalone

Stack

Parallel
More details can be found in:


Including:

• Derivations of the main theoretical results,
• Analysis of charge sharing modes due to partial overlap of switching in the top and bottom of the stack,
• Simulations and physical experiments using discrete components, and comparisons between experimental and theoretical predictions, as well as
• Experimental measurement of the alpha-parameter, which was around 1.5
Stacking Voltage-Controlled Oscillators in DC powered circuits: Analysis and Application
Stack connection of two ring oscillators

- We are talking about DC, i.e. about average value of $V_f$ in steady state
- In practice due to short-circuit currents $V_f$ is close to $0.5V_{in}$ and does not depend on the number of inverters
Model of an inverter

Topologies of the ring oscillator

The model does not take into account short circuit current and leakage

The capacitance of $C_t = C_p (n - 1)/2$ increases with increase of the number of inverters, $n$
Reminder: 
Circuit model with the discharging cap

This is a model of a circuit with constantly switching capacitors!
The role of a switched cap $C_p$ is played by every inverter in turn.
So in the equivalent switching cap circuit $C_p$ is an “effective switching cap”
The effective impedance of the circuit becomes

$$R_{switch} = \frac{1}{f_{switch}C_p}$$

where $f_{switch} = 1/2 \ t_{su}$, $t_{su}$ is propagation delay of an inverter
Externally clocked stack

Muller C-element: \( y = x_1 x_2 + (x_1 + x_2)y \)

- After some transient the system will reach steady-state defined by

\[
R_s = \frac{1}{f_s C_p} ; \quad R_o = \frac{1}{f_o C_p} ; \quad \frac{V_f}{V_{in} - V_f} = \frac{R_o}{R_s} = \frac{f_s}{f_o}
\]
Possible applications

• Stack with a binary tree of inverters that allows adjusting $V_f$

• Cascade of two clocked stacks (frequency mirror) that decouples the control frequency from the ground.
Main Effects in the Proposed Circuit

• Transient, caused by the frequency change and followed by stabilization via the internal feedback “voltage–frequency–impedance–voltage”

• Steady state with some ripple, whose level depends on how the oscillators interact and on how well the products of this interaction are averaged
Application: Pulse Width Modulation (PWM)

- The general purpose of PWM is to control power delivery

Example: step-down (buck) converter

Duty cycle: \( D = \frac{T_{on}}{T_{off}} \)

\( V_o = D V_{in} \)
Frequency controlled PWM circuit

The idea is analogous to current-starved PWM control from:


- Since we control the impedances, the transfer function will be nonlinear
- Let the initial state of the output be logical “1”
- Denote the propagation delays of odd and even inverters by $t_{su1}$ and $t_{su2}$ respectively, then

\[
\begin{align*}
    t_{on} &= (n - 1)t_{su2} \\
    t_{off} &= (n + 1)t_{su1}
\end{align*}
\]

Controlled by even inverters (i.e. by $f_2$)
Controlled by odd inverters (i.e. by $f_1$)
Deriving the transfer function

- In a distinctive super-threshold region the propagation delay of an inverter is:
  \[ t_{su} = \frac{pC_p V_{dd}}{(V_{dd} - V_{th})^\alpha} \]

- Assuming \( \alpha = 2 \) and \( V_{th} \ll V_{dd} \), we approximate
  \[ t_{su} \approx \frac{k}{V_{dd}} \]

  \[ t_{on} = (n - 1)t_{su2}; \quad t_{off} = (n + 1)t_{su1} \]

  \[ f_o = \frac{1}{t_{on} + t_{off}} = \frac{V_1V_2}{k[(n - 1)V_1 + (n + 1)V_2]} \]

  \[ D = t_{on}f_o = \frac{(n - 1)V_1}{(n - 1)V_1 + (n + 1)V_2} \]

- It is evident that \( f_o \) depends on \( k \approx V_{dd}t_{su} \), which should be found experimentally
Deriving the transfer function

\[ D = \frac{(n-1)V_1}{(n-1)V_1 + (n+1)V_2} \]

- In the case of \( V_1 = V_2 \)
  \[ D = \frac{n-1}{2n} \text{ and tends to } 0.5 \text{ for } n \to \infty \]

- The condition of \( V_1 = V_2 \) also allows us to write
  \[ \frac{V_1}{V_{in} - V_1} = \frac{V_2}{V_{in} - V_2} = \frac{f_s}{f_o}; \quad f_s = \frac{2nf_1}{n+1} = \frac{2nf_2}{n-1} \]
  such that
  \[ V_1 = \frac{2nf_1V_{in}}{2nf_1 + (n+1)f_o}; \quad V_2 = \frac{2nf_2V_{in}}{2nf_2 + (n-1)f_o} \]
Deriving the transfer function

Substituting

\[
V_1 = \frac{2nf_1V_{in}}{2nf_1 + (n + 1)f_0}
\]

\[
V_2 = \frac{2nf_2V_{in}}{2nf_2 + (n - 1)f_0}
\]

into

\[
f_o = \frac{V_1V_2}{k[(n-1)V_1 + (n + 1)V_2]}
\]

\[
D = \frac{(n-1)V_1}{(n-1)V_1 + (n + 1)V_2}
\]

we obtain a \textit{quadratic equation for the switching frequency}

\[
f_o^2 + pf_o - q = 0
\]

where

\[
p = \frac{4n^2f_1f_2}{(n-1)^2f_1 + (n + 1)^2f_2}; \quad q = \frac{2nf_1f_2V_{in}}{k[(n-1)^2f_1 + (n + 1)^2f_2]}
\]

and the duty cycle depends on \(f_o\) as

\[
D = \frac{(n-1)^2f_1f_0 + 2n(n-1)f_1f_2}{[(n-1)^2f_1 + (n + 1)^2f_2]f_0 + 4n^2f_1f_2}
\]
Keeping the output frequency constant

- The disadvantage of the considered circuit is that changing $D$, we change $f_o$
- Let $f_o = \text{const}$ and express $f_2$ through $f_1$

$$f_2(f_1) = \frac{k(n - 1)^2 f_o^2 f_1}{2n(V_{in} - 2knf_o)f_1 - k(n + 1)^2 f_o^2}; \quad D(f_1) = \frac{2n(V_{in} - (n + 1)kf_o)f_1 - (n + 1)^2 f_o^2}{2n(V_{in} - 2kf_o)f_1 - 2(n + 1)kf_o^2}$$

\[ f_o = 50kHz \]
Simulation Results

\[ t_{su} = \frac{pC_p V_{dd}}{(V_{dd} - V_{th})^\alpha} \]

\[ t_{su} \approx \frac{k}{V_{dd}} \]

- To provide \( \alpha \approx 2 \) and \( V_{dd} \gg V_{th} \) we used the standard CMOS inverter 74LVC04 with \( V_{in} = 9V \)
- To provide high switching speed, we used the so-called static C-element
- Each of the C-elements is connected to one inverter, while the footer consists of \( n = 11 \) inverters
Simulation Results

- Stabilization of the voltages for $f_1 = 64\, kHz$ and $f_2 = 32\, kHz$

\[ C_1 = C_2 = 0.1\mu F \]

- To calculate the values of $f_o$ and $D$, we need to find $k$

\[ k = \frac{V_{in}}{\left[(n + \frac{1}{n})\frac{f_o}{f} + 2n\right]f_o} \]

where $f = f_1 = f_2$ is the control frequency

$\bf{k} = 3.9 \times 10^{-6}$

$\bf{f_o} = 50\, kHz$
Simulation Results

Output frequency and duty cycle as a function of two equal control frequencies

Dashed line: calculated as a solution of
\[ f_o^2 + pf_o - q = 0 \]

Dashed line: calculated by
\[ D = \frac{(n - 1)^2 f_1 f_o + 2n(n - 1)f_1 f_2}{[(n - 1)^2 f_1 + (n + 1)^2 f_2]f_o + 4n^2 f_1 f_2} \]

Maximum discrepancy \( \approx 13.5\% \)

Maximum discrepancy \( \approx 4.7\% \)
Simulation Results

Output frequency and duty cycle as a function of two different control frequencies

• Both of the surfaces are built using a set of theoretically calculated points
Conclusions

- In capacitor-powered systems asynchronous load causes hyperbolic (rather than exponential!) discharge – it is much slower than exponential.
- Stacking in series allows to extend the life-time at the cost of greater delay.
- Stack of two ring oscillators is a self-adjusting system.
- Large filter capacitances make the interaction between oscillators weak and defined as the ratios of their quasi-static impedances.
- To keep the output frequency of the PWM circuit constant we need to adjust one of the control frequencies.
- It would be advantageous to have inverting elements with delay strictly reciprocal to $V_{dd}$.
- An interesting direction is to develop frequency insensitive computational elements, where the information is represented by duty cycle (phase) – we have built a perceptron based on PWM (paper at DATE 2019 and Royal Soc Transactions, under review).
Acknowledgements and references

This work was done with active involvement of:

Alexander Kushnerov (formerly: BGU, Israel, NCKU, Taiwan and Intel Israel),
Andrey Mokhov (Jane Street and Newcastle University),
Reza Ramezani (formerly: Newcastle University, Pacific Microchip Corp.)

3) A. Kushnerov and A. Yakovlev, Stacking Voltage-Controlled Oscillators: Analysis and Application, 23rd IEEE International Conference on Electronics Circuits and Systems, 11-14 December, 2016, Monte Carlo, Monaco, IEEE, pp. 53-56. DOI: 10.1109/ICECS.2016.7841130
Thank you for your attention!