Newcastle University

Bridging Asynchronous Circuits and Mixed-Signal Design

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Nano-Network 2018, Tjome, 13th June 2018

Agenda

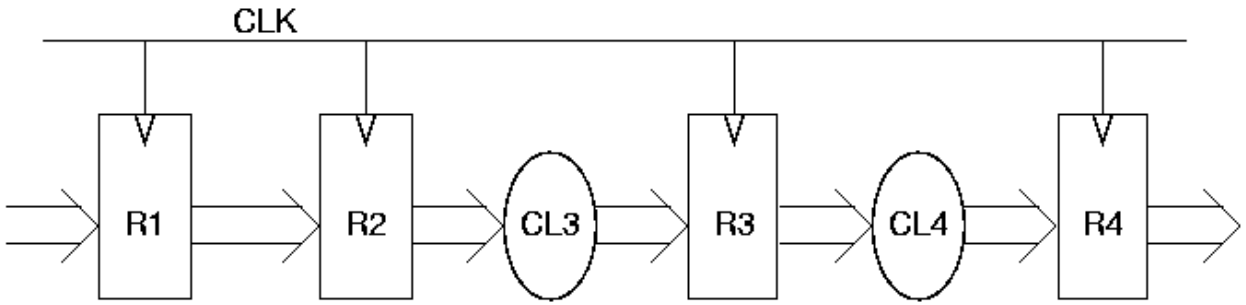
- What are Asynchronous (digital) Circuits?
- Why are Async circuits needed?
  - Tolerant to process variations
  - Tolerant to environmental variations
- Success and Obstacles with Async Design
- “Little digital”: Async design for Analog electronics
  - Design of Power converters
  - Tool Workcraft.org
- Messages and Open challenges

Asynchronous Behaviour

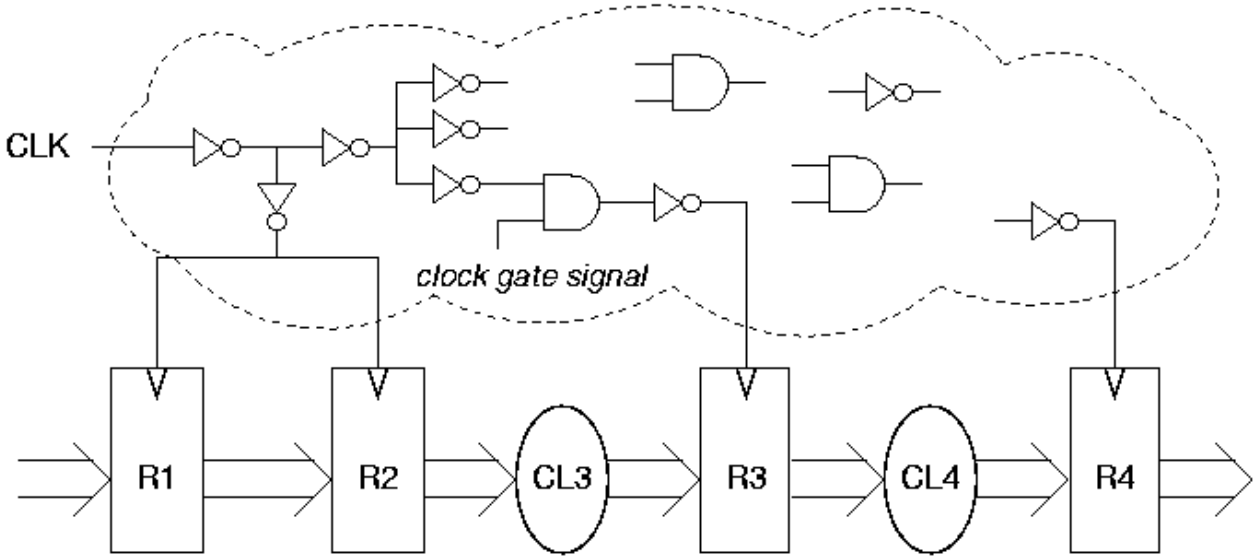
- Synchronous vs Asynchronous behaviour in general terms, examples:
  - Orchestra playing with vs without a conductor
  - Party of people having a set menu vs a la carte
- Synchronous means all parts of the system acting globally in tact, even if some or all part ‘do nothing’
- Asynchronous means parts of the system act on demand rather than on global clock tick
- Acting in computation and communication is, generally, changing the system state
- Synchrony and Asynchrony can be in found in CPUs, Memory, Communications, SoCs, NoCs etc.

Synchronous clocking

How we think

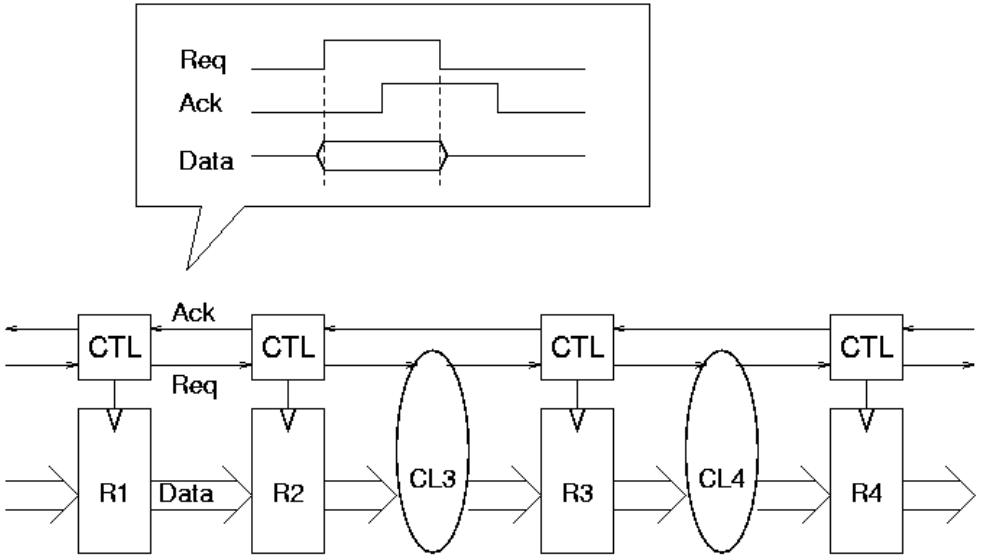


What we design

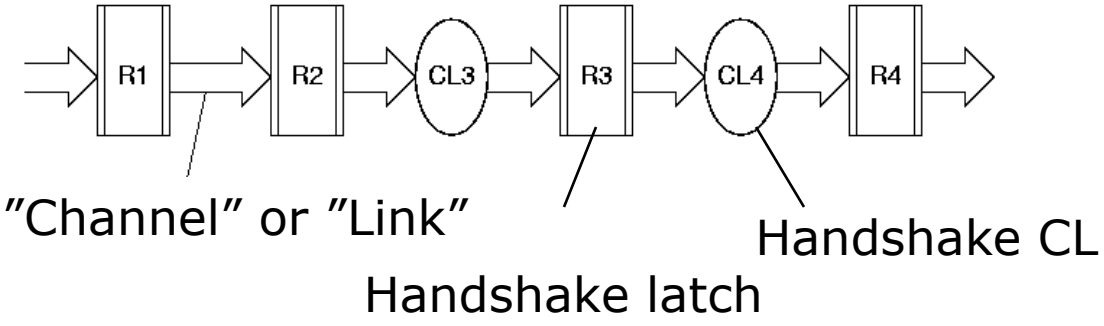


Asynchronous handshaking

What we design



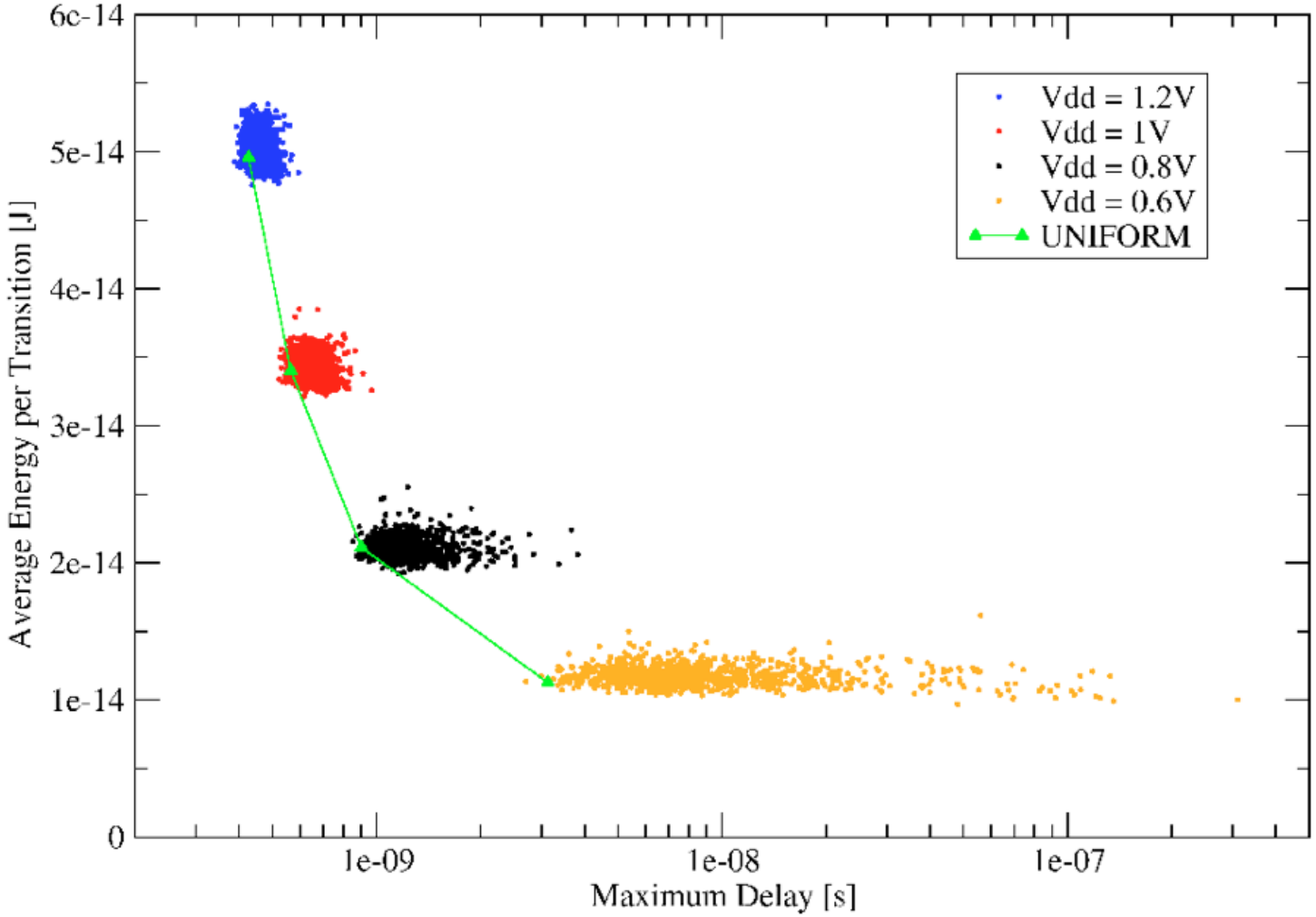
How we think



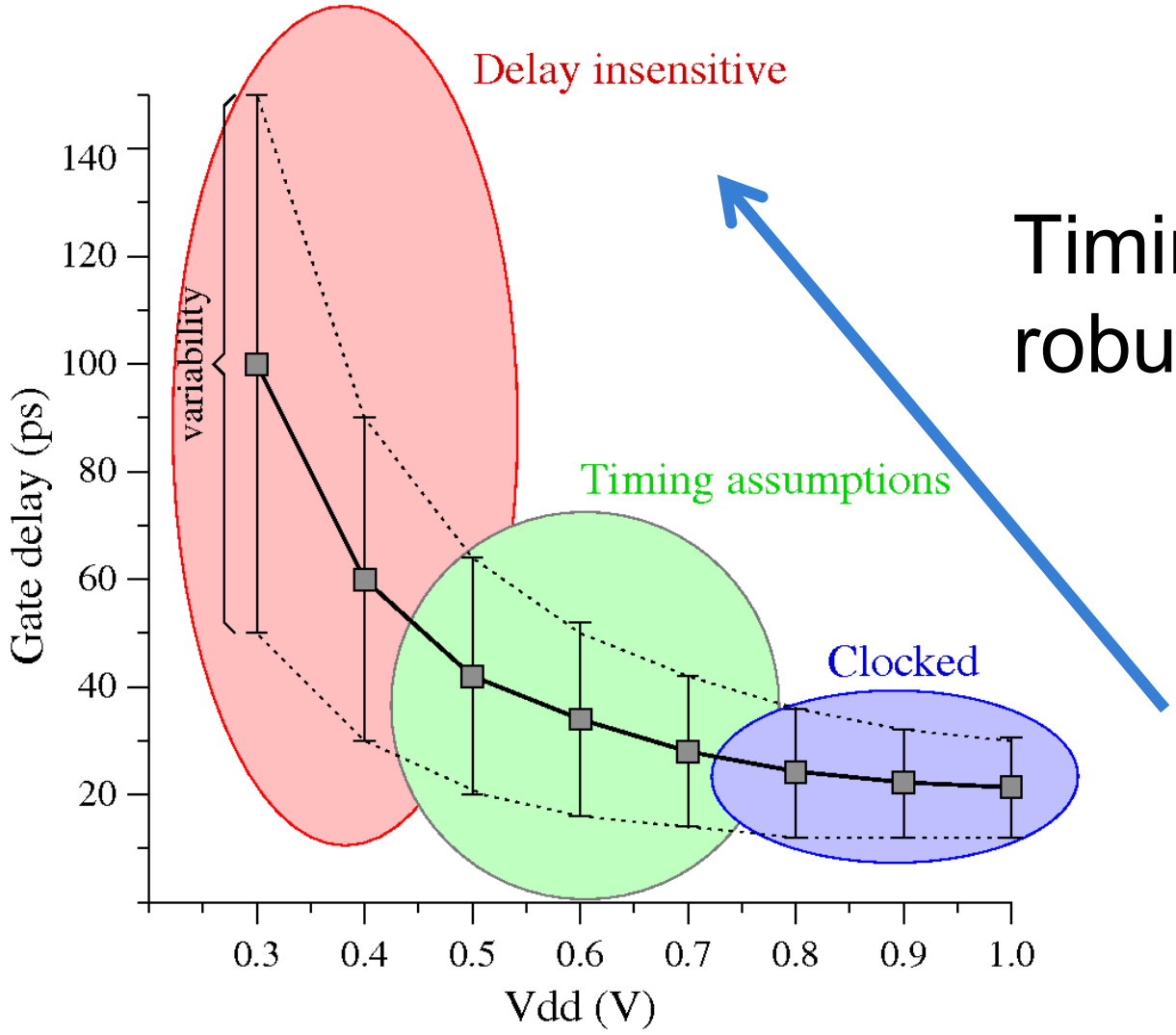
Tolerance to Process variations

Performance/energy/yield trade off

From Asenov,UKDF'10



Asynchronous to cope with uncertainty

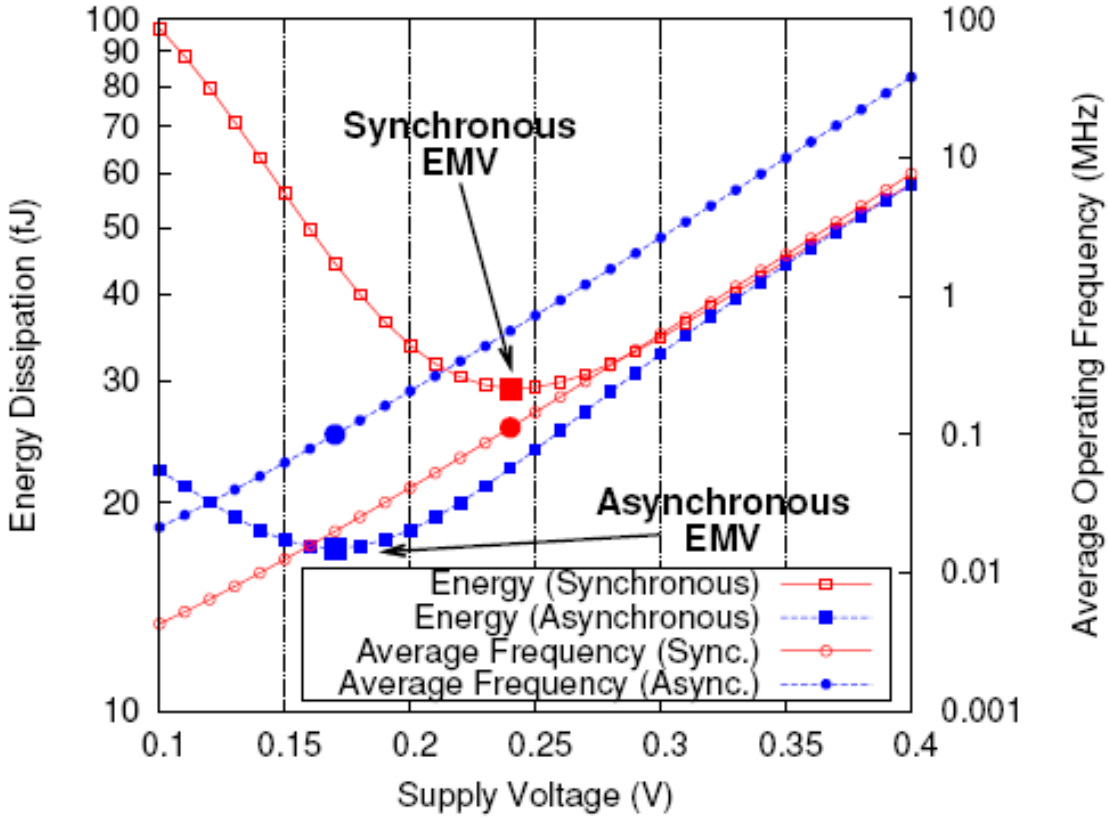


Timing robustness

Technology node: 90nm

Source of variability analysis: Yu Cao, Clark, L.T., 2007

Async for energy efficiency

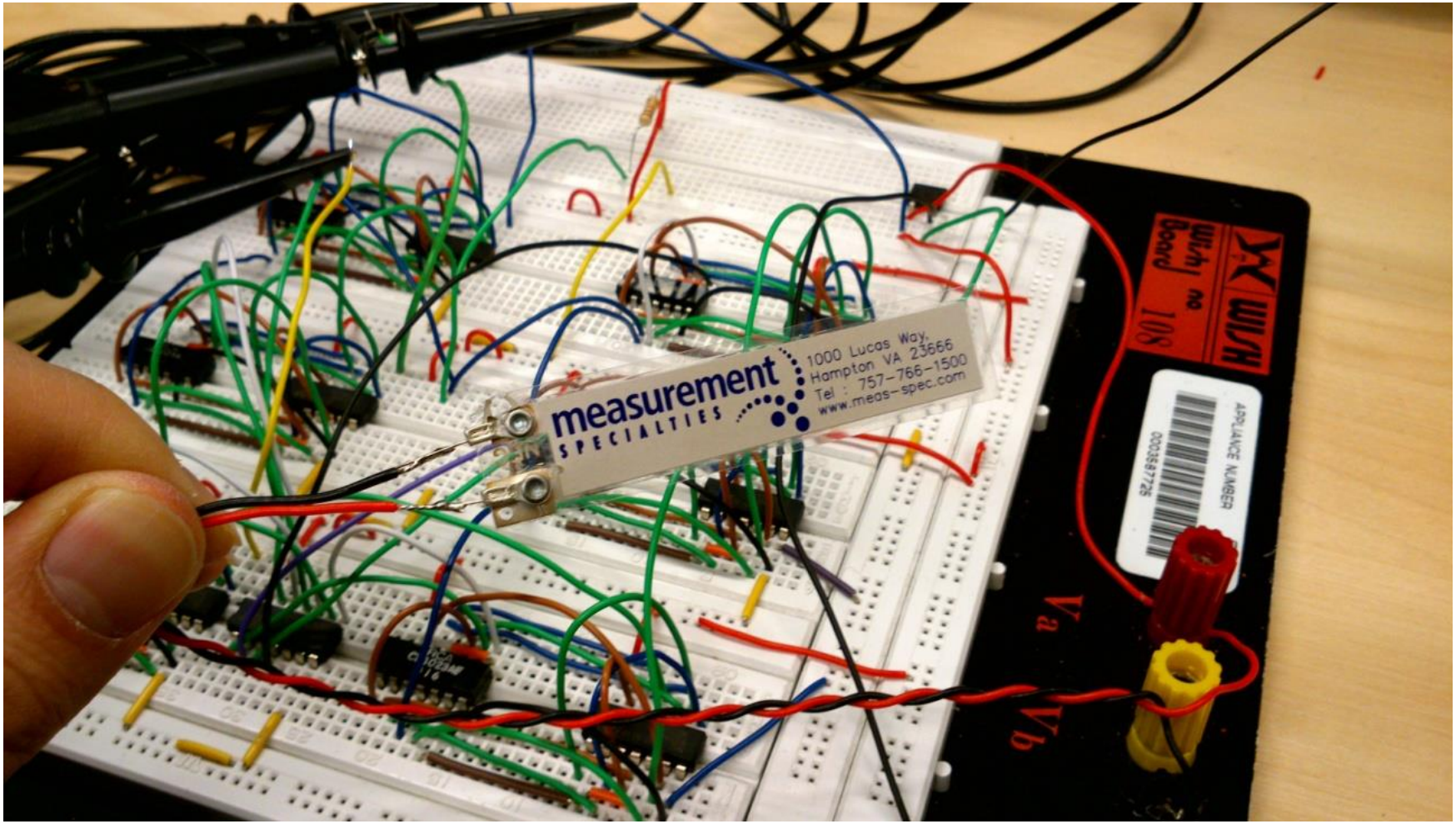


Asynchronous (self-timed) logic can provide completion detection and thus reduce the interval of leakage to minimum, thereby doing nothing well!

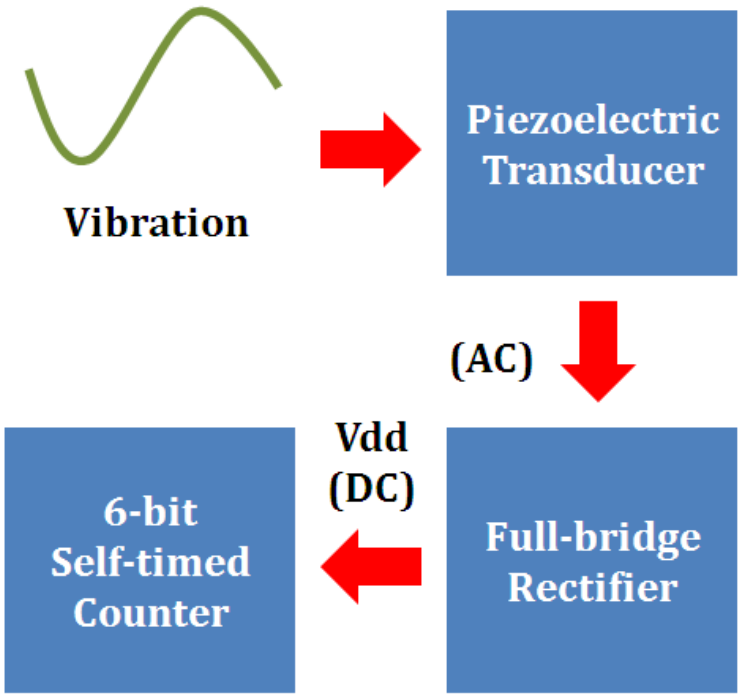
Source: Akgun et al, ASYNC'10

Tolerance to Environmental conditions

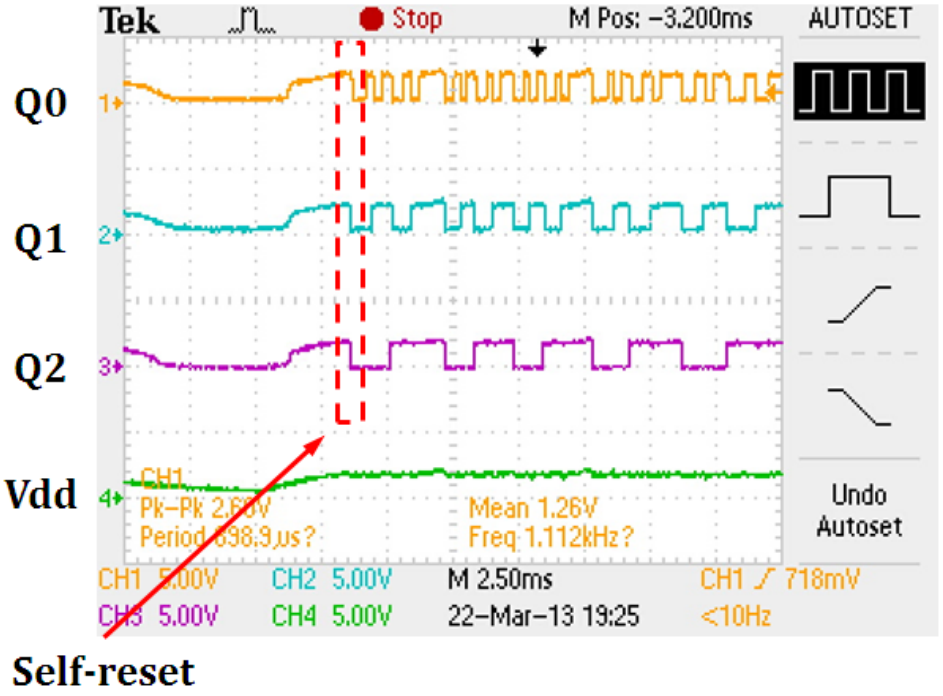
Piezo-Film Experiment



Piezo-experiment with asynchronous counter

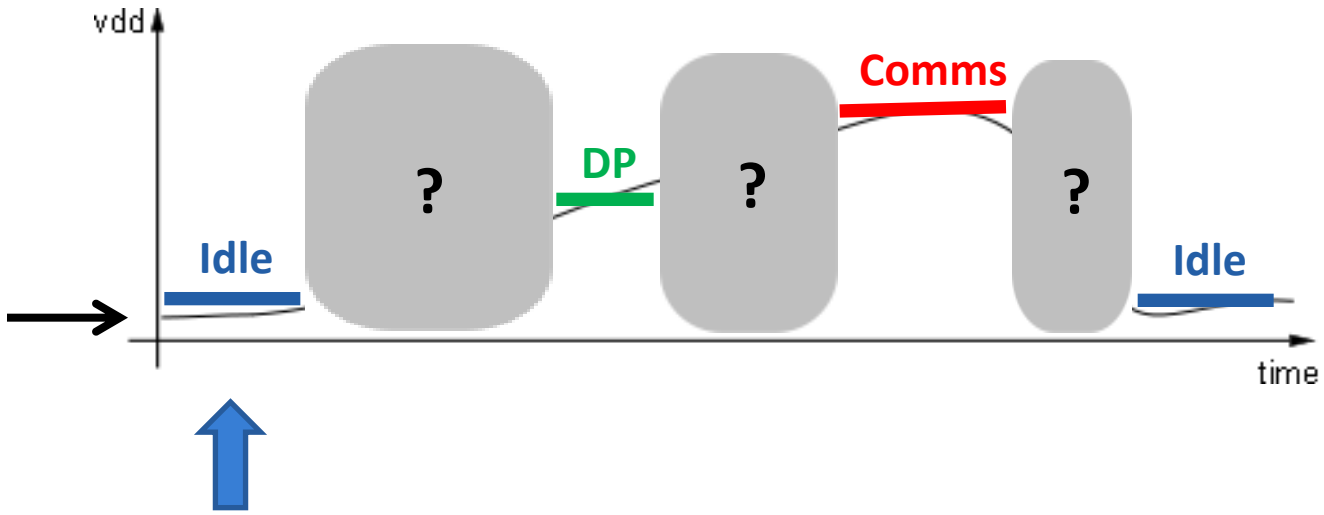


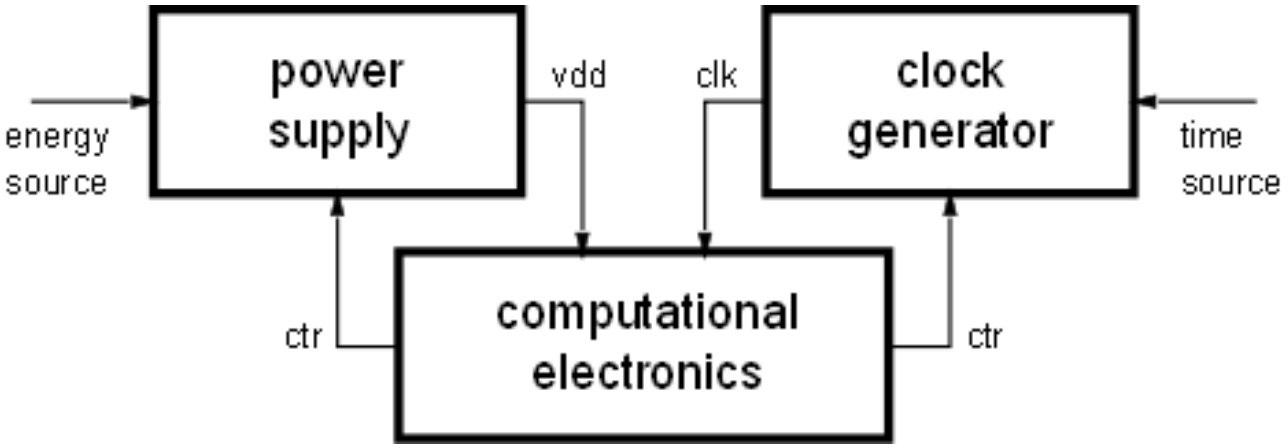
(A)



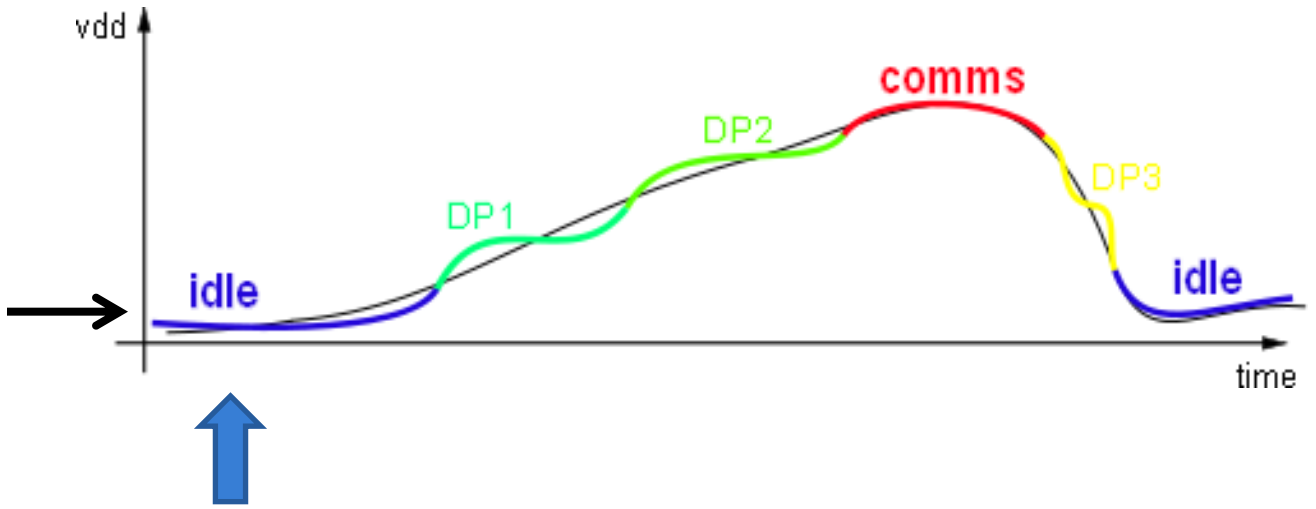
(B)

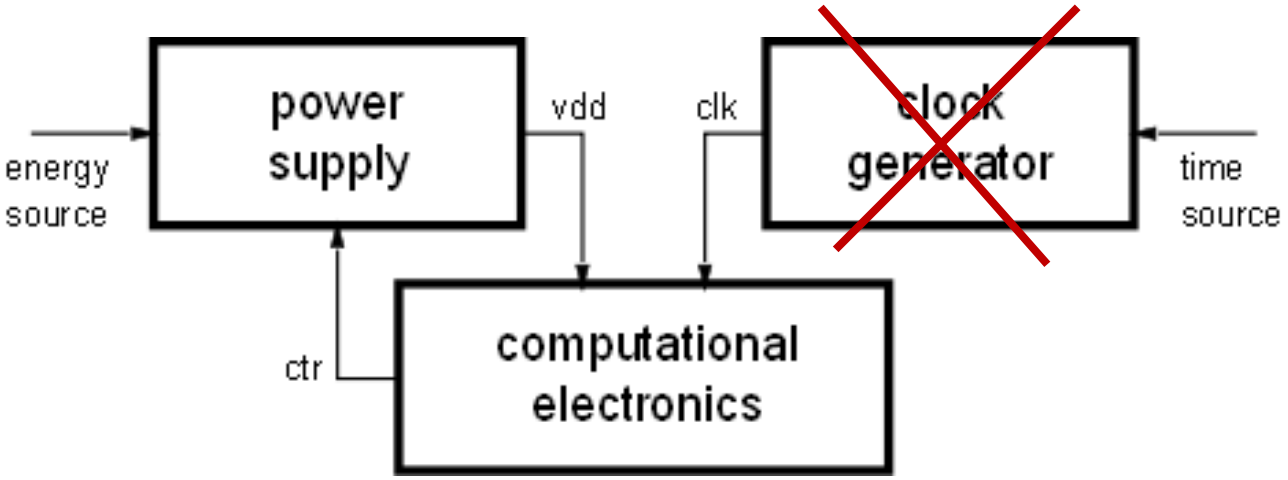
Traditional system





Energy-modulated system

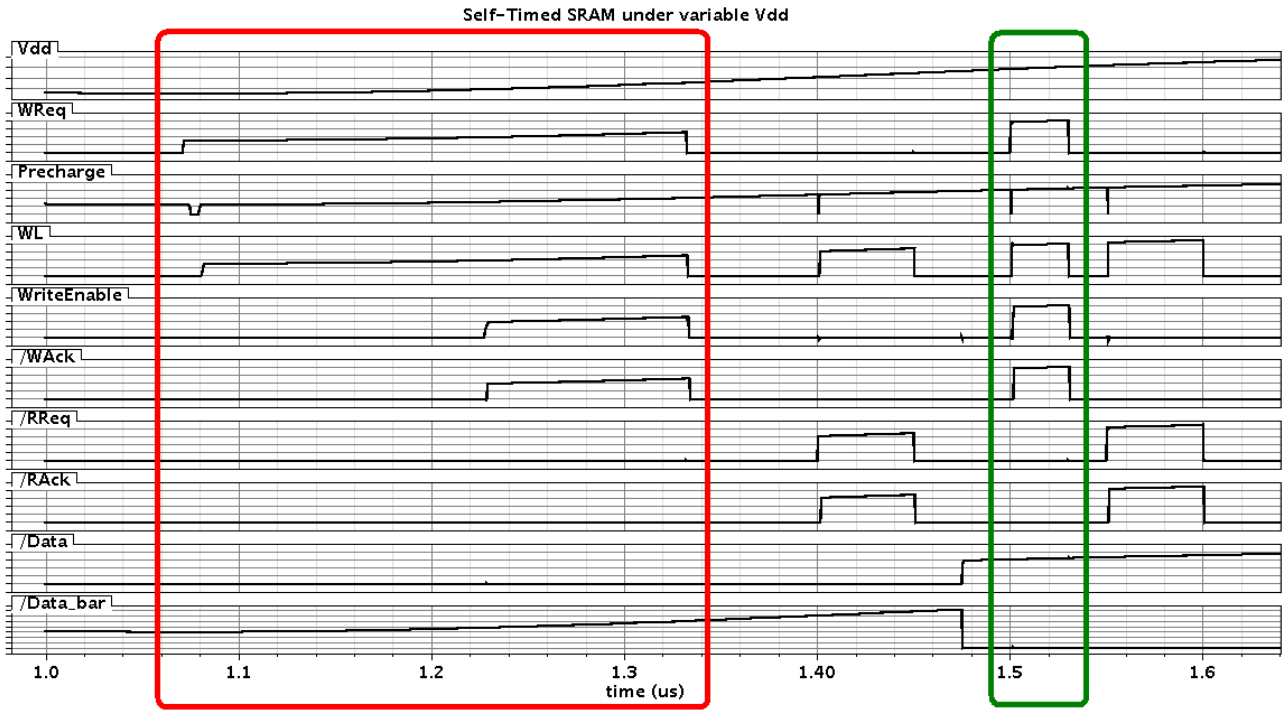




Async (digital) behaviour

- Triggered by events (e.g. level-crossing)
- Modelled by
  - cause-effect relations
  - token flow
  - handshakes
  - data-flow
- Power-driven timing
- Applications: interfacing, control, pipeline

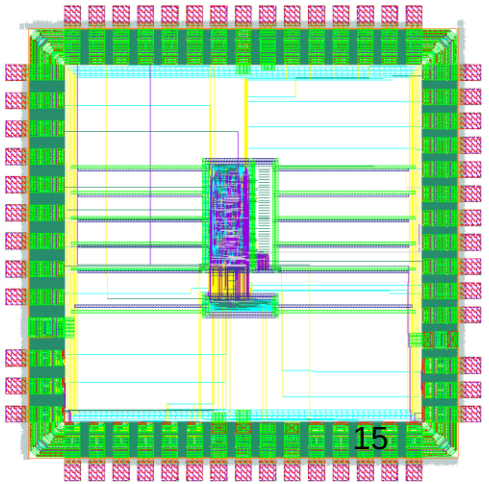
Example 1: speed-independent SRAM



Low Vdd – slow response

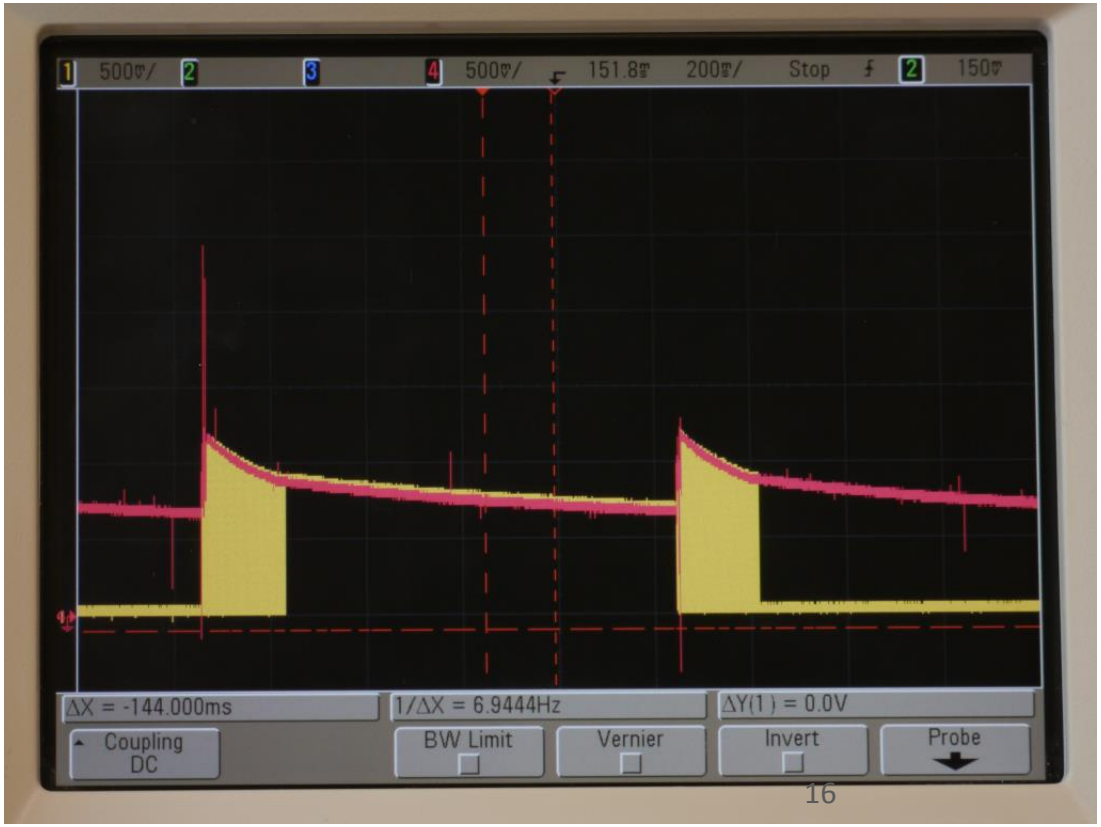
High Vdd – fast response

Self-timed SRAM chip: UMC CMOS 90nm



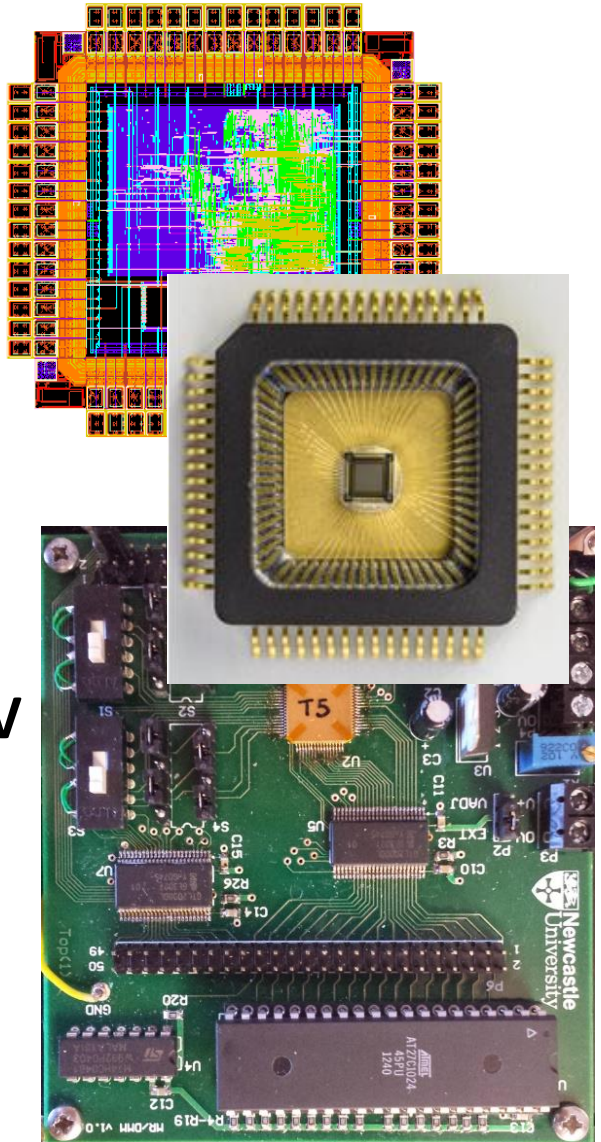
SRAM testing and results

- SRAM operations modulated by Vdd from a Capacitor Bank
- When Vdd goes below 0.75v, the ack signal is not generated by SRAM
- The circuit automatically wakes up when Vdd goes up



Example 2: Power-proportional CPU design (8051)

- CMOS 130nm CMP process, 2013
- 0.89V to 1.5V: full capability mode
- 0.74V to 0.89V: at 0.89V the RAM starts to fail, so the chip operates using
- 0.22V to 0.74V: at 0.74V the program counter starts to fail, however the control logic synthesised using the CPOG model continues to operate correctly down to 0.22V
- 67 MIPS at 1.2 V
- ~2700 instructions per second at 0.25V



So, if Asynchronous Design is so cool, why does mainstream industry not use it!?

Mainstream industry is Big Digital and has an "established Design Process" (with commercial tools for globally clocked designs)

$$$

Design Cost is the main factor!
TOOLS are a key!

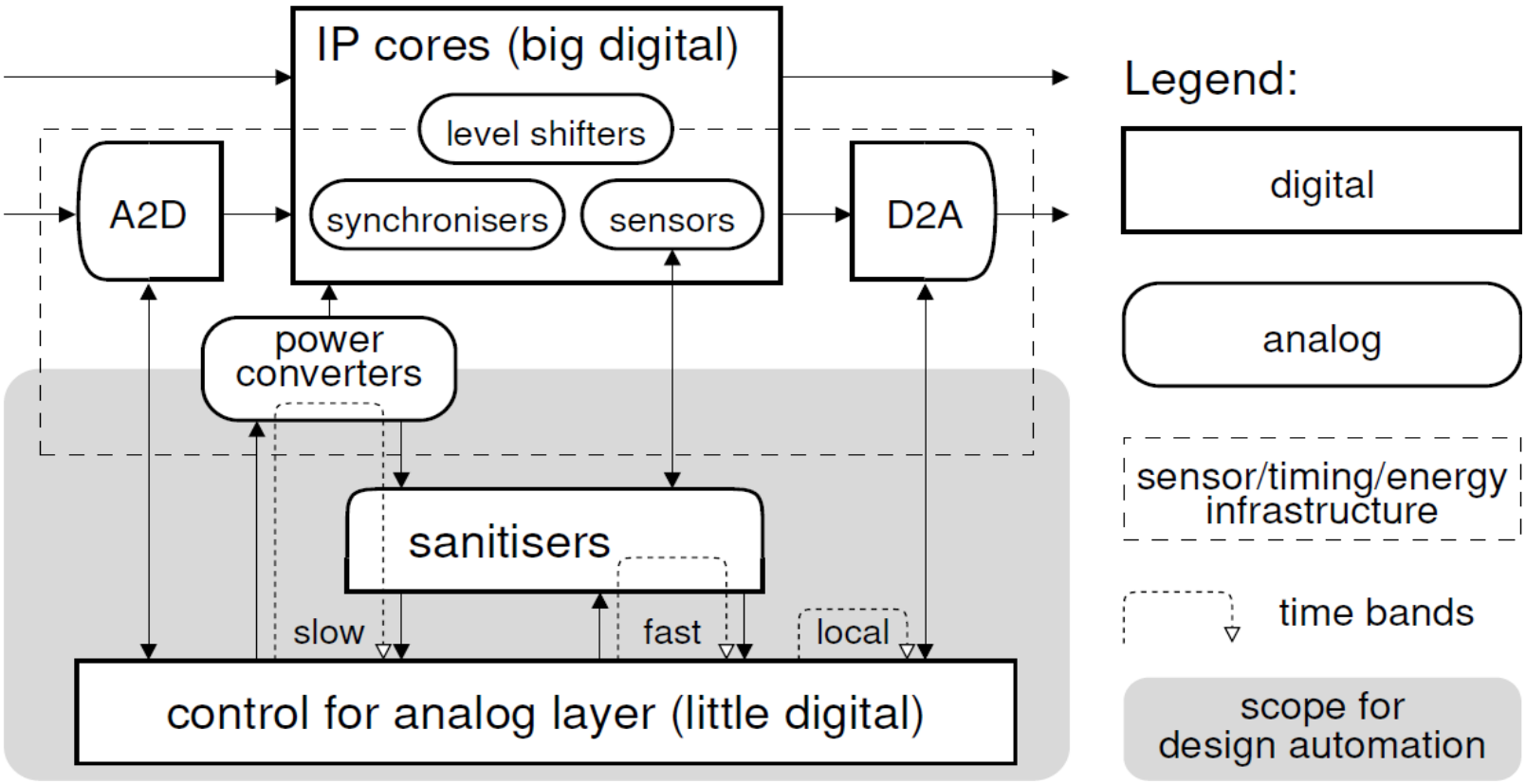
It’s hard to beat Synchronous Design for BIG Digital!

What about Analog-Mixed-Signal?

Motivation for Async for Analog

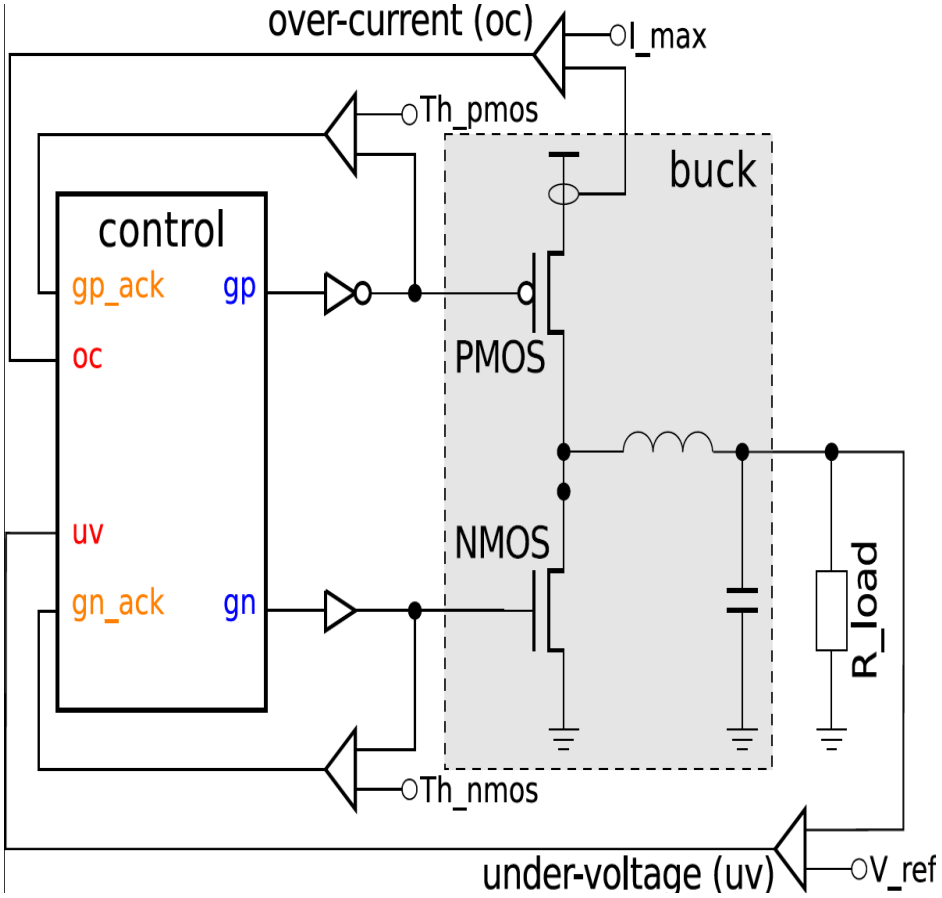
- **Analog and Mixed Signal (AMS) design becomes more complex:**
  - **More functionality**
  - **Move to deep submicron after all!**
- **According to Andrew Talbot from Intel (2016)** ***"transistors are very fast switches, netlists are huge, parasitics are phenomenally difficult to estimate, passives don't follow Moore's law, reliability is a brand new landscape"***

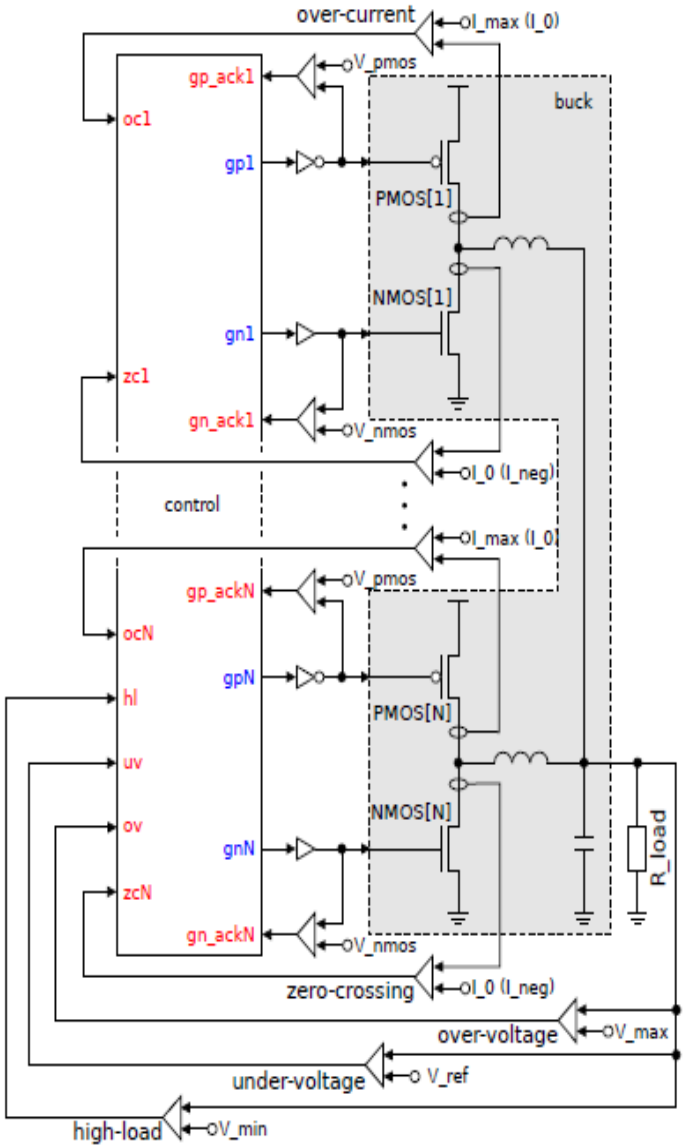
Emergence of little digital electronics



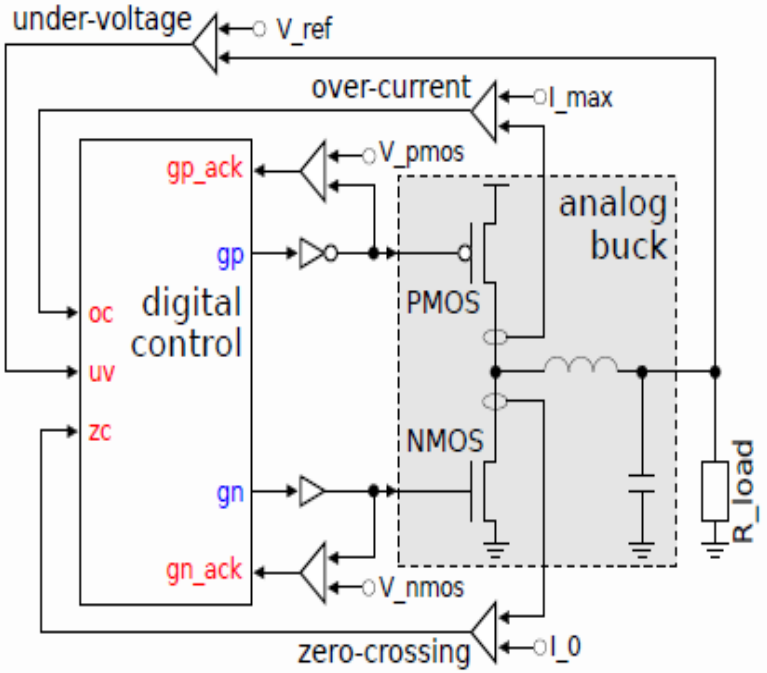
- **Analog and digital electronics are becoming more intertwined**
- **Analog domain becomes complex and needs digital control**

Example: Buck (DC-DC) converter control

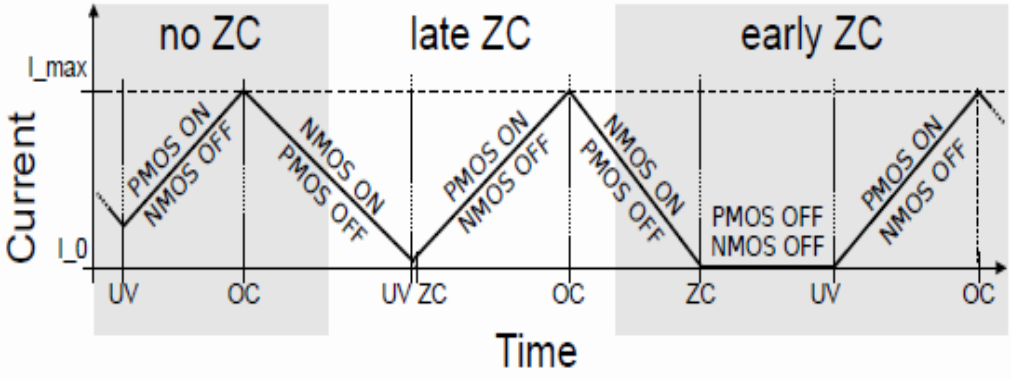




Example: Buck converter



Phase diagram specification:



Buck conditions:

- under-voltage (UV)
- over-current (OC)
- zero-crossing (ZC)

Operating modes:

- no zero-crossing
- late zero-crossing
- early zero-crossing

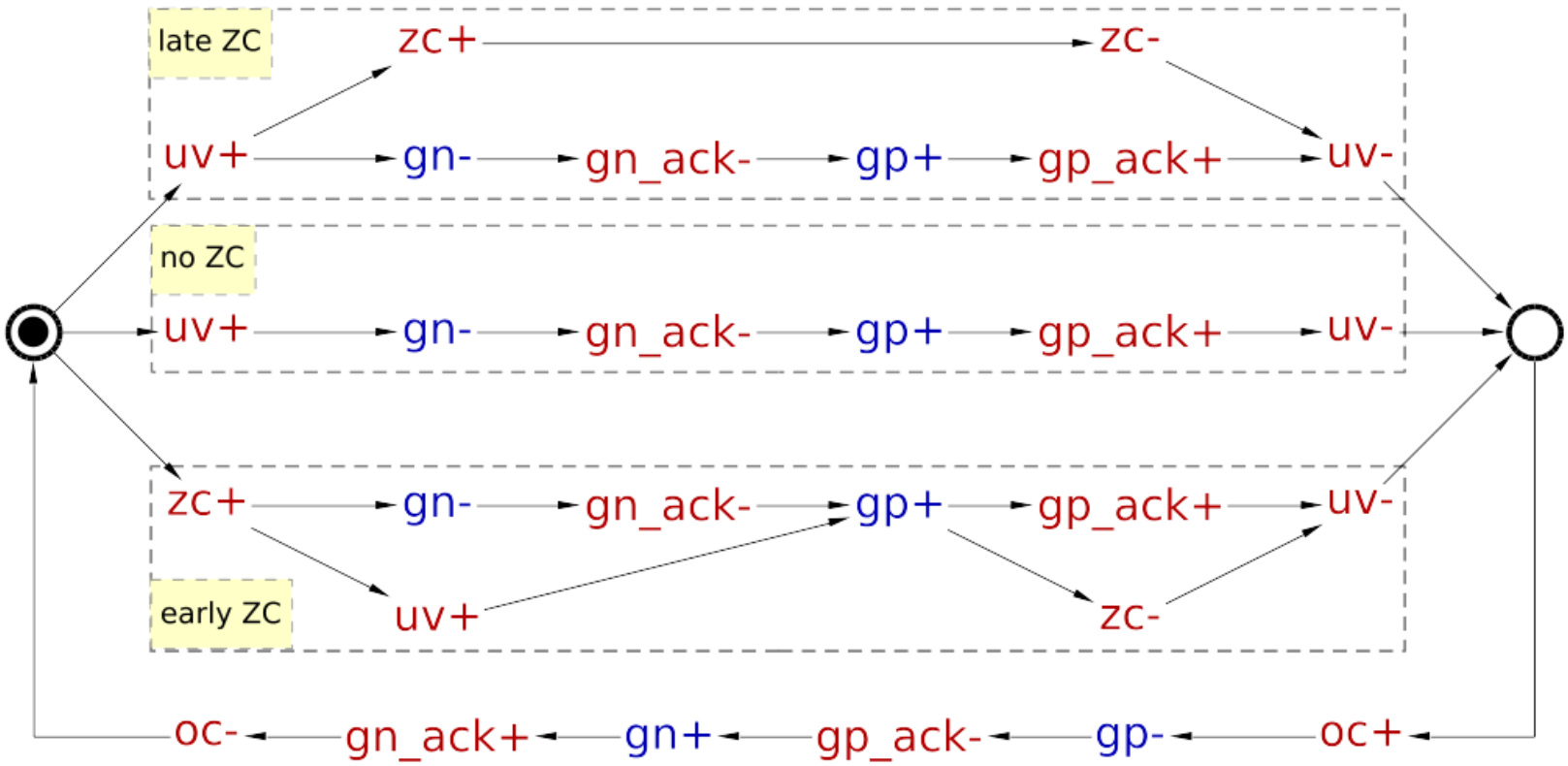
Building asynchronous circuits in Analog-Mixed Signal context requires extending traditional assumptions about speed-independence …

Starting point – a New Behaviour Capture Language:

Signal Transition Graph

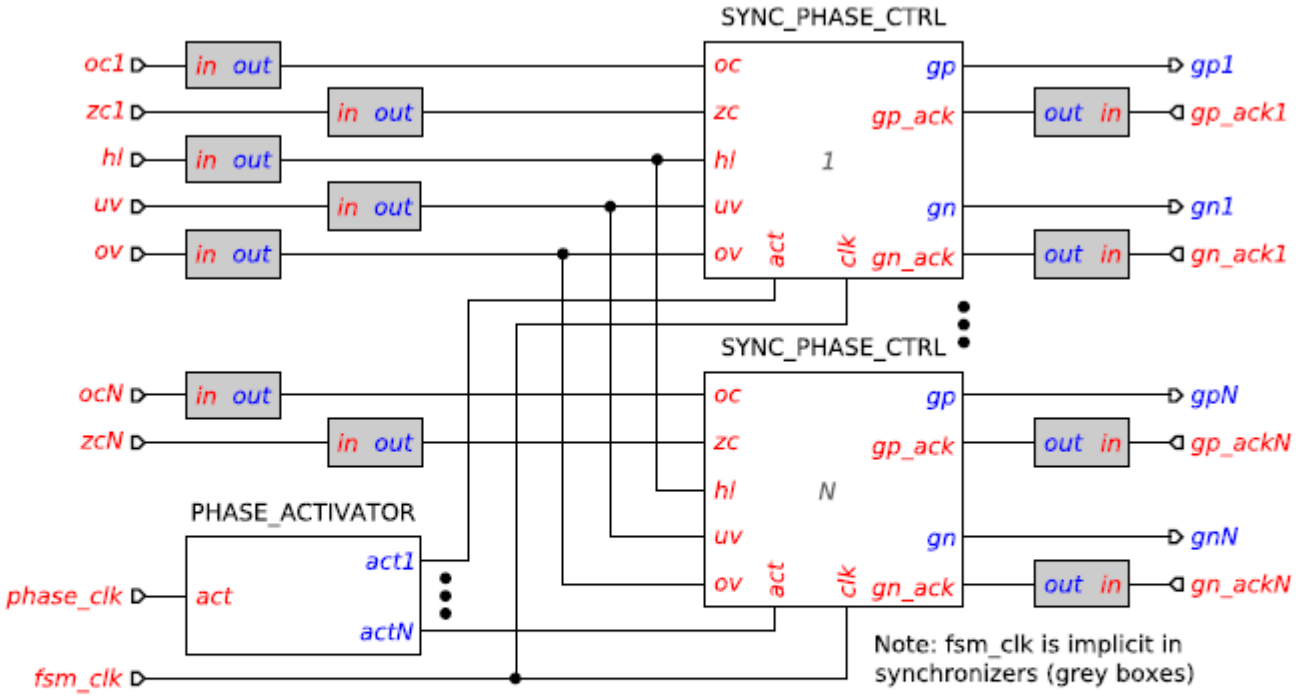
similar to
Traditional Waveforms
so easy to grasp by industry!

STG Specification of buck controller



Design Case Study: Multiphase Buck Converter Sync vs Async

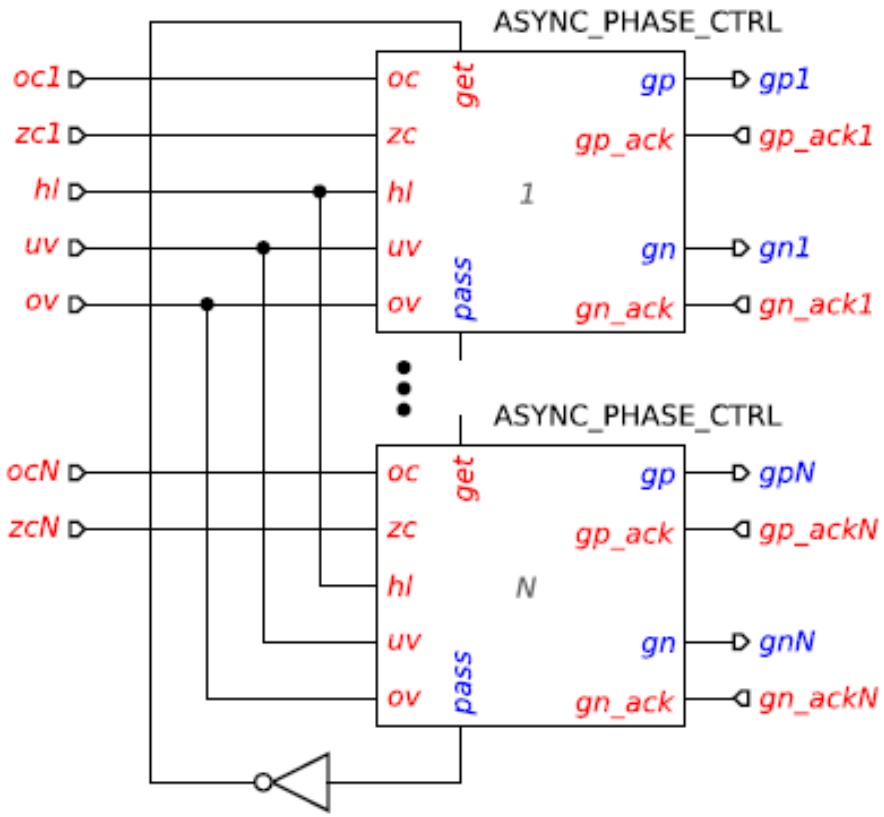
Multiphase Buck: Sync Control



- Two clocks: phase activation (slow) and sampling (fast)
- Need for multiple synchronizers (grey boxes) - latency & metastability
- Conventional RTL design flow

Multiphase Buck: Async Control

D. Sokolov, et al. DATE 2017

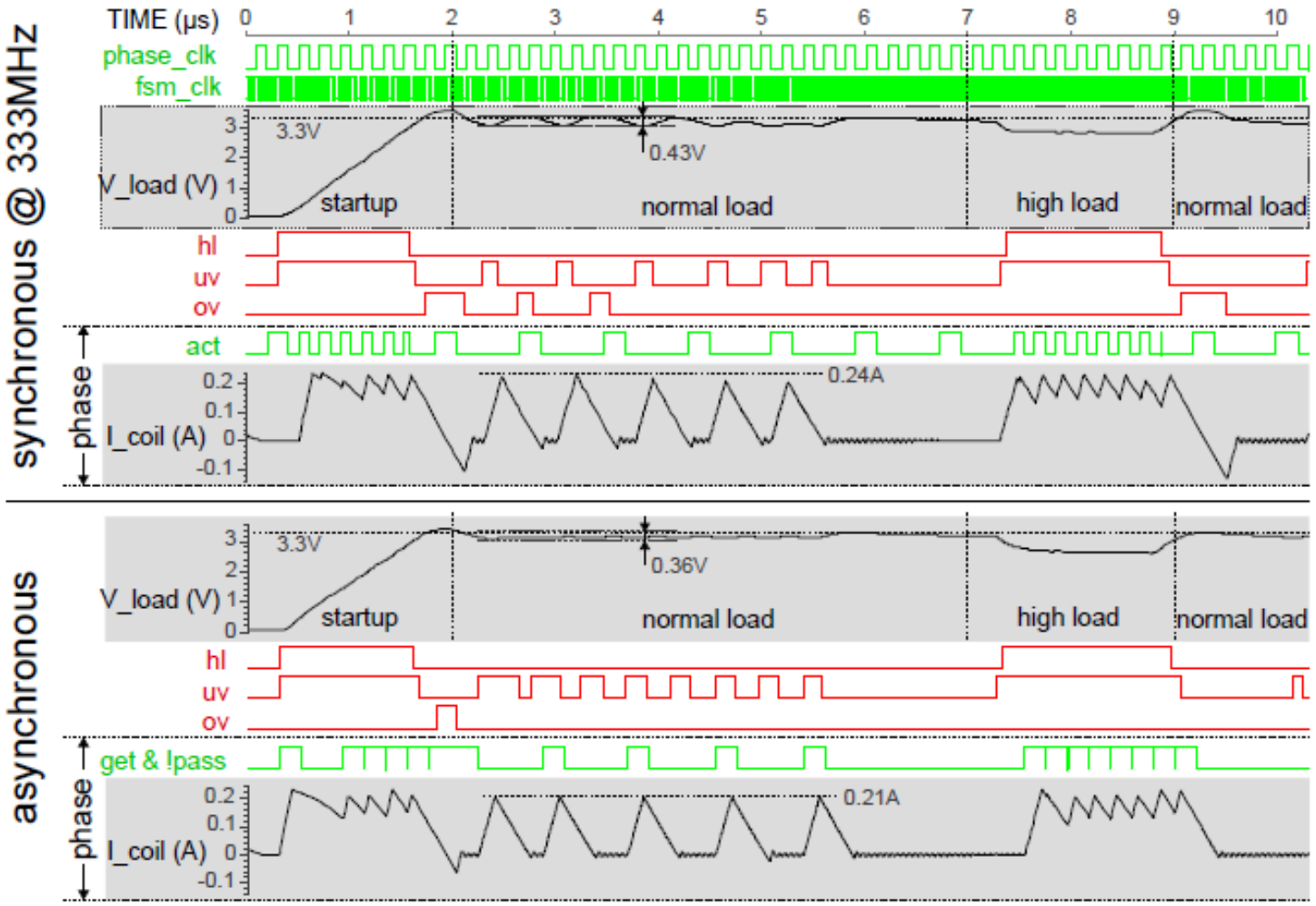


- Token ring architecture, no need for phase activation clock
- No need for synchronisers - all signals are asynchronous
- A4A design flow

Simulation results: Comparison

- Verilog-A model of the 3-phase buck
- Control implemented in TSMC 90nm
- AMS simulation in CADENCE NC-VERILOG
- Synchronous design
  - Phase activation clock – 5 MHz
  - Clocked FSM-based control – 100 MHz
  - Sampling and synchronisation
- Asynchronous design
  - Phase activation - token ring with 200 ns timer (= 5 MHz)
  - Event-driven control (input-output mode)
  - Waiting rather than sampling (A2A components)

Simulation results

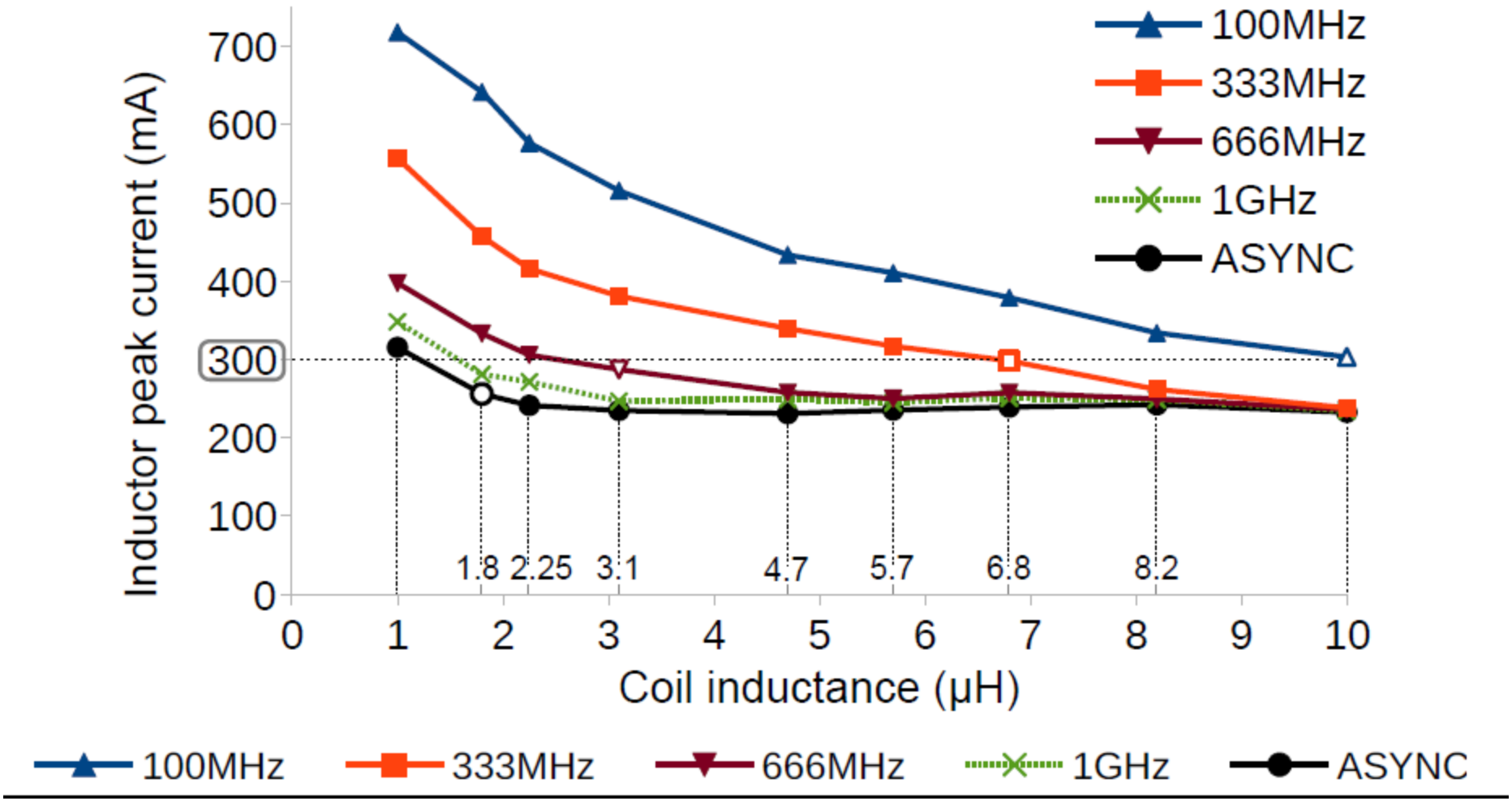


Reaction time

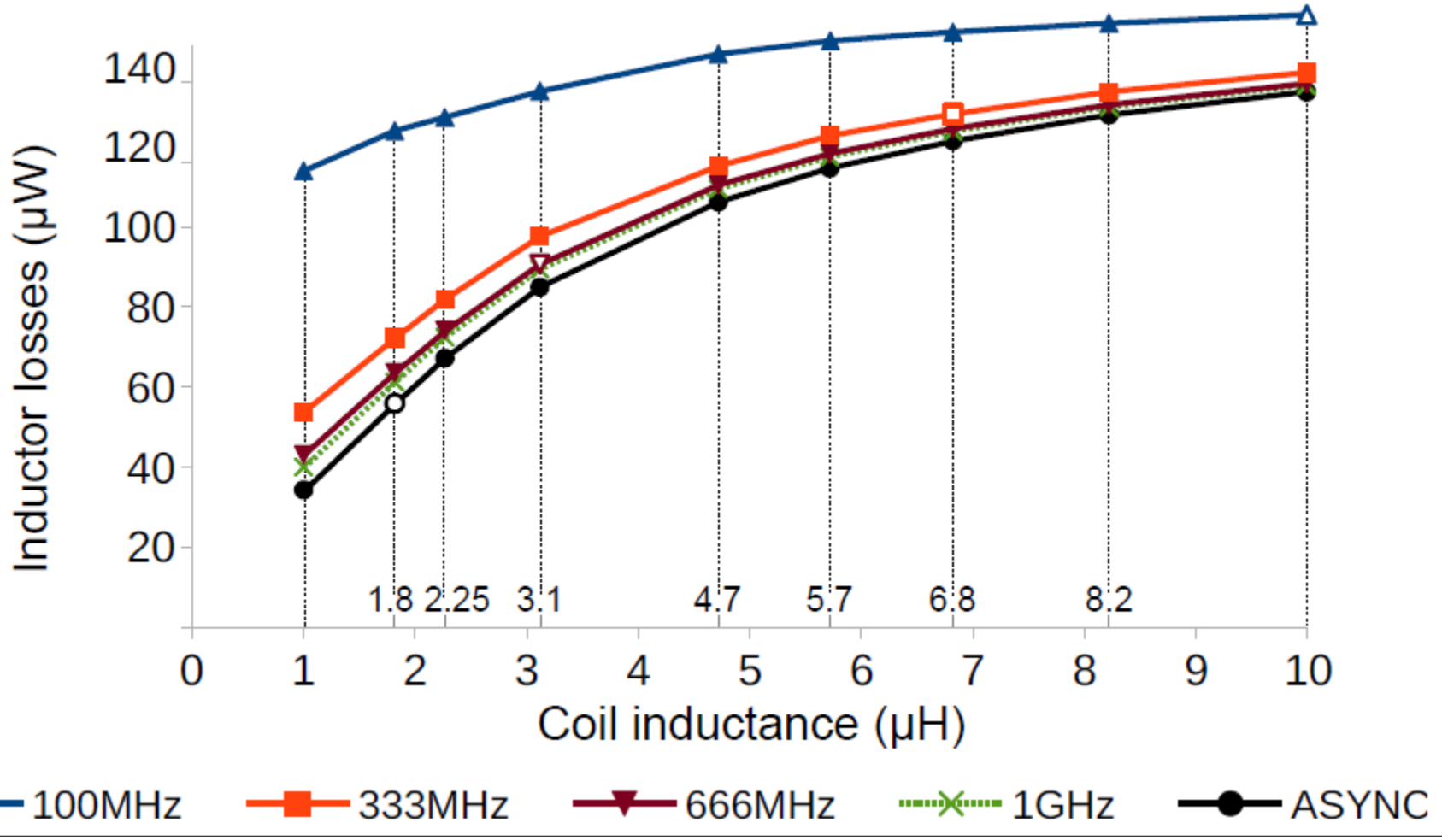
Buck controller	HL (ns)	UV (ns)	OV (ns)	OC (ns)	ZC (ns)
SYNC @ 100MHz	25.00	25.00	25.00	25.00	25.00
SYNC @ 333MHz	7.50	7.50	7.50	7.50	7.50
SYNC @ 666MHz	3.75	3.75	3.75	3.75	3.75
SYNC @ 1GHz	2.50	2.50	2.50	2.50	2.50
ASYNC	1.87	1.02	1.18	0.75	0.31
Improvement over 333MHz	4x	7x	6x	10x	24x

Synchronous buck controllers exhibit latency of 2.5 clock cycles.

Peak current



Inductor losses

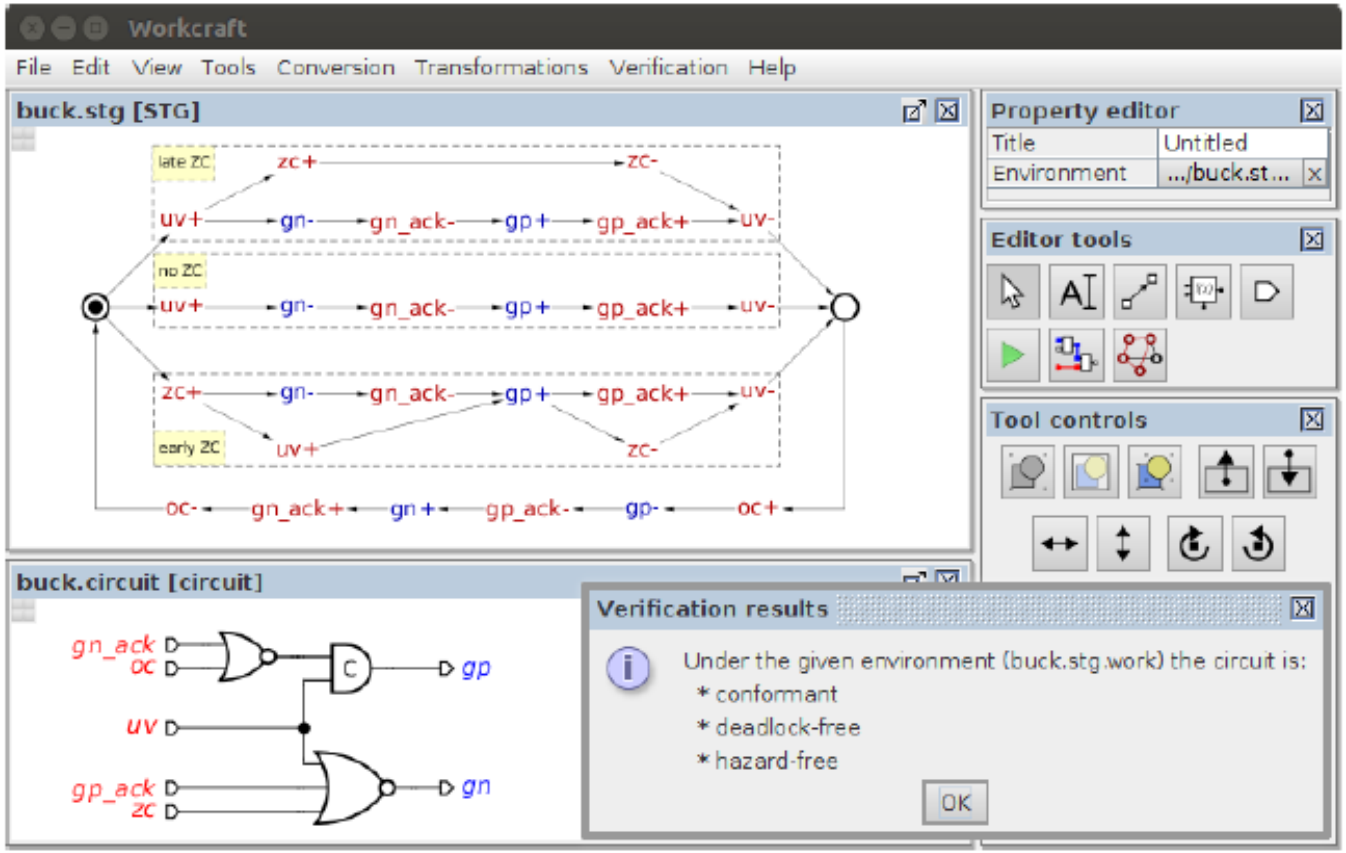


Async Design Tools:

Workcraft.org

Workcraft.org

Logic synthesis and formal verification of asynchronous circuits.



The tool is now used in education, research and industry.

Open source and well supported by tutorials

Messages to take away (for IC design research)

- Asynchronous circuits began their life (in the 50s) for 'little digital' and today is the right time for them
- Analog and mixed-signal is a good application – it combines:
  - Need for low latency and high range of feedback types
  - Non-traditional benefits (inductor size, peak current) can be gained
- Productivity in industry is a good drive – and we have tools accepted by industry
- Interesting research problems are there – tech mapping, holistic analog-mixed signal verification, behavioural mining, dealing with complexity

Messages to take away (for materials and devices researchers)

- Think about power and timing and their relationship
- Thanks to Asynchronous logic and Power-modulated computing we can:
  - Tolerate imperfections of technology (e.g. Variability), so don't push yourself in optimising devices
  - Tolerate environmental variations (e.g. Power doesn't need to be perfectly regulated)
- This is a good way towards building trillions of devices without batteries

THANK YOU!