Avoiding Instabilities in Power Electronic Systems: Toward an On-Chip Implementation

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Abstract

The available controller chips for power electronic systems are used for specific transient and steady-state performances. In such systems, the parameter ranges for stable operation are delimited by slow-timescale as well as fast-timescale instabilities. The usual practice is to design the control loop based on the state-space averaging technique, which cannot predict the fast-timescale instabilities. In this paper the first attempt has been made to propose a new design of the controller chip that can suppress these instabilities, thus extending the stable operating range in the parameter space. For this, we make use of the Filippov method which can effectively predict both types of instabilities. In this approach, the stability of the system is obtained in terms of the state transition matrices across each subsystem and saltation matrices across each switching event. The basic idea is to exercise control over the saltation matrices to increase the stability margin of the periodic orbit. Since in the Filippov approach an increase in the number of switching events in a cycle does not increase the complexity of the analysis, the proposed controller chip will be particularly useful in complex power electronic systems such as interconnected converters, multi-input multi-output converters, resonant converters, micro-grids etc.

Keywords: Stability analysis, Filippov method, saltation matrix, slow-timescale instability, fast-timescale instability, cascaded converter.

1 Introduction

Controllers for power electronic systems have the specific objective of producing switching signals, which is normally done using well-established strategies like voltage mode or current mode control. The output voltage is compared with a reference

voltage to produce the control voltage (in case of voltage mode control) or the current reference for an inner current loop (for current mode control) using a suitable compensator. The values of the storage elements are set using the information of maximum allowable voltage and current ripple, and the parameters of the compensator are decided from the consideration of transient performance using the linearized averaged model of the converter and the standard methods of linear control theory. These strategies are implemented using analog or digital controllers. The desirable steady-state dynamical behavior is where all state variables undergo small periodic oscillations at the clock frequency, and EMI filters are designed for that frequency.

Even though these design procedures are well established and universally followed to design converters and controllers, it has been found that various nonlinear instabilities [1, 2, 3] may set in at different parameter ranges producing undesirable dynamical behaviors with high current and voltage ripples — like subharmonic oscillations at the clock frequency [4, 5] or a slow-timescale oscillation at a much lower frequency [6], or even a chaotic oscillation of the state variables [5]. In digitally controlled converters the discrete sampling and quantization effects can also induce instabilities [7, 8, 9]. The designer therefore sets the “design limits" of the external parameters (like the input voltage and load) based on the values of these parameters where such undesirable behavior sets in. These limits are obtained through averaged the model, circuit simulation of the switched model or experimentally. In complex power electronic systems like cascaded converters, resonant converters, and microgrids, the available parameter ranges for stable operation can be quite small, due to the interaction between the different stages.

However, to allow larger variations of the parameters, there is a necessity to extend these design limits. For some controllers specific strategies have been already developed (e.g., the addition of a compensating ramp to the reference signal in current mode control) to extend these design limits, but these are not general in nature. Therefore, it is necessary to develop methods of avoiding these nonlinear instabilities that can be applied across different systems and controllers. In [10, 11, 12, 13], some preliminary work along this line was reported and was applied to the simple dc-dc converter e.g., buck and boost. The purpose of this paper is to present the approach in a general framework (both theoretically and experimentally) and to provide guidelines for the design of a controller chip that can implement these ideas. Unlike the existing general chips [14, 15] and application specific chips [16, 17], the proposed chip will provide the reliable stable operation for larger parameter ranges by tuning the external resistors proposed controller chip only.

Notable is the fact that the proposed techniques will be effective at steady-state and in no way interfere with targeted transient performance set by suitable compensator. Moreover, the proposed techniques are different from the chaos control methods proposed earlier [17] that aim at locating and stabilizing unstable periodic orbits. Our approach is based on the Filippov method, where the stability of the system is given by the eigenvalues of the monodromy matrix, which is a combination of the state transition matrices and saltation matrices. By suitable manipulation of the individual components of the saltation matrices, stability margin of the system can be extended in practice which in turn increase the useful parameter range. All these methods are validated experimentally in a system of voltage-mode controlled cascaded buck-buck converters.

The rest of the paper is organized as follows. Section 2 presents an overview of stability analysis of periodic orbits using Filippov method. In Section 3 it has been shown that the instabilities can be controlled by three different techniques, each of which exercise control over a specific component of the saltation matrix. In Section 4 an example is considered, the voltage-mode controlled cascaded buck-buck converter, to validate the three specific control methods. The experimental results along with the implementation circuit diagram with different IC chips for different functions are presented in Section 5. In Section 6,

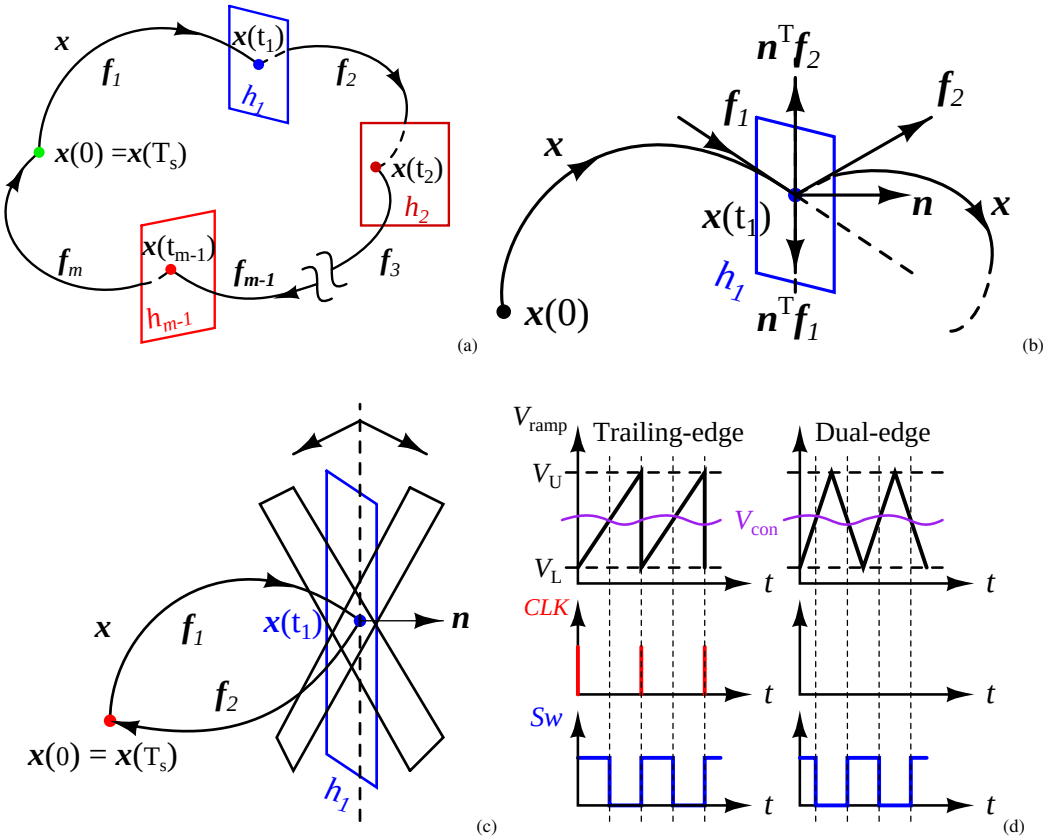

Fig. 1: Schematic diagram of a periodic orbit, switching event and its orientation in a switch-mode converter. (a) Evolution of the state vector $\boldsymbol{x}$ in the state-space, (b) Enlarged view of switching event $h(\boldsymbol{x}, t) = 0$, (c) Orientation of switching surface when $v_{\rm con}$ depends on only one state variable (blue) and more than one state variable (black), (d) Different PWM methods: trailing-edge and dual-edge. (Color online.)

an approach to implement the above ideas in a single controller chip is outlined. Finally in Section 7 the conclusions are listed.

2 Stability analysis of a periodic orbit

As shown in Fig. 1(a), the periodic orbit comprises transitions through a number of subsystems given by different sets of differential equations, and across switching events. For example, in a simple buck or a boost converter the subsystems are the ON and OFF conditions of the switch, and the switchings are the transitions from the OFF state to the ON state and vice versa in continuous conduction mode (CCM). In a more complicated converter like a resonant converter, there may be a large number of subsystems and switching transitions within a cycle. Subharmonic oscillations or slow-timescale oscillations occur when such a periodic orbit loses stability. The information about the stability of a periodic orbit is contained in the state transition matrix computed over a complete cycle. The periodic orbit in continuous time is nothing but the fixed point ($\boldsymbol{x}(0) = \boldsymbol{x}(T_s)$) in the map obtained by sampling the state in synchronism with the clock period T_s. The state transition matrix computed over a complete cycle is nothing but the Jacobian matrix of the map computed at the fixed point. If the magnitude of all the eigenvalues of this matrix are below 1, the periodic orbit is stable.

According to the Filippov approach, the state transition matrix across a full cycle (also called the monodromy matrix) can be calculated as a product of the state transition matrices across each subsystem (denoted as $\boldsymbol{\Phi}_i$, where i identifies the subsystem)

and the state transition matrices across the switching events called saltation matrices (denoted as $\boldsymbol{S}_{i,j}$ for transition from the i^{th} subsystem to the j^{th} subsystem). Thus an orbit that goes through m subsystems, the monodromy matrix can be written as

$$\boldsymbol{\Phi}_{\text{cycle}} = \boldsymbol{\Phi}_m \cdot \boldsymbol{S}_{m-1,m} \cdot \boldsymbol{\Phi}_{m-1} \cdots \boldsymbol{\Phi}_2 \cdot \boldsymbol{S}_{1,2} \cdot \boldsymbol{\Phi}_1 \tag{1}$$

Most power electronic systems are composed of linear subsystems. In that case the state transition matrices across the subsystems are given by exponential matrices

$$\boldsymbol{\Phi}_i = e^{\boldsymbol{A}_i t}$$

where $\boldsymbol{A}_i$ is the state matrix for the i^{th} subsystem.

Now let us consider the state transition matrix across switching events. Suppose there is a switching causing transition from the i^{th} subsystem to the j^{th} subsystem when a condition $h(\boldsymbol{x}, t) = 0$ is satisfied. For example, if the switching occurs when the control voltage equals a ramp waveform voltage, i.e., $v_{\text{con}} - v_{\text{ramp}} = 0$, then the switching function $h(\boldsymbol{x}, t)$ is $v_{\text{con}} - v_{\text{ramp}}$. Suppose that the state equations for the two subsystems are given by

$$\text{Subsystem } i\text{:} \quad \dot{\boldsymbol{x}} = \boldsymbol{f}_i(\boldsymbol{x}, t) = \boldsymbol{A}_i \boldsymbol{x} + \boldsymbol{B}_i \boldsymbol{u} \tag{2}$$

$$\text{Subsystem } j\text{:} \quad \dot{\boldsymbol{x}} = \boldsymbol{f}_j(\boldsymbol{x}, t) = \boldsymbol{A}_j \boldsymbol{x} + \boldsymbol{B}_j \boldsymbol{u} \tag{3}$$

Then the saltation matrix across the switching event is given by [18]

$$\boldsymbol{S}_{i,j} = \boldsymbol{I} + \frac{(\boldsymbol{f}_j - \boldsymbol{f}_i)\boldsymbol{n}^\top}{\boldsymbol{n}^\top \boldsymbol{f}_i + \partial h / \partial t} \tag{4}$$

where $\boldsymbol{I}$ is the identity matrix of the same order as the number of state variables, $h(\boldsymbol{x}, t) = 0$ represents the switching condition which defines a hyper surface in the state-space of the system, $\boldsymbol{n}$ is the vector normal to the switching surface, and $\boldsymbol{n}^\top$ is its transpose. Some of the components of the saltation matrix are shown in Fig. 1(b).

The switching conditions can be of two types:

(a) state-induced switching, where switching occurs when some condition on the state variables is satisfied (for example, the inductor current reaching a reference value), and

(b) time-induced switching, where switching occurs when some condition on *time* is satisfied (e.g., turning the switch on periodically).

The expression (4) gives the state transition matrix for state-induced switching transitions. For time-induced switching the $\boldsymbol{S}_{i,j}$ matrix is unity [10]. The periodic orbit becomes unstable when any of the eigenvalues of the matrix $\boldsymbol{\Phi}_{\text{cycle}}$ goes out of the unit circle. This can happen in three different ways:

- if an eigenvalue becomes equal to -1, a subharmonic oscillation sets in;
- if an eigenvalue becomes equal to $+1$, a saddle-node bifurcation happens; and

- if a pair of complex conjugate eigenvalues has a magnitude of unity, a slow-timescale oscillation sets in.

3 Control of instabilities using saltation matrix

At first, it is to be noted that the matrix $\mathbf{\Phi}_{\rm cycle}$ that ultimately decides the stability of the orbit is composed of two types of component matrices: the state transition matrices $\mathbf{\Phi}_i$ along the subsystems, and $\boldsymbol{S}_{i,j}$ for transitions across subsystems. We now focus on each one, individually.

The current practice of power electronic design is aimed at deciding the parameter values that appear in the state matrices $\boldsymbol{A}_i$. These include the values of the inductances, capacitances, the compensator parameters, etc. We propose to keep these design procedures unaffected, and so do not aim at making any alteration in the state transition matrices $\mathbf{\Phi}_i$. This ensures that the ripple magnitudes and the transient performance—aimed at which the controller was designed—remains unchanged.

Our proposed techniques focus on making small alterations in the matrices $\boldsymbol{S}_{i,j}$ to push the eigenvalues of the monodromy matrix inside the unit circle. Since the state transition matrix across a time-induced switching transition is an identity matrix, it is further narrowed down on the events of state-induced switching.

Upon a closer examination of the expression (4) it has been noticed that it is composed of the following components:

$\boldsymbol{f}_i, \boldsymbol{f}_j$: the RHS of the state equations before and after switching

$\boldsymbol{n}$: the vector normal to the switching surface

$\partial h/\partial t$: the rate at which the switching surface $h(\boldsymbol{x}, t)$ moves with respect to time

Out of these, $\boldsymbol{f}_i$ (or $\boldsymbol{A}_i$ and $\boldsymbol{B}_i$) and $\boldsymbol{f}_j$ (or $\boldsymbol{A}_j$ and $\boldsymbol{B}_j$) contain the design parameters, which were decided to leave unaltered. Therefore, the control of instabilities can be affected by the remaining two components, $\partial h/\partial t$ and $\boldsymbol{n}$. In the following sections we illustrate various ways in which these two can be altered, and in a given situation any of these possibilities can be adopted depending on the preference of the designer.

3.1 Controlling the normal vector $\boldsymbol{n}$

The normal vector depends on the orientation of the switching surface in the state space as illustrated in Fig. 1(c). Consider a voltage mode controlled buck converter with a proportional controller K_p. The control voltage $v_{\rm con} = K_p(V_{\rm ref} - v_o)$ is dependent on the output voltage alone. Therefore, in the capacitor voltage versus inductor current state space, $h(\boldsymbol{x}, t) = v_{\rm con} - v_{\rm ramp}$ will be a straight line parallel to the inductor current axis for an ideal capacitor (ESR=0). The vector $\boldsymbol{n}$ normal to that is parallel to the voltage axis. Due to the time-variation of $v_{\rm ramp}$, the function h sweeps through the state space, and switching occurs when it meets the state-point.

It is clear that, so long as the control voltage is generated through capacitor voltage feedback alone, the orientation of the switching function h will be the same (shown by blue color). If the inductor current i_L is also used to generate the control signal $v_{\rm con}$, the orientation of h will change (shown by black color) and the expression of $v_{\rm con}$ becomes as follows:

$$v_{\rm con} = K_p(V_{\rm ref} - v_o) - K_{i_L} i_L$$

where K_{i_L} is the gain for current feedback. If a proportional-integral (PI) controller is used for the voltage loop together with

current feedback, the expression becomes

$$v_{\rm con} = K_p(V_{\rm ref} - v_o) + K_i \int (V_{\rm ref} - v_o)dt - K_{i_L} i_L$$

where K_i is the integrator gain. The integrator has an associated state variable $\rho = \int (V_{\rm ref} - v_o)dt$. The new switching surface is

$$h(\boldsymbol{x}, t) = v_{\rm con} - v_{\rm ramp} = K_p(V_{\rm ref} - v_o) + K_i\rho - K_{i_L} i_L - v_{\rm ramp}$$

Therefore, the normal vector to the switching surface is given by

$$\boldsymbol{n} = \begin{bmatrix} \partial h/\partial v_o \\ \partial h/\partial i_L \\ \partial h/\partial \rho \end{bmatrix} = \begin{bmatrix} -K_p \\ -K_{i_L} \\ K_i \end{bmatrix}$$

By controlling the ratio of K_p and K_{i_L}, the normal vector can be controlled. This approach is particularly applicable in situations where the current signal is available in the voltage across the capacitor, because of the ESR of the capacitor [19].

3.2 The control of $\partial h/\partial t$

In case of pulse-width modulation techniques, the switching surface sweeps through the state space. For example, in a voltage mode controlled converter, the switching occurs when the control voltage equals the ramp voltage:

$$\begin{aligned} h(\boldsymbol{x}, t) &= v_{\rm con} - v_{\rm ramp} \\ &= v_{\rm con} - \left\{ V_L + (V_U - V_L) \left(\frac{t}{T_s} \bmod 1 \right) \right\} \end{aligned} \tag{5}$$

The expression (5) shows that the time-dependence of h depends on both the control voltage and the ramp voltage. The lower and upper thresholds of the $v_{\rm ramp}$ are denoted by $V_{\rm L}$ and $V_{\rm U}$ respectively and T_s is the clock period.

3.2.1 Slope control of $v_{\rm ramp}$

In a voltage mode controlled converter, the switching surface $h(\boldsymbol{x}, t)$ sweeps through the state space at a speed of

$$\frac{\partial h}{\partial t} = -\frac{V_U - V_L}{T_s}$$

This is nothing but the slope of the ramp waveform. This slope can be altered by making small changes in $(V_U - V_L)$ while keeping the clock period constant, or by varying the clock period T_s while keeping amplitude of the ramp signal constant. The second option may not be desirable because the EMI filters are tuned to the clock frequency.

It is interesting to note that in current mode control, the widely known technique of adding a stabilizing ramp achieves exactly this, as it induces a change in $\partial h/\partial t$. In this paper we are generalizing the idea, to make it applicable to any converter and control strategy.

3.2.2 Addition of external signal with $v_{\rm con}$

Normally the control voltage is generated through a linear compensator using the feedback of the output voltage and eventually the inductor current that needs to be regulated. Therefore $v_{\rm con}$ does not have any explicit dependence on time. But the injection of a time-varying signal can make $v_{\rm con}$ explicitly dependent on time, which can act as a lever in controlling $\partial h/\partial t$.

An interesting possibility is offered by the injection of a sinusoidal signal synchronized with the clock frequency f_s (or at an integer multiple of the clock frequency). It has been shown earlier that this strategy can effectively increase the parameter range for stable operation [12, 10]. Suppose that the injected signal is given by $q(t) = a\sin(\omega_s t + \theta)$ where $\omega_s = 2\pi f_s$. In order to be used as an effective stabilization strategy, the design guideline has to take into account the following considerations. Firstly, this injected signal is not likely to be invasive of the desired steady-state operation and therefore to alter the duty ratio in the steady state. Therefore its value should be zero at the switching instant, i.e.,

$$\sin(\omega_s t + \theta) = 0 \quad \text{at the switching instant}$$

or, $\theta = -2\pi{\times}d$ where d is the duty ratio. The steady state duty ratio can be calculated using the information about the input voltage and the demanded output voltage, which can be used to set the phase of the injected sinusoidal signal. Secondly, a maximum effect on $\partial h/\partial t$ at the switching instant is desired. This is automatically guaranteed if the injected signal is a sinusoid, because the derivative is a cosinusoid, which assumes a maximum value when the signal itself has zero value.

3.2.3 Utilizing the edges of triangular wave

Fig. 1(d) shows two different PWM modulation methods: trailing-edge and dual-edge which can give different stability margins. If a ramp waveform with an instantaneous reset (trailing-edge) is used to generate the PWM, the first switching within a clock cycle is a state-dependent switching and the second one is time dependent. Thus, saltation matrix across the second switching is always an identity matrix. But if the trailing edge of the waveform does not drop instantaneously and goes through a steady decline with a definite slope (dual-edge), one can have state-dependent switching there also. Thus there would be a non-identity state transition matrix at the second switching event within a clock cycle, and that would have an effect on $\mathbf{\Phi}_{\rm cycle}$, which can be used to push the eigenvalues into the unit circle. Note here that the number of subsystems within a switching cycle increases and the dynamics of the overall system will change. This fact has to be taken into account when designing the controller.

In all practical analog implementations, the trailing edge of the PWM waveform is generated by discharging a capacitor—which cannot happen instantaneously. Therefore, to implement the proposed strategy, all that one has to do is to enforce a state-dependent switching. In digital implementations, the sampling must be done when there is no ringing noise and the easiest way to implement this is by changing the ramp waveform to a triangular wave (dual-edge).

4 Example: Cascaded Buck-Buck Converter

Cascaded converters are used in many applications such as telecommunication systems, computers, and military applications (space stations, aircraft, ships) [20]. It has flexible configuration, high efficiency, and reduced weight and size. Many criteria have been proposed [21] to analyze the stability of such systems, e.g., impedance criterion, phase margin and gain margin criterion,

the opposing argument criterion, the energy source analysis, the maximum peak criterion. [22, 23] have shown, with counter-examples and case studies, that these methods are not applicable to all power electronic systems in general. Some alternate stability assessment methods are also available [24, 25, 26]. However, in these methods the switching dynamics implicitly appear in the expressions, and so these are difficult to apply in complex systems with a large number of switching in a cycle.

The proposed techniques in this paper have been illustrated with a cascade connection of two buck converters which is used in applications that require a low output voltage. More specifically there is a standard voltage mode controlled buck converter with PI compensator followed by another one as shown in Fig. 2(a). Unlike the approximate linearized state-space averaged model which neglects the switching dynamics, we have used an exact model of the overall switched nonlinear system considering the interaction between two stages.

So far most of the research on cascaded converters has been done for the converters operating in continuous conduction mode (CCM), feeding constant power loads (CPLs). In this paper, a system is considered in which the first converter operates in discontinuous conduction mode (DCM) and the second in CCM—a configuration on which very few reports are available [27, 28]. In this system there are 8 subsystems, and there can be many switching events within a clock cycle. Such a system is very difficult to analyze using the methods mentioned earlier. But in our approach, the complexity of the system does not increase the complexity of the model.

4.1 System Description

As shown in Fig. 2(a), both the switches S_1 and S_2 are driven by pulse-width modulated (PWM) switch signals u_1 and u_2. These signals are generated by comparing the control voltage $v_{\rm con}$ with a ramp signal $v_{\rm ramp}$. When $v_{\rm con}$ is greater than $v_{\rm ramp}$, the switch signal u is "HIGH" and is "LOW" otherwise. The PI compensators are used to get zero steady-state error for both the output voltages. To prevent multiple switching within a clock cycle S-R flip-flops (FF_1 and FF_2) have been introduced.

For the first converter, the control voltage and the ramp voltage are given by

$$v_{\rm con1} = K_{\rm p1}(V_{\rm ref1} - v_{\rm o1}) + K_{\rm i1}\int (V_{\rm ref1} - v_{\rm o1})dt$$
$$v_{\rm ramp1} = V_{\rm L1} + (V_{\rm U1} - V_{\rm L1})\left(\frac{t}{T_s} \mod 1\right)$$

where, $K_{\rm p1}$ and $K_{\rm i1}$ denote the proportional and integral gains respectively, $v_{\rm o1}$ is the output voltage, $V_{\rm L1}$ and $V_{\rm U1}$ are the threshold voltages of the ramp, and T_s is the switching period.

4.2 Mathematical Modeling

The power stage of the system (Fig. 2(a)) is described by the following set of differential equations

$$\frac{di_{L_1}}{dt} = \frac{1}{L_1}\left[-v_{\rm o1} + u_1 V_{\rm in}\right], \qquad \frac{dv_{\rm o1}}{dt} = \frac{1}{C_1}\left[i_{L_1} - u_2 i_{L_2}\right], \tag{6}$$
$$\frac{di_{L_2}}{dt} = \frac{1}{L_2}\left[u_2 v_{\rm o1} - v_{\rm o2}\right], \qquad \frac{dv_{\rm o2}}{dt} = \frac{1}{C_2}\left[i_{L_2} - \frac{v_{\rm o2}}{R_L}\right] \tag{7}$$

where $u_1 = 1$ and $u_2 = 1$ if both the switches S_1 and S_2 are ON ($u_1 = 0$ and $u_2 = 0$ if S_1 and S_2 are OFF).

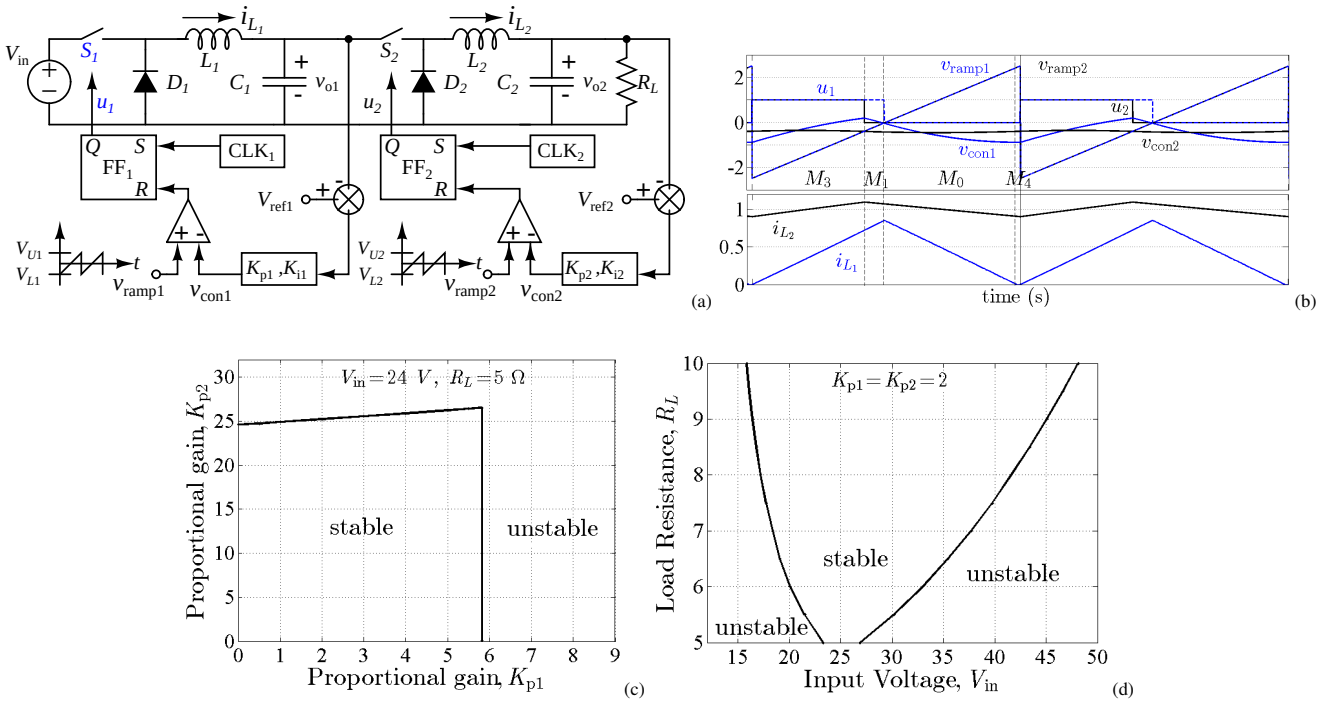

Fig. 2: Cascaded buck-buck converters with voltage mode control (a) Closed-loop circuit diagram, (b) Nominal period-1 waveforms of the control voltages, ramps, and currents when the first converter is in DCM and the second converter is in CCM, (c) Stable region in the $K_{p1}-K_{p2}$ parameter space with $V_{in}=24$ V, $R_L=5\ \Omega$, (d) Stable region in the $V_{in}-R_L$ parameter space with $K_{p1}=K_{p2}=2$. Other parameters are given in Table 2(b).

The two integrators of the PI compensatots are given by the following state equations

$$\frac{d\rho_1}{dt}=K_{i1}[V_{ref1}-v_{o1}],\quad \frac{d\rho_2}{dt}=K_{i2}[V_{ref2}-v_{o2}]. \tag{8}$$

For different operating conditions there are different switch signals u (subsystems M_k) as given in (Table 1). For two switches (S_1 and S_2), 2^2 different set of linear differential equations are possible in continuous conduction mode (CCM). In discontinuous conduction mode (DCM) of the first stage ($i_{L_1}=0$, both S_1 and D_1 are OFF), the number of subsystem increases by four (Table 1).

Table 1: Status of switch signals and different subsystems in CCM and in DCM of the first stage

u_2	u_1	i_{L_1}	M_k	u_2	u_1	i_{L_1}	M_k
0	0	>0	M_0	0	0	0	M_4
0	1	>0	M_1	0	1	0	M_5
1	0	>0	M_2	1	0	0	M_6
1	1	>0	M_3	1	1	0	M_7

As shown in Fig. 2(b), when the first stage is in DCM there are four subsystems ($M_3-M_1-M_0-M_4$) within a switching cycle (or clock period) for a typical steady-state operation.

Each subsystem is represented using state-space model as

$$M_k : \dot{\boldsymbol{x}} = \boldsymbol{A}_k \boldsymbol{x} + \boldsymbol{B}_k \boldsymbol{u}$$

where, $\boldsymbol{x} = \begin{bmatrix} i_{L_1} & v_{\rm o1} & \rho_1 & i_{L_2} & v_{\rm o2} & \rho_2 \end{bmatrix}^\top$, $\boldsymbol{u} = \begin{bmatrix} V_{\rm in} & V_{\rm ref1} & V_{\rm ref2} \end{bmatrix}^\top$. The subsystems M_k are defined in Table 1 and some of them are appearing in a typical steady-state are shown in Fig. 2(b).

The transitions between subsystems occur after satisfying switching conditions which change the status of the switch signals. Therefore, the switching instants can be determined from the following switching conditions:

$$h_1 : \ v_{\rm con1} - v_{\rm ramp1} = 0, \quad h_2 : \ v_{\rm con2} - v_{\rm ramp2} = 0, \quad h_3 : \ i_{L_1} = 0.$$

Table 2: System design: (a) Specifications, and (b) Parameter values for power-stage and controllers.

Specifications	Values
Input voltage	$V_{\rm in} = 24$ V
Output voltage (1^{st} stage)	$v_{\rm o1} = 12$ V$\pm 5\%$
Output voltage (2^{nd} stage)	$v_{\rm o2} = 5$ V$\pm 1\%$
Output Power	$P_{\rm o2} = 5$ W
Switching frequency	$f_s = 10$ kHz

(a)

Parameters	Values
Inductors	$L_1 = 0.70$ mH, $L_2 = 1.5$ mH
Capacitors	$C_1 = 50$ μF, $C_2 = 50$ μF
Output Resistor	$R_L = 5$ Ω
Voltage References	$V_{\rm ref1} = 12$ V, $V_{\rm ref2} = 5$ V
Threshold of the ramps	$V_{\rm U1} = V_{\rm U2} = 2.5$ V, $V_{\rm L1} = V_{\rm L2} = -2.5$ V
Proportional gains	$K_{\rm p1} = K_{\rm p2} = 2$
Integral gains	$K_{\rm i1} = K_{\rm i2} = 1000\ s^{-1}$

(b)

4.3 Design of the Overall System

Based on the specifications (Table-2(a)), the design values of the power-stage and controllers are given in Table-2(b). The current ripple in the second stage is kept within $\pm 20\%$ of the output current.

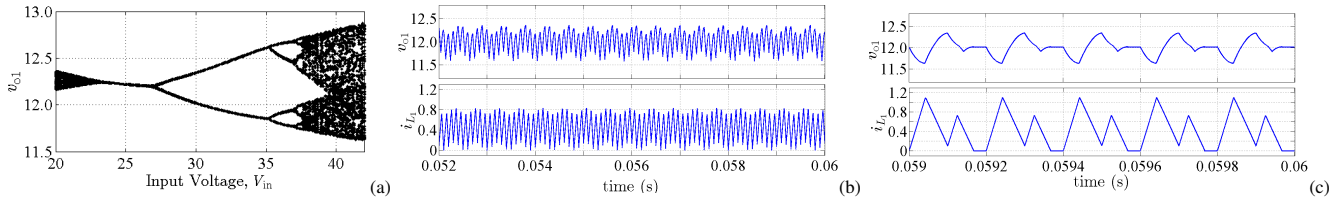

Fig. 3: Bifurcation diagram and waveforms. (a) Bifurcation diagram with $V_{\rm in}$ as varying parameter, (b) waveforms at $V_{\rm in} = 20$ V, slow-time-scale or quasi-periodic oscillations, (c) waveforms at $V_{\rm in} = 30$ V, subharmonic oscillation. Other parameters are given in Table 2(b).

Table 3: Eigenvalues for different values of $V_{\rm in}$ corresponding to Fig. 3(a).

$V_{\rm in}$(V)	Orbit	Subsystem Sequence	Eigenvalues
20.00	Unstable Period-1	$M_3-M_1-M_0$	0.1860 $\pm$ 0.9879j (≈ 1.0053), 0.5590 $\pm$ 0.6395j, 0.9561, 0.9617
23.32	Unstable Period-1	$M_3-M_1-M_0$	0.1012 $\pm$ 1.0028j (≈ 1.0078), 0.5566 $\pm$ 0.6391j, 0.9553, 0.9618
23.33	Stable Period-1	$M_3-M_1-M_0-M_4$	0.9572 $\pm$ 0.0048j (≈ 0.9572), 0.5553 $\pm$ 0.6119j, 0.1407, 0
24.00	Stable Period-1	$M_3-M_1-M_0-M_4$	0.9571 $\pm$ 0.0045j (≈ 0.9571), 0.5556 $\pm$ 0.6127j, 0.1121, 0
26.90	Stable Period-1	$M_3-M_2-M_0-M_4$	$-$0.9995, 0.5709 $\pm$ 0.6074j (≈ 0.8336), 0.9555, 0.9541, 0
26.91	Unstable Period-1	$M_3-M_2-M_0-M_4$	$-$1.0002, 0.5708 $\pm$ 0.6074j (≈ 0.8335), 0.9555, 0.9541, 0
26.91	Stable Period-2	$M_3-M_2-M_0-M_4$– $M_3-M_1-M_0-M_4$	$-$0.0430 $\pm$ 0.6801j (≈ 0.6815), 0.9133, 0.9096, 0.0159, 0
30.00	Stable Period-2	$M_3-M_2-M_0-M_4-M_3-M_1-M_0$	$-$0.2451, $-$0.0643 $\pm$ 0.7075j (≈ 0.7104), 0.9161, 0.9106, 0
35.00	Stable Period-2	$M_3-M_2-M_7-M_4-M_3-M_2-M_0$	$-$0.2705, $-$0.0614 $\pm$ 0.6967j (≈ 0.6994), 0.9111, 0.9128, 0

With a set of parameters given in Table 2(b), the first stage is in DCM and the second stage is in CCM. The stable region has been shown in the parameter space of proportional controller gains (Fig. 2(c)). If $K_{\rm p1}$ is increased beyond 5.82, a border collision bifurcation occurs resulting in chaotic oscillations. The stable region in the $V_{\rm in}-R_L$ parameter space is shown in Fig. 2(d). If R_L is held at 5 Ω the system is stable over a small range of input voltage [23.33, 26.90] V. As $V_{\rm in}$ goes below 23.33 V, a slow-timescale instability sets in through a Neimark-Sacker bifurcation, and as $V_{\rm in}$ goes above 26.90 V, a period doubling bifurcation occurs resulting in subharmonic oscillations. The calculated eigenvalues of the monodromy matrix for different input voltages are given in Table 3.

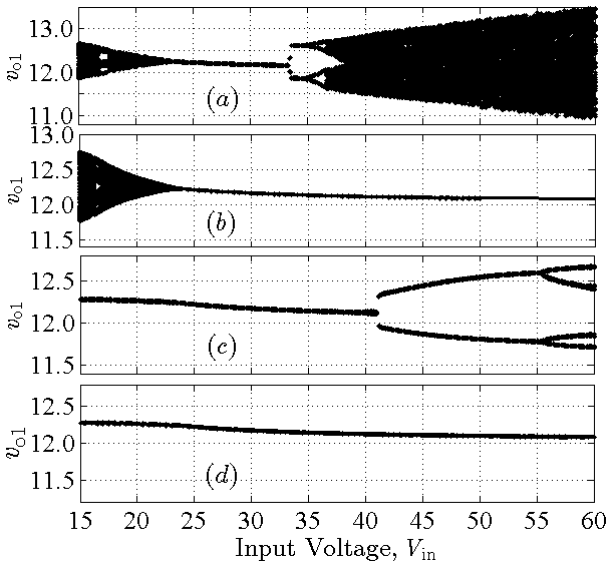

Fig. 4: Bifurcation diagrams with $V_{\rm in}$ as varying parameter (a) with sinusoidal injection ($a=0.2$, $\theta=0$), (b) with ramp thresholds $V_{\rm U1}=V_{\rm U2}=5$ V and $V_{\rm L1}=V_{\rm L2}=-5$ V, (c) with current feedback $K_{i_{L_1}}=K_{i_{L_1}}=0.5$, (d) applying all the methods together.

4.4 Avoiding Instabilities

Fig. 4 shows the increase of stability limits using three different techniques: with an injected sinusoidal signal (Fig. 4(a)), by changing the ramp threshold voltages (Fig. 4(b)), and by current feedback (Fig. 4(c)). It is clear that the stable range of the input voltage has increased in all the cases. It can be noted that the phase of the injected sinusoidal signal is zero. This value was used

Table 4: Eigenvalues with variation of V_{in} corresponding to Fig. 4(d).

V_{in} (V)	Orbit	Subsystem Sequence	Eigenvalues
15	Stable Period-1	$M_3-M_1-M_0$	0.9654 ± 0.0007j (≈ 0.9654), 0.4847 ± 0.8305j, 0.6772 ± 0.4768j
24	Stable Period-1	$M_3-M_1-M_0-M_4$	0.9630 ± 0.0076j (≈ 0.9630), 0.6538 ± 0.4614j, 0.5033, 0
40	Stable Period-1	$M_3-M_1-M_0-M_4$	-0.1766, 0.6802 ± 0.4612j (≈ 0.8218), 0.9604, 0.9575, 0
50	Stable Period-1	$M_3-M_2-M_0-M_4$	-0.4521, 0.6809 ± 0.4652j (≈ 0.8246), 0.9623, 0.9553, 0
60	Stable Period-1	$M_3-M_2-M_0-M_4$	-0.6907, 0.6810 ± 0.4676j (≈ 0.8261), 0.9629, 0.9545, 0
75	Stable Period-1	$M_3-M_2-M_0-M_4$	-0.9968, 0.6809 ± 0.4699j (≈ 0.8273), 0.9634, 0.9539, 0

because it is easy to implement, though, as we have seen earlier in Section 3.2.2, this method has maximum effect if $\theta = 2\pi \times d$ where d is the duty ratio of the converter.

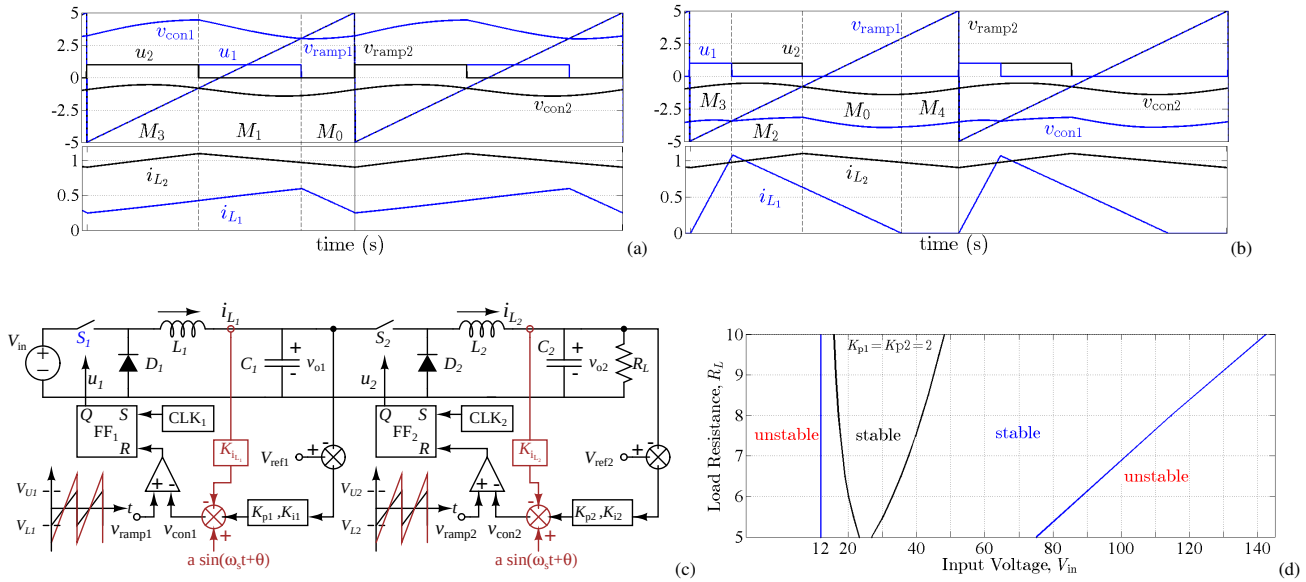

Fig. 5: Waveforms of the modified circuit and its stability: (a) Waveforms at $V_{\text{in}} = 15$ V, period-1 (b) Waveforms at $V_{\text{in}} = 60$ V, period-1, corresponding to Fig. 4(d). Other parameters are given in Table 2(b), (c) Closed-loop circuit of voltage mode controlled cascaded buck-buck converters with sinusoidal injection, current feedback and increment of ramp amplitude (brown color), (d) Stable regions in the parameter space $V_{\text{in}} - R_L$.

Fig. 4(d) shows that, when all the proposed techniques are applied simultaneously, an even higher range of input voltage for stable operation can be obtained. The waveforms for the steady-state period-1 operation at $V_{\text{in}} = 15$ V and $V_{\text{in}} = 60$ V are given in Fig. 5(a) and (b) respectively. After applying sinusoidal injection and current feedback mechanisms the control voltage is modified as $v_{\text{con1}} = K_{\text{p1}}(V_{\text{ref1}} - v_{\text{o1}}) + \rho_1 + a\sin(2\pi f_s t) + K_{i_{L_1}} i_{L_1}$, where integral state $\rho_1 = K_{\text{i1}} \int (V_{\text{ref1}} - v_{\text{o1}})dt$. The amplitude of the ramp voltage v_{ramp1} is increased by changing the difference of the thresholds $(V_{\text{U1}} - V_{\text{L1}})$. The calculated eigenvalues of the monodromy matrix for different input voltages are given in Table 4. This shows that one chip with all these facilities (Fig. 5(c)) can be very useful in control-oriented design of the converters that can operate stably over very large parameter ranges as given in Fig. 5(d). Note that the region delimited by black lines increases to that delimited by blue lines as a result of the proposed control.

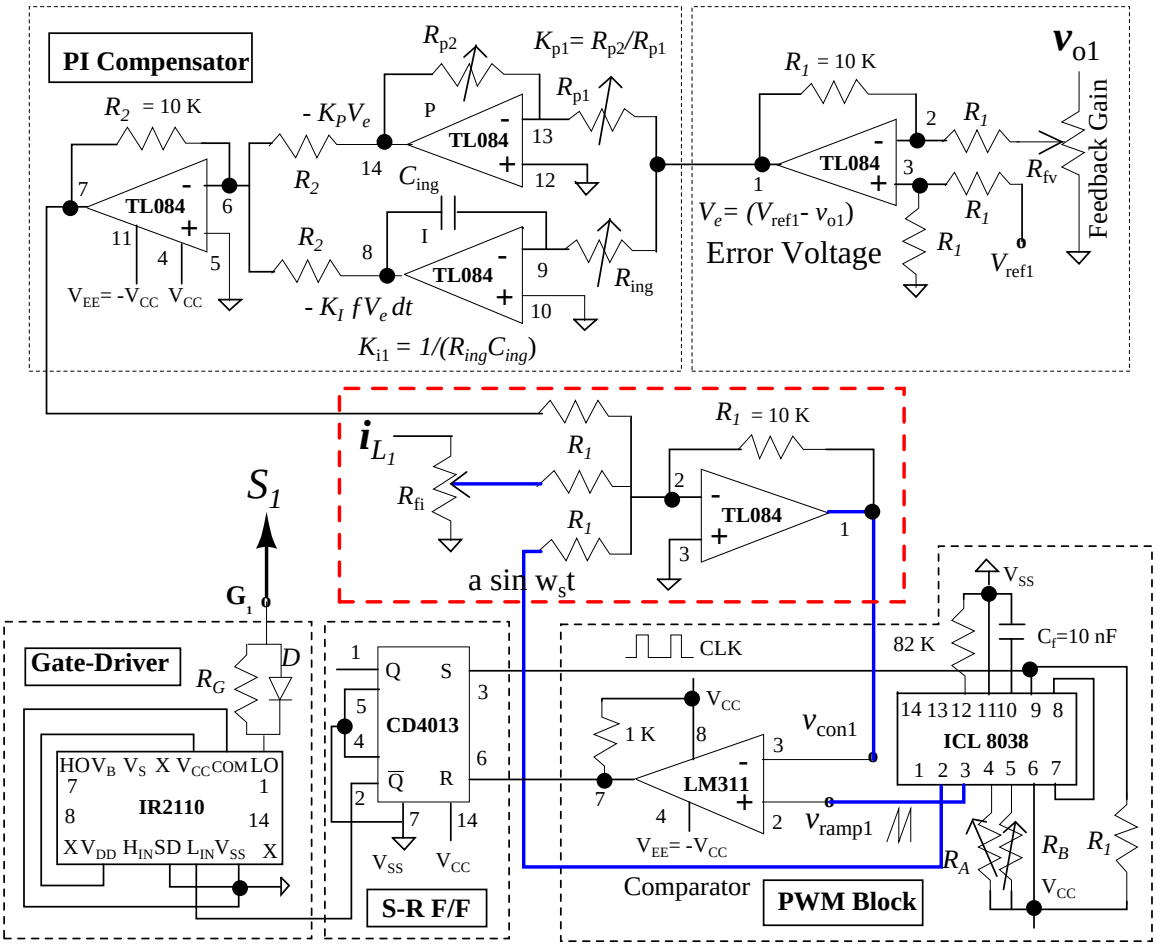

Fig. 6: Implementation of the proposed control mechanisms for the first stage of the voltage mode controlled cascaded buck converter using different IC chips for different functions.

5 Experimental Validation Using Discrete Components

In this section, theoretical results corresponding to the cascaded buck converter has been validated using an experimental prototype. The parameter values for the power stage and controller stage given in Table 2(b). The schematic diagram of the system with the conventional voltage mode controller with PI compensator is presented in Fig. 2(a) and that incorporating the proposed control methods is given in Fig. 5(c). The circuit implementation with discrete components for the controller of the first stage is shown in Fig. 6. Relatively higher values of the output capacitors ($C_1 = 100$ μF, $C_2 = 80$ μF,) were chosen to keep the voltage ripples ($\pm$ 0.1 V) within limit in presence of ESR ($r_{C_1} = 0.2$ Ω, $r_{C_2} = 0.15$ Ω). The MOSFET switches S_1 and S_2 are realized using IRF640 ($R_{\mathrm{DS(ON)}} = 0.15$ Ω) which are driven by driver IC IR2110. Two E-type Ferrite core inductors with values 0.7 mH ($r_{L_1} = 0.12$ Ω) and 1.5 μH ($r_{L_2} = 0.22$ Ω) were fabricated with maximum current rating of 3 A. The diodes D_1 and D_2 are realized by Schottky diode SR240 with forward voltage drop of 0.5 V. In the controller stage, IC ICL8038 is used to get synchronized clock, ramp and sinusoidal signals. The rising slope, falling slope, and frequency of the ramp are controlled by R_A, R_B, and C_f respectively. For the realization of the error amplifier, the compensators, addition, subtraction etc., the operational amplifier TL084 is used. The gains of the PI compensators are obtained from the values of capacitors and variable resistors around the op-amps. The current through inductors are measured using LEM HY 5-P (bandwidth 50 kHz). The comparator IC

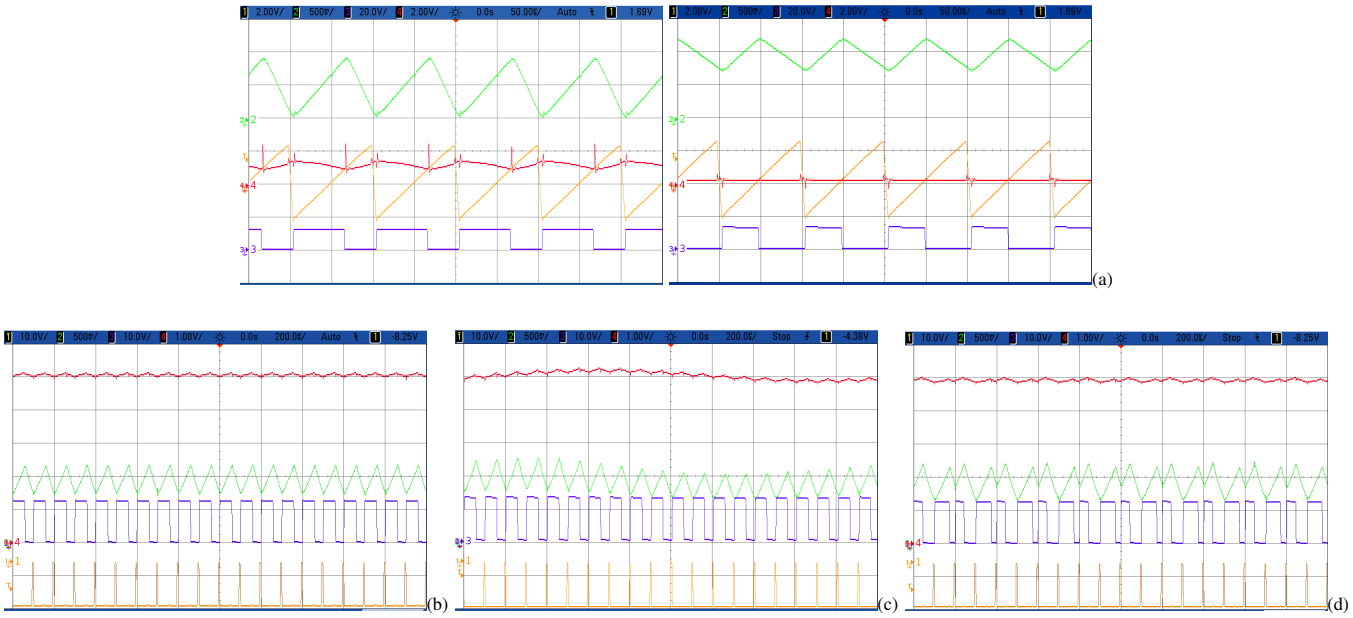

Fig. 7: Experimental waveforms with conventional PI compensator for (a) both the stages when the first converter is in DCM and the second converter is in CCM. The control voltages (magenta), ramps (yellow), gate signal to the MOSFETs (violet) and currents (green). The second stage buck converter at (b) $V_{\text{in}} = 24$ V, period-1, (c) $V_{\text{in}} = 16$ V, slow-timescale (quasi-periodic) oscillation, (d) $V_{\text{in}} = 32$ V, period-2. Clock signal (yellow), gate signal of the MOSFET (violet), inductor current (green), output voltage (magenta). (Color online.)

LM311 compares the control voltage with the ramp voltage. For realization of S-R flip-flop, IC CD4013 is used. At the start of the clock period, the output (pin 2) is set HIGH with the rising transition of the clock (CLK) when data input (pin 5) is grounded. Resetting of the output (pin 2) is accomplished by the high level of the comparator to the pin 6.

By setting $K_p = 4$, and $K_i = 1000$ s^{-1}, the waveforms of the system show period-1 behavior for both the stages at $V_{\text{in}} = 24$ V as shown in Fig. 7(a). Now starting with this nominal voltage $V_{\text{in}} = 24$ V, the second stage buck converter has output ripple voltage within 0.1 V (Fig. 7(b)). With the decrease of the input voltage, at $V_{\text{in}} = 16$ V a slow-scale oscillation is introduced in the output voltage (Fig. 7(c)). The output voltage ripple now increases to 0.36 V. On the other hand if the input voltage increases, a fast-timescale subharmonic oscillation sets in (current waveform in Fig. 7(d)) at $V_{\text{in}} = 32$ V.

After applying three control mechanisms: current feedback, sinusoidal injection and increasing the ramp amplitude, the system is stable for the large input voltage range as shown in Fig. 8(a) and (b). Qualitatively, the simulation and experimental results without the proposed control mechanisms and with control mechanisms are in good agreement.

6 Design of a single controller chip

We propose to implement all the above ideas in a single voltage mode controller chip (Fig. 8(c)) with which converters of very large operating ranges can be designed. A controller chip for current mode control can be produced in a similar manner.

Design guidelines for the controller chip are as follows:

- In the available chips[14, 15], the frequency can be set using the external resistor and capacitor. There is no facility of controlling the amplitude of the ramp signal.

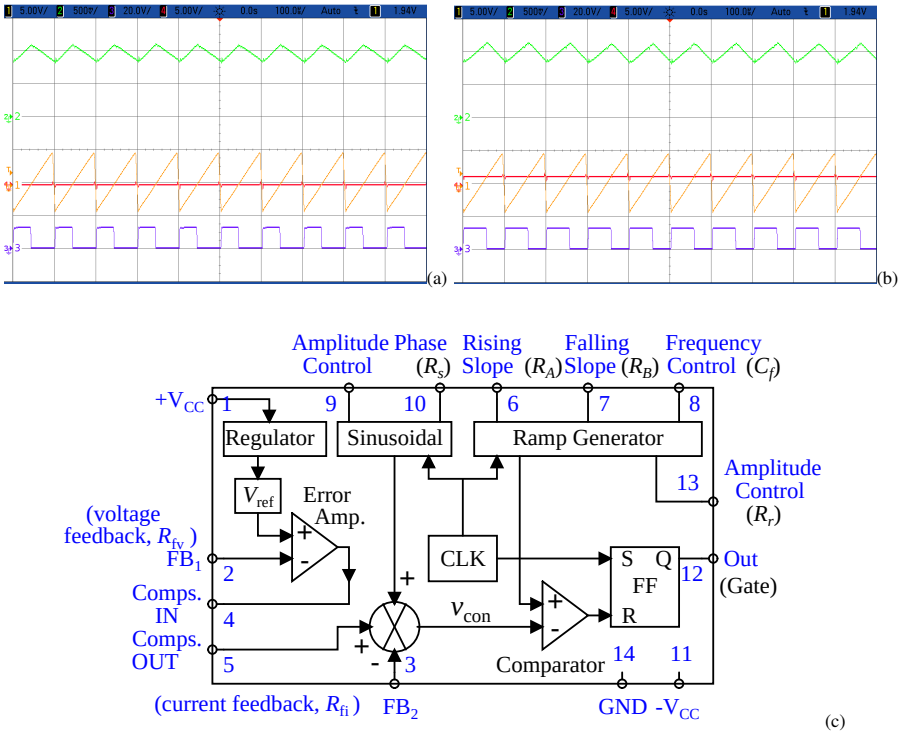

Fig. 8: Experimental waveforms for the second stage buck converter with three control mechanisms: current feedback, sinusoidal injection and increasing the ramp amplitude at (a) $V_{\text{in}} = 16$ V, period-1, (b) $V_{\text{in}} = 60$ V, period-1. The control voltages (magenta), ramps (yellow), gate signal to the MOSFETs (violet) and currents (green), (c) The functional block diagram of the proposed 14 pin voltage mode controller chip showing connections to typical external components.(Color online.)

In the proposed chip, as shown in Fig. 8(c), the generation of a ramp with amplitude control facility (pin 13) is needed using a resistor R_r in addition to the control of the frequency. Suitable components resistors (R_A, R_B) and capacitor (C_f) are connected externally to determine the frequency of the ramp. To set the value of the frequency, capacitor C_f is connected to pin 8 and to control the slope of rising edge (pin 6), falling edge (pin 7) of the ramp independently, tuning of variable resistors R_A and R_B is needed.

- Generation of a sinusoidal voltage (pin 9) at the same frequency of the ramp. To control the phase (pin 10) of the sinusoid, one can use the traditional constant-amplitude phase shifter in which the phase shift is changed manually by tuning a variable resistor (R_s) [29].

- To prevent multiple switchings an S-R flip-flop along with the clock is needed. In between pin 4 and 5 different compensators such as Type II, Type III can be added externally using op-amps, resistors and capacitors. In this paper we use PI compensator as shown in Fig. 6.

- To generate a fixed and stable reference voltage (V_{ref}) inside the chip, a regulator is used which uses supply voltage at pin 1. At pin 2 (FB_1), output voltage (v_o) is fed through a voltage divider i.e., a tunable resistor (R_{fv}) to compare with the reference voltage. The maximum gain of the feedback gain-setting circuit is 1. The designer can choose reference voltage from wide range of values by selecting minimum gain within practical limits. Similarly, the current is fed back at pin 3 (FB_2) through a tunable resistor R_{fi}.

- The output signal of the compensator, current feedback signal, and sinusoidal signal are added to generate control signal which is compared with the ramp. The output of the S-R flip-flop is available at pin 12 which drives the gate of the MOSFET. The GND and negative supply $-V_{CC}$ of the chip are available at pin 14 and pin 11 respectively.

7 Conclusion

In this paper we have proposed the design guidelines of a controller chip that can drastically increase the operational parameter ranges of power electronic systems, especially the complex converters like cascaded converters, resonant converters, and micro-grids. The three techniques by which one can manipulate the terms that appear in the saltation matrices, can be integrated in a single chip. These have been done in such a way that specific implementations will only need one to choose the external resistances appropriately. This approach can control both fast-scale as well as slow-scale instabilities, without changing the intended transient and steady-state performances. The idea has been experimentally validated using a system of cascaded buck converters, by implementing the controller with discrete components. The basic purpose of this paper was to present a proof-of-concept on the basis of which a chip development effort could be undertaken. The function of the proposed controller chip is the cumulative effect of the functions of all the discrete components. The experimental results using discrete components show that the idea is feasible. The fabrication and testing of such a chip are left for future work.

8 Acknowledgments

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