Adaptive PD+I Control of a Switch-Mode DC–DC Power Converter Using a Recursive FIR Predictor

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***Abstract*—This paper presents an alternative technique for the adaptive control of power electronic converter circuits. Specific attention is given to the adaptive control of a dc–dc converter. The proposed technique is based on a simple adaptive filter method and uses a one-tap finite impulse response (FIR) prediction error filter (PEF). The method is computationally efficient and based around a dichotomous coordinate descent (DCD) algorithm. The DCD-recursive least squares (RLS) algorithm has been employed as the adaptive PEF to reduce the computational complexity of existing RLS algorithms for efficient hardware implementation. Results show that the DCD-RLS is able to improve the dynamic performance and convergence rate of the adaptive gains (filter taps) within the controller. In turn, this yields a significant improvement in the overall dynamic performance of the closed-loop control system, particularly in the event of abrupt parameter changes. The proposed controller uses an adaptive proportional–derivative+integral (PD+I) structure which, alongside the DCD algorithm, offers an effective substitute to a conventional proportional–integral–derivative (PID) controller. The nonadaptive integral controller (+I), introduced in the feedback loop, increases the excitation of the filter tap weight and ensures good regulation. The approach results in a fast adaptive controller with self-loop compensation. This is required to minimize the prediction error signal and, in turn, minimize the voltage error signal in the loop by automatically calculating the optimal pole locations. The prediction error signal is further minimized through a second-stage FIR filter (adaptation gain stage). This ensures that the adaptive gains converge to their optimal value. This paper presents detailed simulation analysis and experimental validation on a prototype synchronous dc–dc buck converter. The experimental results clearly demonstrate the superior dynamic performance and voltage regulation compared to conventional PID and adaptive LMS control schemes, with only a modest increase in the computational burden to the microprocessor.**

***Index Terms*—Adaptive controller, adaptive filter, dichotomous coordinate descent (DCD), finite impulse response (FIR) linear predictor, proportional–integral–derivative (PID) controller, recursive least square (RLS), switch-mode dc–dc power converter (SMPC), system identification.**

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I. INTRODUCTION

MANY CLASSICAL digital control systems for switch-mode power converters (SMPCs) suffer from inaccuracies in the design of the controller. This may be due to poor knowledge of the load characteristics or unexpected external disturbances in the system [1], [2]. In addition, SMPC uncertainties, such as component tolerances, unpredictable load changes, changes in ambient conditions, and aging effects, all affect the performance of the controller [1]–[3]. For these reasons, autotuning and adaptive digital controllers are playing an increasingly important role in SMPC systems. Adaptive digital controllers offer a robust control solution and can rapidly adjust to system parameter variations. However, often, these controllers are not fully exploited in low-cost low-power SMPCs due to the computational complexity of the autotuning algorithm, which may require a high-specification microprocessor to successfully implement [4]. Therefore, there is a requirement to further research and develop cost-effective computationally light autotuning methods which continue to offer robust control performance.

Recent research demonstrates several productive self-tuning and adaptive control techniques for power electronic converter applications. However, these solutions are not always aimed toward low-complexity systems. Often, the algorithms require advanced digital signal processing resources which introduce cost penalties to the target application. Straightforward relay-feedback-based methods have successfully been used in the parameter identification and autotuning of dc–dc converters [5], [6]. However, during the parameter tuning of the PID controller, these methods typically introduce undesirable oscillations into the regulated output for short periods of time [7]. Also, this type of approach requires relatively complex algorithmic steps to tune the controller parameters. Other techniques have been proposed, such as inserting limit cycle oscillations (LCOs) into the duty cycle signal of the power converter [8]–[10]. The compensator is then retuned using pole-zero PID cancellation. This technique is highly efficient in terms of hardware; however, it results in lower system identification accuracy [11]. Alternative methods consider perturbing the duty cycle with a frequency-rich input signal [1], [12], [13]. Typically, Fourier transform methods are applied to find the frequency response of the system. The PID controller parameters are then tuned online using discrete-time dynamic measurements of the system. Unfortunately, the identification process can take significant amount of time to complete and may need to process long data sequences. In addition, during the identification process, the system operates in open loop without regulation [8]. These

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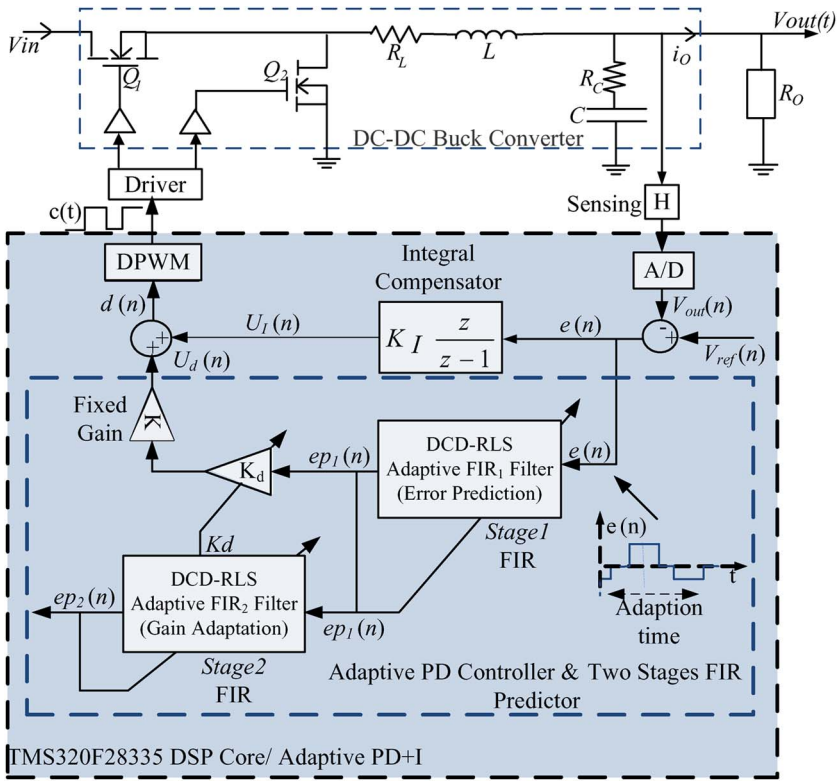

Fig. 1. Adaptive PD+I controller using DCD-RLS algorithm.

self-tuning and adaptive control techniques are most effective during the steady state where the parameters are tuned using predetermined rules, such as phase margin and gain margin requirements. For this reason, these categories of controller are generally unsuitable for time-varying systems where online compensation is desirable.

Kelly and Rinne [14] proposed an adaptive self-learning digital regulator, based on a one-tap least mean square (LMS)-prediction error filter (PEF) for online system identification. The presented solution is simpler than many other methods. However, there appears to be two limitations to this system. First, the scheme involves subjecting the system to a repetitive disturbance [4], which after many iterations the controller begins to learn. In this way, the control system "acclimatizes" to the disturbance [8]. Consequently, there is a risk of instability in the system due to an external non-repetitive disturbance to the system. Furthermore, in this scheme, only a proportional–derivative (PD) controller is considered, and this can yield a nonzero steady-state error [8]. For this reason, this paper attempts to build upon the PD adaptive controller scheme presented by Kelly. Specifically, an adaptive proportional–derivative+integral (PD+I) controller is presented to address some of the issues raised in this work. Different implementation methods are presented, and with dc–dc converter control in mind, emphasis is placed on achieving high-quality performance with a simple signal processing attitude.

This paper is set out as follows: The proposed PD+I adaptive control technique is outlined in Section II, while Section III presents the unique application of a DCD-RLS-PEF within the adaptive control structure. Section IV then provides a specific overview of the DCD-RLS algorithm. Following this, the relationship between a one-tap finite impulse response (FIR) filter and a PD controller is explained in Section V. Section VI presents detailed simulation results, highlighting the positive performance of the proposed technique. Section VII presents the experimental validation of the proposed solution and experimental comparison to conventional PID and adaptive LMS controllers. A method to further reduce the computational complexity of the scheme is then suggested in Section VIII. Finally, conclusions from the work are outlined in Section IX.

II. Control of a DC–DC Converter Using an Adaptive PD+I Controller

Fig. 1 shows a block diagram of the proposed control scheme. Here, a similar PD control method to Kelly and Rinne [14] is employed. However, a nonadaptive integral compensator is included in the feedback loop. This replaces a reference voltage feed-forward path in the original scheme. In this way, we look to achieve an adaptive PD+I controller. The integral compensator has a number of roles. First, during the initial convergence time for the filter tap weight, the integral compensator is used to excite the system. The integral effectively introduces a transient, which is then amplified. This, in turn, initiates an oscillation in the control error signal. The excitation signal improves the convergence time of the adaptive filter, the time to obtain optimal tap weight parameters. It also allows the adaptive controller to work continuously in an online mode. For all online identification methods, some form of perturbation of the system is essential for the identification and prediction process [1], [3], [5].

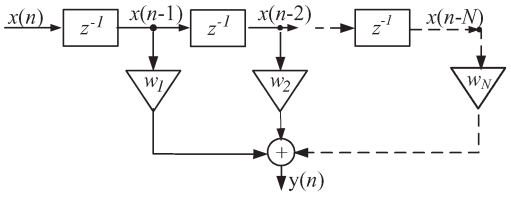

Fig. 2. One-step-ahead linear FIR predictor.

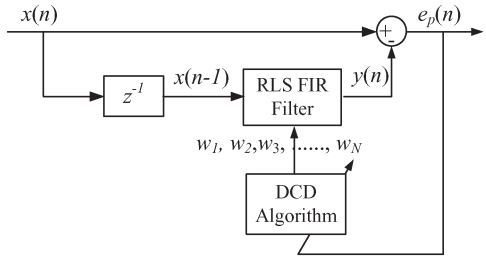

Fig. 3. Adaptive FIR linear predictor based on DCD-RLS.

The advantage of this scheme is that the adaptive PEF rapidly "learns" the behavior of the oscillation created by the integral compensator and rejects it from the control loop. Therefore, for the majority of the time, a smooth output response is observed. The oscillation in the output voltage response only appears for a very brief period of time, sufficient for identification purposes. The final purpose of the integral compensator is more obvious; it helps the output voltage regulation and ensures a zero steady-state error in the system. When actually choosing the value of integral gain K_I, a compromise exists between the magnitude of the excitation signal in the loop and the need to avoid unwanted LCOs [15], [16]. At the output of the PD compensator, a fixed gain (K) is included in the control loop (Fig. 1). This gain increases the excitation until the adaptive filter weight converges to the optimal value. For the buck converter system under consideration, $K = L/T$, where T is the switching period and L is the inductor value [14].

III. Adaptive RLS Linear Predictor Filter

A second alteration to the original algorithm in [14] is made by replacing the original LMS-PEF with an RLS-PEF. The classical RLS algorithm is used in many adaptive control strategies. Unfortunately, these schemes often require significant signal processing and microprocessor hardware to implement. This can be a problem in cost-sensitive systems. For this reason, the RLS algorithm is implemented using a fast, computationally light, and hardware-efficient adaptive algorithm, known as dichotomous coordinate descent (DCD) [17]. This algorithm has traditionally been developed for use in the field of telecommunications. Here, we adapt the algorithm and apply it for the first time in the adaptive control of power electronic circuits. In Fig. 1, the adaptive error predictor (stage 1 FIR filter) is responsible for the identification, or prediction, of the error signal [18]. The desired output is the minimization of this error signal. The FIR filter is implemented using a one-step-ahead linear FIR predictor, as shown in Fig. 2 [19].

This predictor consists of N unit delays and N tap weights. The output estimation $y(n)$ is the prediction of the present input signal $x(n)$. It is determined as follows [19]:

$$y(n) = \sum_{k=1}^{N} w_k x(n-k) = \mathbf{wx} \tag{1}$$

$$\mathbf{w} = [w_1\ w_2 \ldots\ldots\ldots\ldots w_N]$$

$$\mathbf{x} = [x(n-1)\ x(n-2) \ldots\ldots\ldots x(n-N)]^T. \tag{2}$$

To define the vector coefficients $\mathbf{w}$ of the linear prediction filter, analytical calculation of the linear system equations is required. This can be achieved using Wiener equations, but this requires considerable computational effort. Alternative methods, such as the Levinson–Durbin algorithm, can reduce the number of mathematical operations. Adaptive approaches can also be used to optimally calculate the tap weights and further trim the computational load [14], [19]. Fig. 3 shows the proposed DCD-RLS method of implementing an adaptive FIR predictor. The adaptive FIR predictor consists of two key components: a digital RLS-FIR filter which includes the tap weight coefficients previously described and the DCD algorithm which is used to vary the tap weight coefficients in real time. The DCD algorithm continuously adjusts the filter coefficients to minimize the error prediction signal $e_P(n)$. The error prediction is defined as

$$e_P(n) = x(n) - y(n) = x(n) - \sum_{k=1}^{N} w_k x(n-k). \tag{3}$$

According to (3), the error prediction signal is determined by applying the delayed input signal to the digital filter to produce the estimation output signal $y(n)$. The prediction error is then the difference between the desired signal $x(n)$ and this generated estimation output signal. To minimize the error signal, the adaptive algorithm must solve a series of linear equations to estimate the coefficient vector $\mathbf{w}$, where [20]

$$\mathbf{w} = \mathbf{R}^{-1}\beta. \tag{4}$$

Here, $\mathbf{R}$ is an autocorrelation matrix of size $N \times N$, and $\boldsymbol{\beta}$ is an element vector of length N. $\mathbf{R}$ and $\boldsymbol{\beta}$ are continually updated at each time instant n. For the proposed DCD-RLS, $\mathbf{R}(n)$ and $\boldsymbol{\beta}(n)$ may be described as follows [17]:

$$\mathbf{R}(n) = \lambda\mathbf{R}(n-1) + \mathbf{x}(n)\mathbf{x}^T(n)$$

$$\beta(n) = \lambda\beta(n-1) + z(n)\mathbf{x}(n). \tag{5}$$

In (5), λ is a forgetting factor which applies weighting to the previously calculated elements of $\mathbf{R}$ and $\boldsymbol{\beta}$. When $\lambda = 1$, the system behaves like the classical RLS algorithm. $z(n)$ is the scalar desired signal, which relates the actual adaptive filter output estimation $y(n)$ to the estimation error [17] $e(n)$ according to $e(n) = z(n) - y(n)$. Importantly, from a practical point of view, it is possible to find vector coefficients $\mathbf{w}$ without any mathematical division operations.

TABLE I
DCD ALGORITHM DESCRIPTION

Step	Equation
	Initialization: $\mathbf{h} = 0, \mathbf{r} = \boldsymbol{\beta}$, $d = H$, $k = 0$
	for $m = 1,....,M$
1	$d = d/2$
2	Flag = 0
	for $n = 1,....,N$
3	If $\lvert r_n \rvert > (d/2)R_{n,n}$
4	$h_n = h_n + sign(r_n)d$
5	$\mathbf{r} = \mathbf{r} - sign(r_n)d\,\mathbf{R}^{(n)}$
6	$k = k + 1$, Flag = 1
7	If $k = N_u$, algorithm stop
8	If Flag = 1, repeat for step 2

IV. DCD ALGORITHM

Least square estimation techniques are fundamental in adaptive signal processing applications. In real-time applications [20], the solution is normally based on matrix inversion, which is computationally heavy and presents implementation difficulties. However, there are alternative algorithms for solving the linear equations expressed in (4). Amongst them, the DCD algorithm appears to be a particularly effective method [17], [20], [21]. Attractively, the computation is based on an efficient fixed point iterative approach with no explicit division operations [21]. The DCD-RLS algorithm is only slightly more complex than the conventional LMS method; the DCD-RLS uses $3N$ multiplications per sample, compared to $2N$ for the LMS, where N is the length of the filter. It is also appropriate for real-time hardware implementation [21]. The overall computational requirement of the DCD algorithm depends mainly upon the number of iterations (N_u) used to update the parameter set. The number of iterations is very important for the speed and accuracy of the identification process [20].

Table I shows the operational steps of the DCD algorithm [17], [21]. For a more rigorous mathematical analysis of the algorithm, the reader is referred to the work originally presented by Zakharov *et al.* [17], [20], [21]. It is based on an iterative approach to estimating N parameters within an estimation parameter vector $\mathbf{h}(\mathbf{h} = \mathbf{w})$. Each parameter is assumed to reside within a defined amplitude range $[-H, H]$. Initially, the iteration step size d is chosen such that it equals H. Then, during each pass of the algorithm, the step size is halved ($d = d/2$, step 1). This division by two processes is very important from a hardware point of view. It allows a multiplication operation to be replaced with a more computationally efficient shift register [21]. The algorithm is performed using binary arithmetic. It starts the iterative search from the most significant bit M_b for each element in the parameter vector $\mathbf{h}$. Once complete, the algorithm determines the next most significant bit M_{b-1} and so on until M_0. At this point, the binary representation of M is fully updated. During each iteration, the magnitude of a residual vector $\mathbf{r}$ is analyzed. In the event that the residual is too small, the solution is not updated (step 3). If the residual is sufficiently large, one element of the parameter vector is updated (step 4) by adding, or subtracting, the value of d, depending upon the polarity of r_n. Following this, the residual vector $(\mathbf{r})$ is updated (step 5). The algorithm repeats this process until all elements in the residual vector $\mathbf{r}$ become small enough that the set condition in step 3 is met [21] or the number of iterations reaches a predefined limit number (N_u) [17]. The iteration limit may be used to control the execution time of the algorithm.

V. ONE-TAP LINEAR FIR PREDICTOR FOR PD COMPENSATION

A digital FIR filter can be described, in difference equation form, by (1). From this, it is possible to describe the digital filter in the z-domain as

$$Y(z) = X(z)(w_1 z^{-1} + w_2 z^{-2} + \ldots + w_N z^{-N}). \quad (6)$$

Referring to Fig. 3 and using (3) and (6), a FIR-PEF can therefore be represented in z form as

$$\frac{E_P(z)}{X(z)} = (1 + w_1 z^{-1} + w_2 z^{-2} + \ldots + w_N z^{-N}). \quad (7)$$

The order of the digital filter candidate model is application dependent. As described by Kelly and Rinne [14], [22], a second-order minimum phase plant, such as a buck converter, can be compensated using a typical moving average filter model (FIR or all-zero filter). Based on pole placement methods, the order of the moving average filter is one order lower than the plant. Hence,

$$\frac{D(z)}{E(z)} = \delta_0 + \delta_1 z^{-1} \quad (8)$$

where, δ_0 and δ_1 are the coefficients of the digital filter. By comparing (8) with (7), a low-order approximation FIR-PEF can actually be implemented as a gain controllable compensator [14]

$$\delta_0 + \delta_1 z^{-1} = K_d(1 + w_1 z^{-1}). \quad (9)$$

Equation (9) is equivalent to a PD controller. Importantly, it only requires one addition and one multiplication operation. A good quality regulator is required to optimally place the poles within the z-plane unit circle [14], [22]. This is the second purpose of the two-stage adaptive linear predictor shown in Fig. 1. In the first stage FIR, the adaptive algorithm places a zero (w_1) as close as possible to the dominant poles of the autorecursive model to minimize the error in the loop [23]. In the second stage, the adaptive algorithm estimates and adapts the gain (K_d) to minimize the prediction error in the adaptive filter. Conveniently, the adaptation of K_d is performed by the same mathematical process as the stage 1 FIR filter. However, here, the FIR filter uses the prediction error signal $ep_1(n)$ as an input signal [14], rather than the voltage error signal (Fig. 1). Finally, automatic adjustment of (K_d, w_1) reduces the variance of the prediction error and influences the final controller output duty signal. This PD controller is then incorporated with the integral compensator to form the PD+I structure. As a result, a low-complexity adaptive controller is achieved. This controller is capable of self-regulation, by finding and placing the optimal closed-loop poles in any system, without explicit knowledge of the actual circuit parameters.

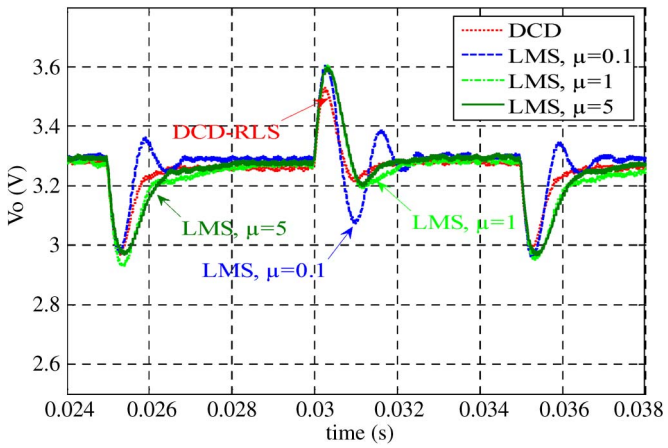

Fig. 4. Reference voltage feed-forward: Comparison of transient response between LMS and DCD-RLS. Repetitive load change between 0.66 and 1.32 A every 5 ms.

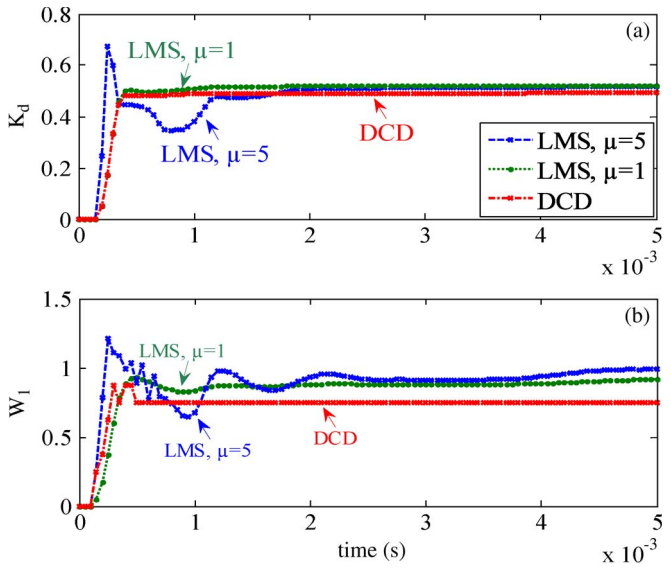

Fig. 5. Adaptation of gain (K_d) and tap weight (w_1) in the two-stage adaptive linear predictor.

VI. Simulation Results

To test the concept of the proposed DCD-RLS adaptive control scheme, a voltage-controlled synchronous dc–dc buck SMPC circuit has been simulated using Matlab/Simulink. The circuit parameters of the buck converter are the following: $R_O = 5\ \Omega$, $R_L = 63\ \text{m}\Omega$, $R_C = 25\ \text{m}\Omega$, $L = 220\ \mu\text{H}$, $C = 330\ \mu\text{F}$, $V_{\text{out}} = 3.3$ V, and $V_{\text{in}} = 10$ V. The buck converter is switched at 20 kHz using conventional pulsewidth modulation. The output voltage is also sampled at 20 kHz. For the DCD-RLS algorithm, the parameters are as follows: $N_u = 1$, $H = 1$, and $M = 4$ (number of bits). For completeness, the simulation model includes all digital effects, such as analog to digital converter (ADC) quantization and sample and hold delays. To present the viability of the proposed DCD-RLS algorithm, an equivalent system based on the conventional LMS adaptive controller presented in [14] is also simulated.

A. Reference Voltage Feed-Forward Adaptive Controller

Fig. 4 shows the initial comparison between the LMS with different step size (μ) values and the proposed adaptive DCD-RLS algorithm, using the original reference voltage feed-forward structure presented by Kelly and Rinne [14]. Both methods are able to maintain voltage regulation and recover from abrupt system changes. However, it is clear from Fig. 4 that the dynamic characteristics using the proposed DCD-RLS are much better than the conventional LMS. There is much smaller overshoot and a distinctly faster recovery time after a parametric change or when there is an increase in excitation. From this, we can deduce that the DCD-RLS method yields an overall improvement in the transient response of the system.

In LMS algorithms, the choice of step size (μ) may give rise to problems; one has to compromise between fast convergence rate and estimation accuracy. It is also compulsory to ensure that μ is within a range that guarantees that the filter tap weights will approach their optimal value [18]. This range is defined as

$$0 < \mu < \frac{1}{\lambda_{\max}}. \tag{10}$$

Here, $\lambda_{\max}$ is the largest eigenvalue of the autocorrelation matrix $\mathbf{R}$. However, a first-order PEF filter is proposed; thus, the value of λ is simply equal to $R(1)$, and μ mainly depends on the maximum input signal value. For this specific example, the optimal step size value is when $\mu = 1$. The adaptive gain (tap weight) of the LMS predictor filter, the convergence time, the tap-weight gradient noise, and the stability of the adaptation all depend heavily on μ. Large values of μ decrease convergence time and improve the dynamic response as shown in Fig. 4 but increase the filter gradient noise and vice versa for low values of μ [14].

Fig. 5 shows the adaptation performance of the LMS and DCD-RLS algorithms. In both methods, the tap weights approach approximately the same values, and the zeros of (9) lie inside the unit circle of the z-plane. Hence, a minimum phase PEF filter is created and the stability criterion may be fulfilled [24], [25]. However, the DCD-RLS is superior in terms of convergence time and effect of gradient noise on the determination of the adaptive gains. As a result, the choice of step size is important for dealing with unexpected system disturbances. For example, in SMPC applications, one might observe a high control error signal, due to a high initial transient or an abrupt change in load current; if the step size is large, instability may arise. This is demonstrated in Fig. 6, where a significant change in load current (1.3–6.5 A) is observed at 25 ms. It can be seen that, when $\mu = 1$, the converter output voltage collapses due to loss of control. In this particular case, a lower value of μ is required to cope with this disturbance, as shown when $\mu = 0.1$. Alternatively, a signal conditioning unit (an attenuator or rate limiter) may be included before the LMS filter. However, this will also slow down the convergence rate and the overall final response of the system. This problem is eliminated through the use of the DCD-RLS algorithm, since it is independent of any step size parameter.

B. Voltage Control Using Adaptive PD+I Controller

In this section, the adaptive PD+I controller initially discussed in Section II is implemented. Fig. 7 shows the

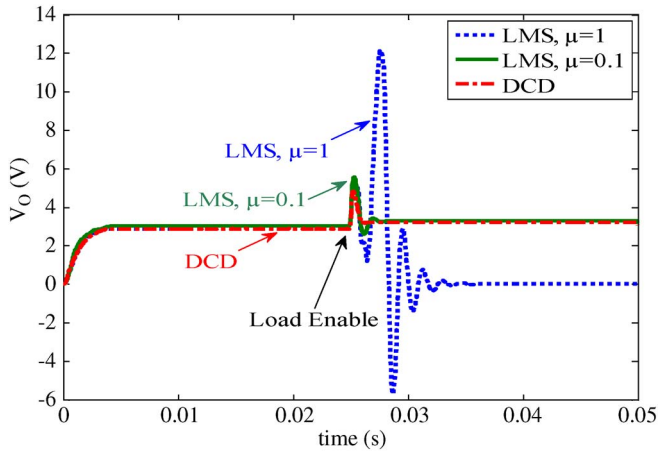

Fig. 6. Comparison of transient response between LMS and DCD-RLS. Significant change in load current (1.3–6.5 A).

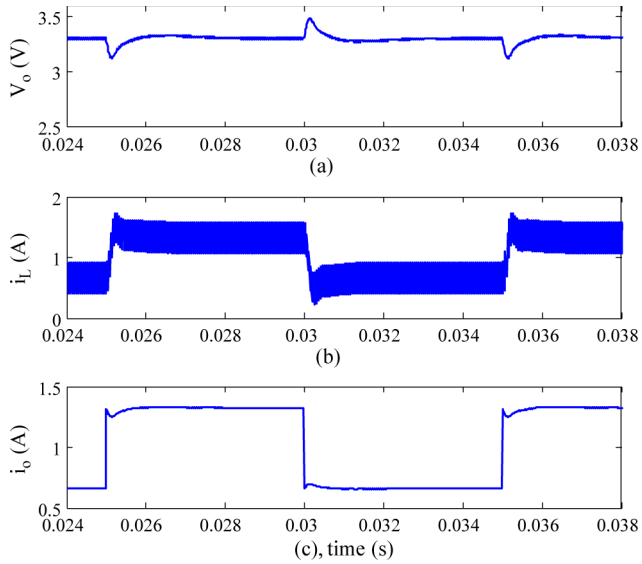

Fig. 7. Transient response of the proposed adaptive controller. (a) Output voltage. (b) Inductor current. (c) Load current. Load current change: 0.66–1.32 A every 5 ms.

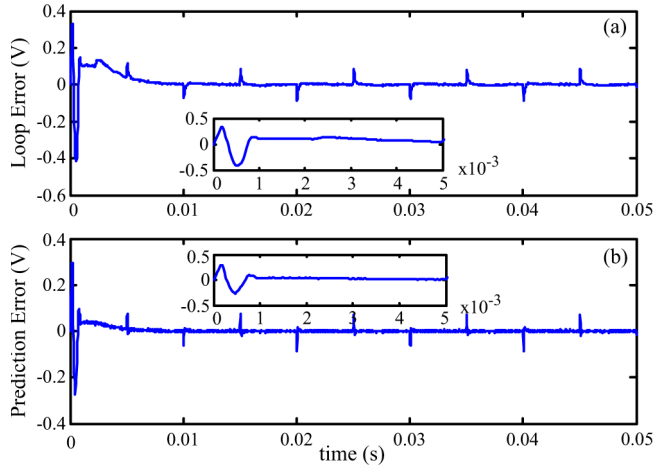

Fig. 8. Error signal behavior during adaptation process. (a) Loop error. (b) Prediction error (ep_1). Load current change: 0.66–1.32 A every 5 ms.

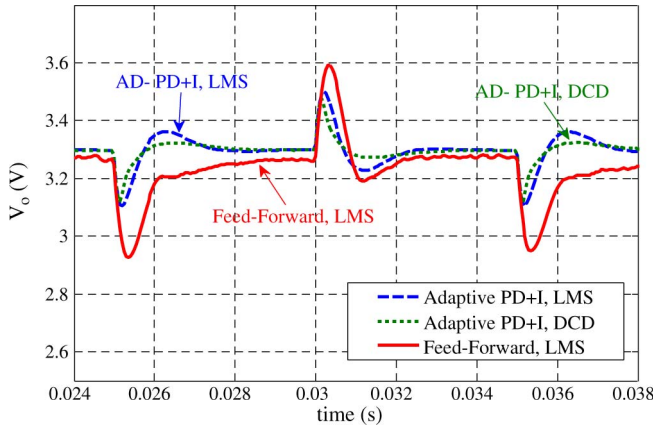

Fig. 9. Transient response of the proposed adaptive PD+I controller using DCD-RLS or LMS and the comparison with the reference voltage feed-forward scheme using LMS $(\mu = 1)$.

performance of placing the integral compensator (see Fig. 1) in the feedback loop to increase the excitation of the adaptive filter and drive the steady-state error to zero, hence improving the identification accuracy of the adaptive filter. To investigate the robustness of the algorithm to system disturbances, a load change is introduced into the system. This load change forces the load current to switch between 0.66 and 1.32 A every 5 ms (Fig. 7). Usually, the performance of adaptive methods and self-tuning controllers is measured using particular metrics. A cost function is one metric that can be used to describe the performance of a PEF. The benefit of using a PEF is that a cost function naturally exists. The optimum cost function for a PEF is actually the minimization of the prediction error signal power required to reduce the loop error to zero. It is clear from Fig. 8 that the algorithm is capable of minimizing the prediction error power; thereby, a well-regulated output voltage is ensured. However, the main role of the PEF is to continuously work alongside the adaptive algorithm to minimize the prediction error. This, in turn, improves the prediction and identification of the input filter.

The conventional LMS method can be applied with the adaptive PD+I structure to provide enhanced performance over the previous reference voltage feed-forward method (Fig. 9). With the introduction of the integrator into the control loop, the loop excitation is increased, and this helps the identification process. However, as mentioned earlier, careful attention must be given to the selection of the step size μ. Fig. 9 also shows the equivalent performance of the PD+I structure using the DCD-RLS technique. Once again, it is clear that the DCD-RLS approach provides superior performance and is not a function of step size.

The trajectory path of the adaptive filter coefficients can be represented by combining the two weights of the PEF into one coefficient vector. Here, both cascade FIR filter coefficients are responsible for the minimization of the prediction error. Fig. 10 shows the trajectory paths, in the vicinity of the optimal point, on the mean-square-error surface. It is noticed that the weights of the DCD-PEF algorithm move toward the optimal values using much larger increments. Therefore, the minimization of error prediction is much faster than the LMS-PEF.

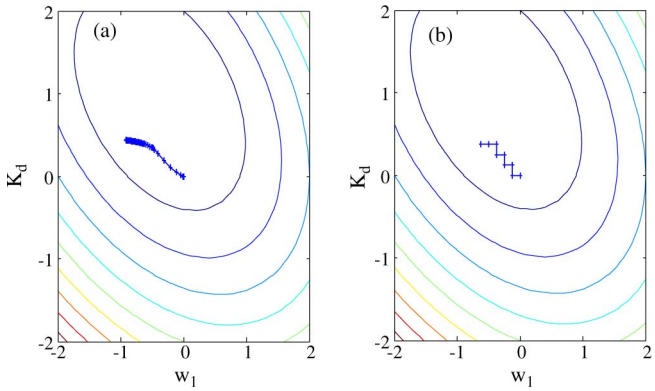

Fig. 10. Trajectory paths of the adaptive filter coefficients. (a) Adaptive PD+I, LMS. (b) Adaptive PD+I, DCD-RLS.

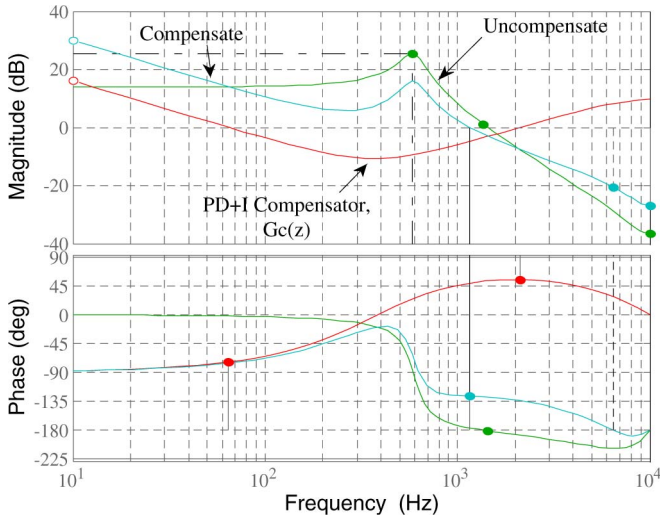

Fig. 11. Frequency response of the PD+I compensator and the compensated/ uncompensated open-loop gains.

Often, SMPC controller behavior is also expressed in terms of frequency response criteria. The frequency response of the proposed adaptive controller is shown in Fig. 11. Here, it is shown that the phase margin of the compensation system is increased through the introduction of the first-order FIR-PEF (PD compensator) into the loop. The phase margin of the adaptive PD+I compensator is 53°, and the gain margin is 20.6 dB. Furthermore, the versatility of the proposed PD+I adaptive controller has been tested with other converter circuit parameters, to represent alternative dc–dc converter designs. It has been evaluated with higher switching frequency systems and compared with nonadaptive control systems such as the classical digital proportional–integral (PI) controller [26]. In each case, the proposed adaptive controller shows very promising results and can handle a wide range of uncertainty in the SMPC parameters.

VII. Experimental Validation

To fully validate the proposed control system, an experimental synchronous dc–dc buck converter has been designed and tested for 5 W operation. For comparison with the simulation results, similar parameters and component values to those outlined in Section VI are chosen. A Texas Instruments TMS320F28335 digital signal processor (DSP) platform is used to implement the digital adaptive control algorithm. The DSP has onboard digital pulsewidth modulation and 12-b A/D converter channels. Initially, a conventional PID voltage controller is implemented on the experimental hardware. The PID is set to control the buck converter output voltage at 3.3 V. This serves as a benchmark for testing the DCD-RLS method. The PID gains are optimally tuned using the well-recognized pole-zero matching techniques previously presented in the literature [8], [27]. The transient characteristics of the PID controller are determined by applying a repetitive step change in load to the buck converter. This step change causes the load current to switch between 0.66 and 1.32 A at 25 ms intervals. The results, shown in Fig. 12, demonstrate that the buck converter is always operating in continuous current mode. The output voltage transient shows significant oscillatory behavior at the points of load change.

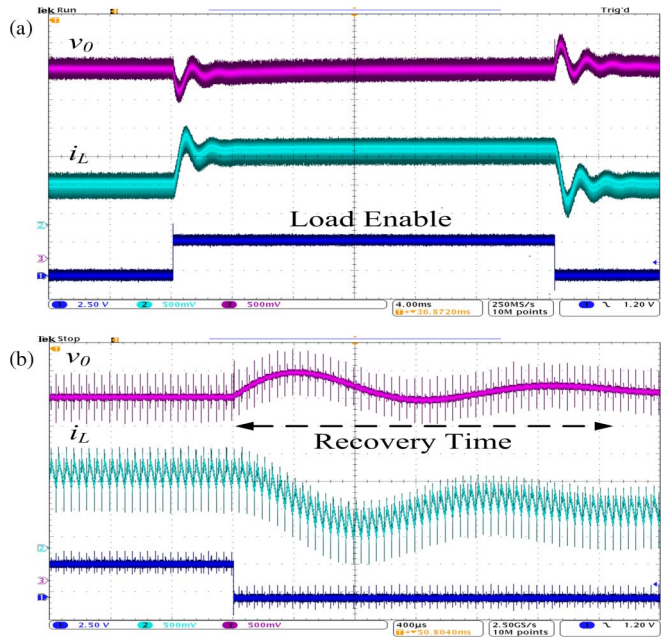

Fig. 12. Transient response of PID controller with abrupt load change between 0.66 and 1.32 A. (a) 4 ms/div: showing two transient changes. (b) 400 μs/div: "zoom-in" on second transient.

Following this, the DCD-RLS adaptive algorithm is implemented on the DSP. For consistency, all circuit parameters remain the same, and the buck converter is subjected to the same load change as previously described. The experimental results, shown in Fig. 13, are in excellent agreement with the simulation results in Fig. 7, thus confirming the successful practical implementation of the proposed DCD-RLS control scheme. Compared to the experimental results achieved with the conventional PID controller, the DCD-RLS scheme yields significantly improved transient performance for the same dynamic load change. The DCD-RLS method demonstrates lower transient overshoot, significantly less oscillatory behavior, and faster recovery time.

Finally, the LMS adaptive controller is implemented on the DSP. Here, each DCD-RLS in Fig. 1 is replaced with

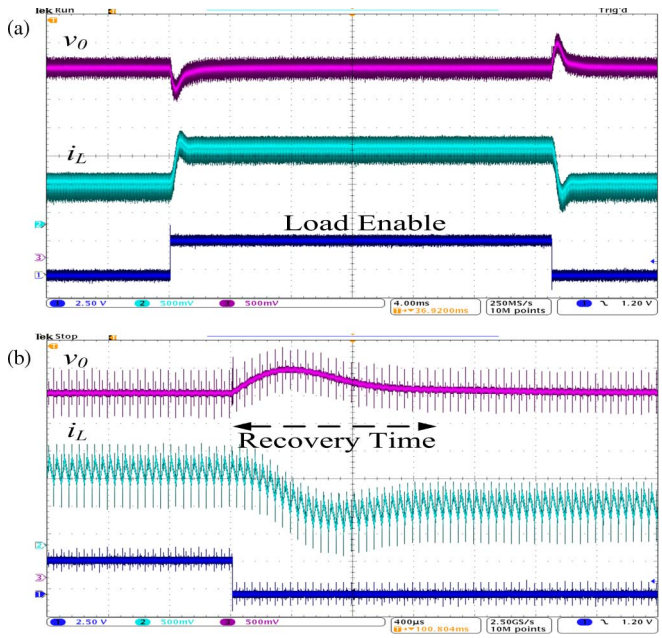

Fig. 13. Transient response of adaptive PD+I DCD-RLS controller with abrupt load change between 0.66 and 1.32 A. (a) 4 ms/div: showing two transient changes. (b) 400 μs/div: "zoom-in" on second transient.

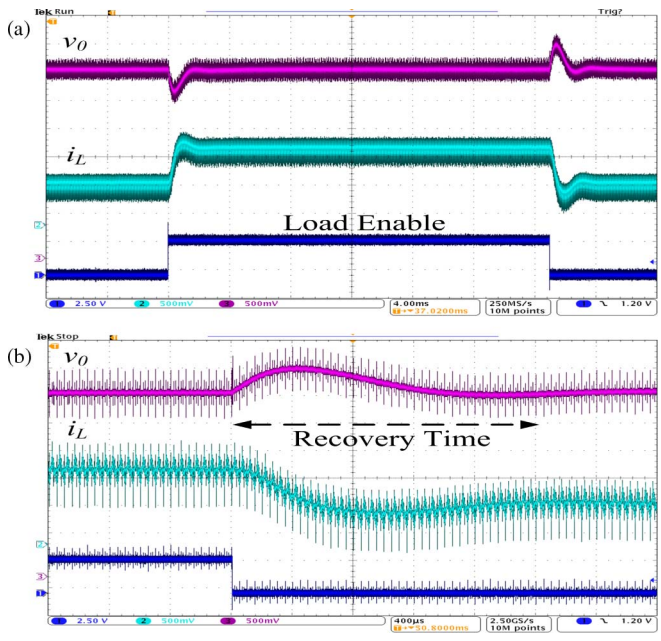

Fig. 14. Transient response of adaptive PD+I LMS ($\mu = 1$) controller with abrupt load change between 0.66 and 1.32 A. (a) 4 ms/div: showing two transient changes. (b) 400 μs/div: "zoom-in" on second transient.

an adaptive LMS filter. As previously described, with the LMS-PEF (stage 1), there is a need to define the step size (μ), in accordance with (10). A range of step sizes has been experimentally tested, and in agreement with the simulations, optimal values of $\mu = 1.0$ are selected. Again, the same set of system parameters is used, and the experimental results are shown in Fig. 14. These results are a good match to the initial simulation waveforms shown in Fig. 9. Compared to the conventional PID controller, the adaptive LMS controller offers

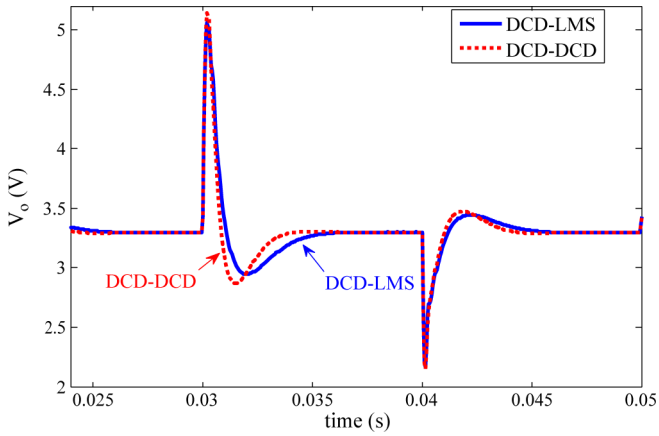

Fig. 15. Load transient response at significant change in load current, with two-stage DCD–DCD adaptive controller and hybrid DCD–LMS adaptive controller.

improved transient performance. However, as predicted by the simulation results and confirmed experimentally, the DCD-RLS offers superior dynamic performance over the LMS.

VIII. Complexity Reduction

In most applications, there is a tradeoff between the dynamic performance and computational complexity (i.e., speed of execution) of the controller. This paper has presented two solutions, each giving a different weighting to these two important performance indicators. The LMS is designed for good dynamic performance with low computational complexity, while the DCD-RLS is designed for optimum dynamic performance. The DCD-RLS is a computational-efficient algorithm compared to the classic RLS schemes, but it is acknowledged that a higher computational burden than the LMS exists. For this reason, the overall system complexity of the proposed DCD-RLS scheme (Fig. 1) can be reduced by exchanging the second stage DCD-RLS for a classical LMS-PEF. The first stage DCD-RLS still remains in place. In this way, we develop a "hybrid" DCD-RLS:LMS control scheme.

This change does not appear to significantly compromise the behavior of the system response with respect to convergence time, identification accuracy, and control error signal power, even during the initial transient or due to a significant change in the system parameters. When the first stage is faced with a high error signal, the DCD-FIR filter influences the prediction error signal. This prediction error signal is then passed onto the second stage LMS-FIR filter to adapt the tap weights and adaptive gain. The simulation results from DCD-RLS:LMS system are shown in Fig. 15 (load change: 1.3–6.5 A). The experimental results are shown in Fig. 16 (load change: 1.32–0.66 A). Here, the same conditions have been used as those originally specified in Section VII. While it is apparent that the dynamic performance of hybrid DCD-RLS:LMS is not quite as good as the originally proposed two-stage DCD–DCD algorithm, it still achieves an excellent response (as shown in Fig. 15). For this reason, in systems where computational complexity may be an issue, this gives a good compromise solution. Also, in this particular

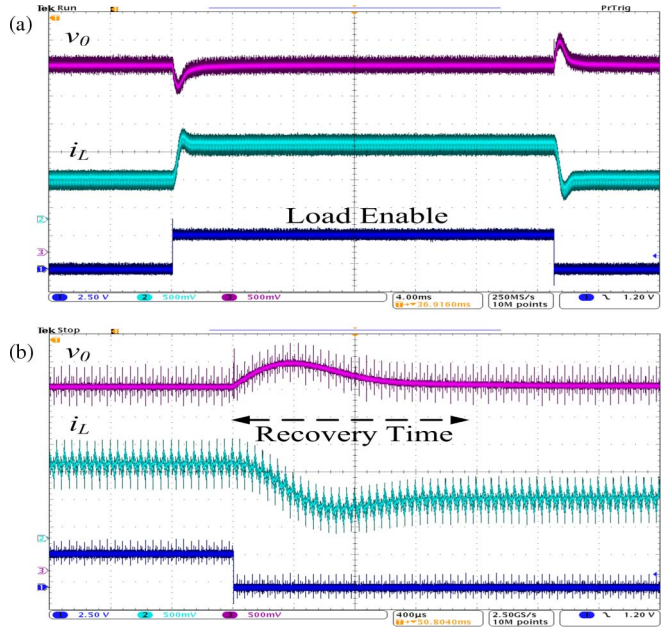

Fig. 16. Transient response of hybrid DCD-RLS:LMS ($\mu = 1$) adaptive controller with abrupt load change between 0.66 and 1.32 A. (a) 4 ms/div: showing two transient changes. (b) 400 μs/div: "zoom-in" on second transient.

configuration, it is possible to use a larger value of step size μ and still obtain acceptable performance.

IX. Conclusion

In the area of adaptive control and system identification, RLS methods provide promising results in terms of fast convergence rate, small prediction error, and accurate parametric estimation. However, they often have limited application in low-cost applications, such as SMPCs, due to computationally heavy calculations demanding significant hardware resources.

This paper has demonstrated the feasibility of an adaptive PD+I controller for the output voltage regulation of a dc–dc converter. The adaptive control system uses a two-stage FIR filter and integral controller. A computationally efficient DCD-RLS algorithm is used to implement the adaptation mechanism. This algorithm overcomes many of the limitations of classic RLS methods, making it well suited for power electronic applications. The controller has the ability to work continuously in the feedback loop and rapidly minimize the controller error signal by finding real-time tap weights for the FIR filter. The integral controller generates an amplified oscillation in the feedback loop for a very short period of time to increase the excitation for prediction and identification purposes. The adaptive filter parameters quickly converge and eliminate this oscillation. In this way, the approach is suitable for two important purposes: prediction/identification and controller adaptation.

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