EPSRC Grant JOINT FINAL REPORT

asynchronous COmmunication Mechanisms FOr Real-Time systems (COMFORT)

GR/L92471 (King's College London): 1/4/1998 to 31/7/2001
& GR/L93775 (Newcastle University): 17/5/1998 to 17/11/2001

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Background/Context

There are at least two contexts in which distributed multi-processor real-time (R-T) systems present increasingly difficult technical challenges to continuing the 'synchronous-digital-design' methodology that has been standard practice for many years: (i) complex systems where the parts are widely spaced (and often in relative motion) cannot easily operate with a common clock and (ii) advances in integrated circuit technology are leading to a capability to integrate huge numbers of high-performance processors on a single chip, and commercial pressures are ensuring that these complex components will be utilised in many future systems. The increased speeds and reduced feature sizes make it increasingly problematic to distribute a common clock around such integrated circuits.

As a result, there is increased interest in trying to design systems in an asynchronous manner – the potential advantages and the difficulties have been known for many years, and so far, many digital systems designers are not yet convinced of the need to abandon the synchronous design philosophy, but it appears likely that in the two contexts referred to above, there is a good potential for improving performance by a change to an asynchronous design philosophy. An intermediate approach (Globally Asynchronous, Locally Synchronous, known as GALS) is widely expected to become popular.

It is within all these contexts that asynchronous communications arise, with a requirement for a reliable means for data transfer between their data-processing subsystems. Traditional techniques using handshakes and message-passing protocols have limitations with regard to important R-T requirements including safety and temporal predictability.

Asynchronous data communication mechanisms (ACMs), however, offer a number of advantages as data links between subsystems, including providing full temporal independence for one or both of the communicating sides.

The COMFORT project has contributed to a number of advances in the theory and practice of ACMs. Particular emphasis has been on: (i) improving the modelling and analysis techniques for ACMs; (ii) developing and improving systematic approaches to ACM design; (iii) investigating automatic synthesis of ACMs; and (iv) implementing and testing example ACM hardware initial investigations have been made into system construction using ACMs as the "glue" between subsystems.

This research has been closely linked with a number of ongoing projects being conducted in both NU and KCL. These include one concerned with the synthesis of systems with heterogeneous timing, with emphasis on multiprocessor R-T systems, one concerned with the visualization aspect of asynchronous system design, and one in the field of nonlinear dynamics.

The COMFORT project results have been reported in over 40 academic publications, including PhD theses, book chapters, technical reports, and journal and conference papers, and in seminars presented at various universities. The technical advances have been made available to Matra BAe Systems via our close collaboration with them, and to other academic and industrial partners through our deep participation in the asynchronous systems community in the UK (Asynchronous UK Forum), EU (ACiD Working Group), and worldwide (annual ASYNC symposia and the asynchronous mailing list) and the general circuits and systems community (annual ISCAS symposia and various other IEEE meetings). Furthermore, through its initiation and planning of an international workshop (AINT'2000) in Delft, Netherlands, the COMFORT project contributed to the wider exposure and understanding of ACMs among such industrial companies as IBM, Intel, and Philips.

Key Advances and Supporting Methodology

The original objectives of the project were specified in a number of tasks and sub-tasks. These are repeated here along with our contributions to each one. We also published an end of first year report to highlight our progress through the tasks [30]. In our proposal a report was also specified at the end of each task, but this has become unnecessary because the results of all tasks are covered by our publications.

Task I: Methods and tools for formal modelling and rigorous analysis of ACMs

Task I.1: Development of Petri net modelling strategy, experimenting with existing ACMs

This task started with an extensive literature search soon after the start of the project. This search revealed relevant work previously unknown to us by several authors, and more importantly gave us references to new terminology. New indexing terms relevant to asynchronous communication included wait-free communication, atomic communication and non-blocking communication. Our interest in ACMs and in metastability had origins in a 12 month Royal Society Industrial Fellowship held over a decade ago by the KCL Principal Investigator at the then Army Weapons division of British Aerospace. The contacts made at that time were maintained, and led to the industrial support for this project from Matra BAe. This support and collaboration had given us a very good initial understanding in this field, but the literature search allowed us to widen our

views and concepts and to create an online bibliography of asynchronous and wait-free communication mechanisms has been created (www.eee.kcl.ac.uk/~comfort).

The representation of ACMs in various forms, and our awareness of the MASCOT method, showed us how MASCOT networks could be represented by Petri nets (PNs) and vice versa, and this laid the foundation for representing ACMs using PNs [25]. This in turn led to the development of a novel computer based tool for checking the properties and correctness of ACM designs in a uniform manner. Prior to this, each published design had been analysed and/or verified by its author using methods specific to that design. The nature of ACMs is such that very small changes in details (some of which may seem of no serious consequence) can invalidate the correctness. Some of the designs are deceptively simple, but making a complete evaluation of their properties and a proof of correctness under all timing constraints and conditions presents a challenging problem. We also made some preliminary studies of the impact of metastability on some of the ACMs, and this interest in metastability also led to some contributions to the analysis of multi-way arbiter circuits [18,32].

By representing ACMs with PN models, the extensive theory of PNs is available to investigate properties, and reachability searches may be used to test for incorrect behaviour. We have also made significant input to the theory of hardware and PNs via the HWPN conference [36,22,43], and the modelling and verification of concurrent Ada programs using PNs [13]. Because exhaustive searches can be completed in a moderate time on a modern workstation, it is possible to both make conclusive claims about correctness can be made and the particular timing sequences which can cause failure of an incorrect design can be identified. As explained below (Task I.3), specially developed search tool was used instead of standard tools for reachability analysis.

A PN modelling technique was developed for the analysis of Pool type ACMs [16,25] and used to model all of Simpson's algorithms [16,25,28] and others including those from Peterson, Kirousis, Anderson & Gouda, and Tromp [16]. Using the same modelling and analysis techniques for all the ACMs enabled the different algorithms to be compared in a meaningful fashion [12,16] for the first time. Models for stochastic analysis of ACMs have also been developed [26], making it possible to study ACM properties quantitatively. Extensions to the ACM protocol taxonomy [7] have produced refined versions of Signal and Message type ACMs and algorithms for their implementation [4,8], as well as Channel type ACMs [38,42].

The application of ACMs to system design and systems on chip design has been investigated by introducing the concepts of Heterogeneously Timed Systems (HETS) [7].

Low level PN models have also been produced to investigate how different algorithm implementations are affected by hardware failures and phenomena such as metastability [16]. Further details are described below (Task IV).

Task I.2: Formal capture of main properties (data consistency and freshness); development of analysis techniques

The concepts of Data Coherence and Data Freshness were introduced by Simpson in his early papers. He investigated these properties using his 'role model' method. These were then complemented by another property called 'Data Sequencing' in a later Simpson publication.

Data coherence is maintained if individual data items are atomic during transfer from the writer to the reader. Data Freshness is maintained if the reader always obtains the most up to date data item from the ACM. Data sequencing is maintained if the reader obtains data items in the same order as the writer provides them. These are the main data-correctness properties, and have been partially used in varying forms by all the ACM designers mentioned above. We have extended the use of these properties and formalized their definitions by using PN modelling techniques. This has allowed us to analyse them in more detail [10,16,23,25,27,41,44].

More recently we introduced the property of data latency [4], which is concerned with the time delay between writing an item of data into a mechanism and being able to read that item. We have also analysed in quantitative detail the previously largely ignored properties of data loss and data re-reading [26], gaining important insights about the suitability of each type of ACM for specific applications.

Task I.3: Development of algorithms and software for validation of ACMs

ACM algorithms are in general endless loops. This cyclic nature causes problems during standard Petri net analysis. At the time of the initial research into PN models of ACMs a study of the freely available analysis tools was made. No tool found during this survey was able to deal with this problem effectively. Several of the tools available at the time were graphical entry tools, and these did not lend themselves to easy model entry and checking or design re-use. Other tools available used unnecessarily complicated temporal logics, which confused the modelling issues and also meant that the analysis was far less efficient. Therefore a dedicated tool called 'Reach' was implemented [16,29]. This tool performs a simple reachability search but avoids becoming stuck in endless loops by keeping a list of all visited states. It has also been tuned to output PN model states in forms which aid the visualisation of any error conditions encountered within an algorithm, and to focus on checking data coherence, freshness and sequencing.

Stochastic PN models and techniques have also been employed to highlight operating characteristics of the ACMs not shown up by the state space analysis approach [26,39].

Task II: Methods and tools for synthesis of ACMs for hardware implementation

This task is closely related to Task V.

Task II.1: Development of techniques for hardware (Self timed and (a)synchronous) implementation from Petri net models of ACMs

Manual or direct implementation has been performed from some of the algorithms without going via PN models, resulting in relatively high-level, conceptual circuit schematics [1,12].

Implementation from the PN models of ACMs using more systematic approaches has produced more detailed and interesting results. One approach was to employ the 'direct translation' technique using a 'David cell' to represent each Petri net place, therefore producing a straightforward implementation of the PN model in hardware. Versions of Simpson's 3 and 4 slot Pool algorithms have been produced and investigated using this technique [21]. The second approach to PN model implementation was through logic synthesis using the 'Petrify' tool resulting in logic equations which can be implemented using self-timed logic hardware. A 3 slot Pool [10], and a 4 slot Pool [17,33] have been implemented using 'Petrify'.

Synthesis techniques for other forms of ACMs have also been investigated with the production of algorithms and hardware implementations for a 'non-blocking' FIFO [38,40,42], and also Signal and Message type ACMs [3,6].

Designs have been fabricated in silicon (jointly with the EPSRC HADES project GR/K70175), incorporating several different Pool type ACMs [5]. These have all been tested using embedded testing hardware included on the chip [9].

Task II.2: Advancement of existing software tools for self timed control logic synthesis

During the course of this research project, logic decomposition of speed independent circuits was also investigated within the framework of the 'Petrify' tool and involved collaboration with many top level researchers in this area [37].

Task II.3: Logic design of major building blocks for hardware implementation

Several core components used within ACM hardware have been investigated and implemented. A number of novel forms and variations of such circuits as latches, David cells, D elements and C elements have been developed which have special significance in ACM implementations [6,10,17,21,34]. These new elements invariably have reduced metastability effects and faster operation. Many new design techniques for such circuits have also been developed.

Tri-flops and multi-flops have been investigated for their application as multi-way arbiters, and their metastable characteristics have been studied [18,32]. More complex forms of arbiter circuits have also been investigated, including dynamic priority arbiter with FIFO [15], priority arbiters [20], and high speed arbiters [24]. Considerable existing knowledge from the EPSRC HADES project was beneficial in this area.

The NU COMFORT PhD student Delong Shang has made considerable novel input into this area of the research, and is currently writing his thesis entitled "Self timed realisations and testing of real time communication protocols".

Task II.4: FPGA prototyping for hardware implementation

During the course of this project, some shared VLSI silicon space was made available jointly with the EPSRC HADES project, allowing us to leapfrog an FPGA stage and go directly to silicon for high-profile, solid results [21]. The embedded testing circuits included on chip provided some of the verification opportunities of a would-be FPGA approach [9].

In addition, an FPGA demonstrator specification was developed during the course of the project, and this may be implemented during the course of the subsequent joint EPSRC COHERENT project (see below in Further Research).

Task III: Development of specification/model conversion tools

Through academic information exchanges we became aware of other investigators pursuing this line of work. Since some of that work had already made good progress, we decided not to commit major project resources to this task. In addition, with the progress of our project, we gradually moved away from the idea of emphasizing VHDL as a design tool, primarily because of the poor support for asynchronism in the language at the time. Much of the hardware level work has been done within Cadence using analogue components. As a result, a number of conversion tools not restricted to conversion between PN and VHDL have been developed instead as they become needed.

Task III.1: Petri net to VHDL translator

One published example of a Petri net to VHDL translator which we discovered is [D. Prothero – "Petri net modelling and implementation using VHDL" [SBU-EEIE-98 report, also HWPN Lisbon 98. pp 154-167]. Students affiliated with COMFORT completed two conversion tools [N. Baxter, STG to VHDL conversion NU BSc dissertation 1997; L. Guo, ASTG to BLIF (Berkeley Logic Interchange Format) conversion, NU MSc dissertation 2000]. These can both be regarded as additional deliverables from COMFORT.

Task III.2: VHDL to Petri net translator

Significant work on translation/conversion of HDL's to PN and other related formats has also been discovered through our contacts with other researchers in the field. Work on behavioural VHDL is very advanced within the AMULET group in Manchester [http://www.cs.man.ac.uk/amulet/publications/papers/date98.html]. Other such work includes [P. Vanbekbergen, A. Wand, and K. Keutzer "A Design and Validation System for Asynchronous Circuits" Proc. ACM/IEEE Design Automation Conference, June 1995] and translation from Verilog to PNs [I. Blunno and L. Lavagno "Automated synthesis of micro-pipelines from behavioural Verilog HDL" Proc. International Symposium on Advanced Research in Asynchronous Circuits and Systems, pp. 84-92, IEEE Computer Society Press, April 2000]. Part of the MASCOT to Petri net link found in [25] can be regarded as a COMFORT deliverable within this task.

The VHDL to PN link is now being investigated in depth at NU via the EPSRC BESST project which concentrates on system synthesis.

Task IV: ACMs for safety-critical embedded real-time applications, metastable operation, failure modes, analysis and impact

Task IV.1: Analysis of metastability and its effects on implementation behaviour

At the same time as the initial literature search of Task I, an extensive literature search was performed on the subject of metastability. Metastability is an unavoidable risk in any asynchronous hardware, and results in unpredictable output conditions from hardware latches. A substantial database of Metastability references has been accumulated and has been made available via another online bibliography (www.eee.kcl.ac.uk/~comfort).

At the time of this literature search VHDL and VERILOG standards were being produced which included Multi-Valued Logic (MVL), which included labels for various levels of logic state, i.e. 'Z' for high impedance. This provided the idea of a logic level 'M' for Metastable. This was introduced in to our PN models to provide a high level representation of this phenomenon [45]. This state space based Metastability modelling technique was then used during comparisons of several ACM algorithms to see how each was affected by this unavoidable state [16]. Significant insights were also gained into the design and operation of these algorithms, which allowed the production of design guidance hints for ACMs [16].

Metastable operating conditions were also investigated at the level of the dynamic behaviour of the circuits for standard latches with one feedback loop [35] and for latches involving more than one feedback loop, known as Tri-flops for a three-way arbiter, and, in general Multi-flops [18,32]. Other low level components investigated under metastable operation were arbiters [35], fair arbiters [15], synchronisers [19], and A-D converters [35] with significant findings.

Complete self-timed ACM algorithms were also simulated at the low level in the analogue domain under metastable conditions. These self-timed ACMs were constructed using arbitration circuits to prevent variables in the control algorithms from operating under metastable conditions [38,40,42,33].

Task IV.2: Analysis of failure conditions (partial failure), effects of redundancy

In addition to the effects of metastability and conditions under which it may cause failures, we have also included in our analyses of ACMs the effect of random errors in signals where metastability may or may not occur. This has been made possible by the effective modelling and analysis techniques we have developed during this project. Studies which fall into this category can be seen in [16,25].

Task V: Towards synthesis of multi-slot algorithms for asynchronous communication from formal requirements

This task has been very successfully combined with Task II.

Task V.1: Study into techniques for synthesis of parallel algorithms and discrete event controllers

Extensive investigations have been made into the eventual automatic synthesis of control circuits for ACMs at NU. Techniques developed or enhanced during this work include direct translation from STGs to David cell based circuits, optimal use of Petrify, and new types of special asynchronous circuits. In the algorithmic front, work has begun whereby ACM algorithms may be automatically synthesized from Petri net specifications. Several publications in major conferences as well as a journal have resulted from this work [3,6,7,17,21,31].

Task V.2: Investigation into synthesis of Petri net models of ACMs satisfying given correctness and performance requirements

At NU, advances have been made in synthesizing Petri net descriptions of ACMs from state space specifications using regions theory [3,31]. The synthesis method developed is step by step and quasi algorithmic, with good potential for automatization. This is part of the process of synthesizing entire ACM algorithms from basic specifications [3,6,7]. This method breaks new grounds for not only ACM synthesis but also related asynchronous systems synthesis and has potential use in a much wider context.

At KCL, two tools have been under initial development to facilitate the synthesis and analysis of ACMs. One (AutoACM) will automatically generate ACM algorithms from a given instruction alphabet and the other (ACM2PN) will automatically convert any ACM algorithm to its Petri net model. They continue to be developed under our new joint EPSRC project COHERENT— GR/R32895 and GR/R32666.

Research Impact and Benefits to Society

We consider this research to have been very successful. All of the tasks have been completed and in many cases the results exceeded original expectations considerably. The extensive list of publications [1-45] is a tangible measure of output. It is our intention to prepare and submit additional papers based on various results from the project and to continue research work in this area as part of our new joint EPSRC project COHERENT GR/R32895 and GR/R32666.

Explanation of Expenditure

The expenditure plans in our original research proposals have been followed with only minor deviations. Two full time RAs were employed; one each in KCL and NU, and a 10% RA was also employed at KCL. The NU PhD studentship was awarded to Delong Shang, currently writing his thesis. Equipment purchased on the grant was as originally stated, with the exception that KCL used some equipment budget planned for FPGA demonstrator hardware for an additional conference visit. This is explained elsewhere in this report.

Because of the time spent in finding a suitable candidate for the PhD studentship at NU, the project completion date at NU was extended for six months. The EPSRC also kindly extended the completion date at KCL by three months to allow the registration fee for a conference after the original end date to be charged to the grant. The KCL PI was invited to give a plenary lecture at the conference on a topic related to this project. This extension made it possible for other KCL personnel continue to work on this project until the start of the subsequent COHERENT project— GR/R32895 and GR/R32666.

Further Research/Dissemination Activities

The research outcome from this grant is directly applicable in the fields to real-time distributed systems, GALS and Systems on a Chip (SoC). It is of benefit to two new EPSRC grants, one held jointly between Manchester University and Cambridge University investigating GALS systems, and the second held jointly between NU and KCL (COHERENT — GR/R32895 and GR/R32666). The techniques used for analysis of ACM correctness and data properties are being investigated by British Aerospace as useful additions to their existing techniques, offering new insights into this type of mechanism.

The research into the analysis of ACMs correctness and data properties has for the first time allowed direct comparisons to be performed between different ACM algorithms. In the past, individual authors have developed their own methods and techniques specific to testing their own algorithms. The approach used here has drawn on existing standard Petri net techniques and will allow the simple analysis of any ACM algorithm including any which may be published in future literature.

The study of the synthesis of ACMs, both at the hardware level and at the level of algorithms, breaks completely new ground and has provided enough momentum for us to continue pursuing this line of research into COHERENT. It has also highlighted interesting aspects in such areas as the automatic synthesis of asynchronous circuits in general which further projects including the EPSRC funded BESST and MOVIE, both at NU, are pursuing.

We aim to improve and expand the library of known ACM solutions and data properties used to test ACM correctness.

Several M.Sc project placements at NU have been funded by the COMFORT project, these include Agnes Madalinski “Stochastic analysis of ACMs and priority arbiters” and Rene Krenz “Hardware implementation of a duplex communication channel”, proposed by the AMULET group at Manchester University and formally specified at NU. Both produced good and relevant results which benefited the project.

Although not funded from the COMFORT project, associated work has been done by Mustafa Jiffry (“Petri net approach for the analysis of MASCOT interprocess communications”, KCL PhD awarded Nov. 2000), Rosa Munoz-Calanchie (at KCL while on sabbatical leave from Dept. of Informatics, University of Santiago, Chile, “Formal description techniques for the analysis of MASCOT designs”, which includes application of LOTOS to real time distributed networks, PhD being written) and Marta Pietkiewicz-Koutny (“Relating Formal Models of Concurrency for the Modelling of Asynchronous Digital Hardware”, NU PhD awarded Oct. 2000).

The KCL PI has also had several opportunities to present invited seminars on the COMFORT research material at various overseas universities mainly as a by-product of travel on IEEE business. These visits included Monash University (Melbourne, Australia), University of Victoria (British Columbia), Simon Fraser University (Vancouver), University of Southern California, Stanford University, and were independently funded so that EPSRC resources were not used.

Collaboration with our industrial contacts at British Aerospace has been invaluable to this research and they have also contributed to it. We would especially like to thank Hugo Simpson and Eric Campbell, who continue to be active in this area.

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