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# Remote Plasma Atomic Layer Deposition of Strontium Titanate Films Using $Sr(iPr_3Cp)_2$ and $Ti(OiPr)_4$

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ITRS requirements beyond 2012 for DRAM are for EOT values lower than 0.4nm. With dielectric constant values >100, strontium titanate (STO) is a promising candidate material for use as dielectric in metal-insulator-metal (MIM) capacitors for next generations DRAM and for this purpose, it has been extensively studied in recent years [1, 2]. The three-dimensional structures required in order to obtain high capacitance values, make ALD the most suitable technique for these films. There have been a number of studies of both thermal (using $H_2O$ [3] and $O_3$ [4] as oxidants) and plasma [5] ALD of STO using different combinations of Sr and Ti precursors. We present results obtained for STO layers deposited at 250ºC by remote plasma ALD from $Sr(iPr_3Cp)_2$ and $Ti(OiPr)_4$.

STO layers with thicknesses ranging from 20 to 60nm were deposited in an Oxford Instrument FlexAL single wafer reactor and subsequently physically and electrically characterized.

XPS results showed that for the same ratio of SrO : $TiO_2$ cycles, stoichiometric STO layers, with C concentration below the XPS detection limit were obtained.

Spectroscopic ellipsometry (SE) results confirmed by X-ray reflectometry (XRR) showed that the ALD process for the stoichiometric layers is characterized by a growth per cycle (GPC) value of 1Å and when deposited on Si no incubation is observed (Figure 1).

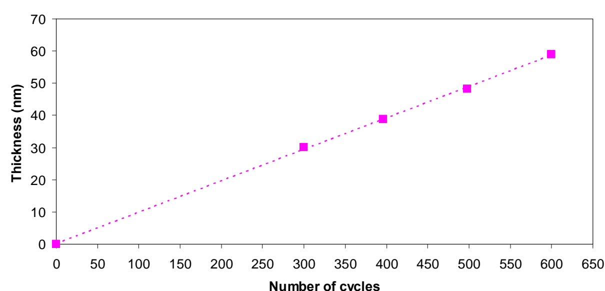


*Figure 1. STO thickness variation with number of cycles for deposition on Si.*

XRD measurements carried out on 45nm thick STO layers deposited on Si show that the as-deposited layers are amorphous. When subjected to a post deposition anneal (PDA) of 2min in $N_2$ (with 1min ramp-up), these layers crystallize at a temperature between 500 and 600ºC (Figure 2). Through crystallization the surface roughness of the layers increases, as expected (Figure 3).

The dielectric constant value extracted from CV measurements on Pt/STO/Pt MIM capacitor structures is ~ 36 for the as-deposited STO layers. IV measurements show very good leakage current density values for the as-deposited layers, ~ 1E-9A/cm$^2$.

The STO layers crystallized following PDA at 600ºC are characterized by a dielectric constant value >170, but also by a substantial increase in the leakage current density.

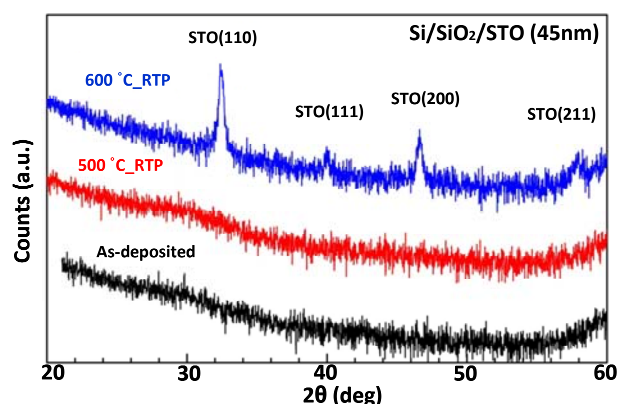


*Figure 2. XRD results obtained for 45nm thick STO layers deposited on Si, as-deposited and after PDA at 500ºC and 600ºC for 2min in $N_2$.*

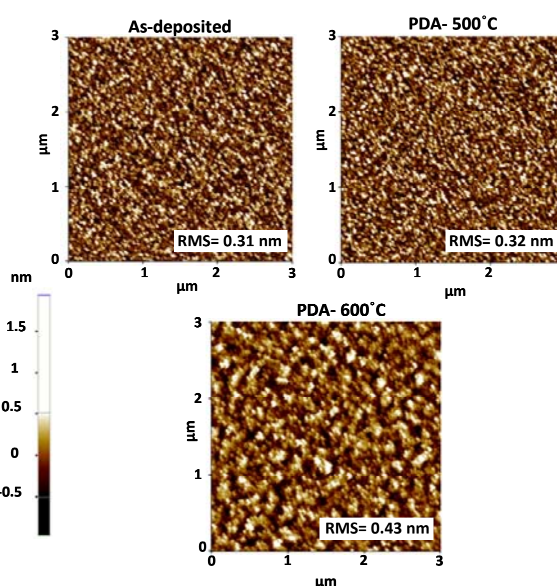


*Figure 3. AFM results showing the RMS of the surface roughness values obtained for 45nm thick STO layers deposited on Si, as-deposited and following PDA at 500ºC and 600ºC for 2min in $N_2$.*

Experiments designed to address the increase in the leakage current density of the crystallized STO layers are on-going.

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