Remote Plasma Atomic Layer Deposition of Strontium Titanate Films Using Sr(iPr3Cp)2 and Ti(OiPr)4
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ITRS requirements beyond 2012 for DRAM are for EOT values lower than 0.4nm. With dielectric constant values >100, strontium titanate (STO) is a promising candidate material for use as dielectric in metal-insulator-metal (MIM) capacitors for next generations DRAM and for this purpose, it has been extensively studied in recent years [1, 2]. The three-dimensional structures required in order to obtain high capacitance values, make ALD the most suitable technique for these films. There have been a number of studies of both thermal (using H2O [3] and O3 [4] as oxidants) and plasma [5] ALD of STO using different combinations of Sr and Ti precursors. We present results obtained for STO layers deposited at 250ºC by remote plasma ALD from Sr(iPr3Cp)2 and Ti(OiPr)4.

STO layers with thicknesses ranging from 20 to 60nm were deposited in an Oxford Instrument FlexAL single wafer reactor and subsequently physically and electrically characterized.

XPS results showed that for the same ratio of SrO : TiO2 cycles, stoichiometric STO layers, with C concentration below the XPS detection limit were obtained.

Spectroscopic ellipsometry (SE) results confirmed by X-ray reflectometry (XRR) showed that the ALD process for the stoichiometric layers is characterized by a growth per cycle (GPC) value of 1Å and when deposited on Si no incubation is observed (Figure 1).

The STO layers crystallized following PDA at 600ºC are characterized by a dielectric constant value >170, but also by a substantial increase in the leakage current density.

Experiments designed to address the increase in the leakage current density of the crystallized STO layers are on-going.


Figure 1. STO thickness variation with number of cycles for deposition on Si.

Figure 2. XRD results obtained for 45nm thick STO layers deposited on Si, as-deposited and after PDA at 500ºC and 600ºC for 2min in N2.

Figure 3. AFM results showing the RMS of the surface roughness values obtained for 45nm thick STO layers deposited on Si, as-deposited and following PDA at 500ºC and 600ºC for 2min in N2.