Lifetime Reliability Characterization of N/MEMS Used in Power Gating of Digital Integrated Circuits

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***Abstract*—Nano/Micro-Electro-Mechanical switches (N/MEMS) have recently been proposed for energy-constrained digital logic applications due to the leakage power limitations of CMOS transistors. Many investigatory research projects are currently exploring the potential use of these switches as the means of power gating devices of digital circuits. This is attributed to their zero-leakage energy compared to that of CMOS power transistors, especially when driving a large capacitive load. This paper investigates the operational limitations of N/MEM switches based power controlling elements. In particular, we model and study the impact of their switching frequencies capping, surface stress, and bending out of plane that are typical implications of lifetime reliability. Further, this paper proposes a new technique to mitigate the impact of contact bouncing and current rushing exhibited by N/MEMS on the power-gated CMOS circuits.**

A systematic optimisation of the N/MEMS parameters is performed using finite element analysis (FEA) in multiphysics COMSOL tool. Using these parameters a switch model simulator is built to simulate the mixed (CMOS+N/MEMS) electronics design. Finally, for validation a set of benchmark circuits have been simulated and evaluated. The final results revealed that our approach can reduce the impact of any potential reliability issues with 9% more energy saving compared to the previously reported approaches.

I. Introduction

Reducing power consumption is a primary requirement in embedded system to prolong battery operating lifetime. A key enabler of low power design is technology scaling coupled with multi-V_{dd} operation. However, continued technology scaling has consistently increased the leakage power consumption and power density per unit area. Therefore, a large proportion of today's system-on-chip (SoC) has to be powered off so that it can still operate within its given power budget due to the "dark silicon" phenomenon [1] [2]. As a result, it is believed that the mainstream of future electronics design in some emerging applications is to shift from performance-driven goals to energy-constrained ones. However, this presents a fundamental challenge in achieving energy efficiency, as the leakage energy continues to grow exponentially.

One of the key opportunities to mitigate leakage energy is during standby periods, when no computation occurs. The microprocessor industry has widely adopted power gating techniques coupled with software-controlled sleep modes in such applications exhibiting substantial idle periods [14] [15].

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Table I: Features of the N/MEMS based power gating approaches.

Approach	Application	Design abstraction	Key method
[3]	low duty cycles asynchronous implementations	Function blocks	Power gating, FIR filter
[4] [5]	Bursty applications	Function blocks+system	Power delivery control for bursty applications
[6] [7]	Controlling power to integrated circuit (IC)	System	Fabrication of MEMS on top of CMOS layer
[8]–[13]	Highly periodic and event-driven processing, baseband processor, and battery operated systems	Function blocks+ system	Theoretical analysis showed N/MEMS achieve upto $\times 10^3$ energy saving compared to that of CMOS counterparts
Proposed	Low duty cycle, adiabatic implementation	Function blocks+ system	3D FEA using COMSOL, power gating+clock gating, mixed electronic simulator , reliability test, voltage supply design

With this technique, transistors are used to disconnect the power from unused sections of a microprocessor, which reduces the leakage power. This approach is attractive because it mitigates leakage without requiring any modification to the logic or power-gated circuitry. However, sleep transistors themselves contribute high-leakage current, especially when driving a large capacitive load. Therefore, many research works have recently proposed using of N/MEMS to completely eliminate leakage power consumption, as shown in Table I.

Results of the published approaches in Table I demonstrate that a greater energy saving can be achieved compared to CMOS power switches. However, the limitations and drawbacks of using N/MEM switches have not been investigated in the previous works. These include, firstly, the impact of contact oscillations on the connected CMOS devices. Secondly, the effect of any spurious actuation due to environmental vibrations on the functionality of the integrated circuits. Lastly, the previous studies are either based on theoretical demonstrations [8], or lack of practical model and simulation environment [9]. Therefore, a novel work based on 3D FEA exercised on COMSOL multiphysics simulation tool is presented to target applications which exhibit low duty cycles.

Despite its promises, the full-scale implementation for power gating remains unresolved due to engineering challenges such as evolving N/MEMS parametric optimization and interaction with power-gated circuits. In this paper, we also

Table II: Key characteristic of N/MEMS actuation characteristics.

MEMS	Piezoelectric	Electrostatic	Magnetic	Thermal
Fast switching	(✓)	(✓)	(∼)	(∼)
Simple fabrication	(✗)	(✓)	(✗)	(✓)
Low pull-in voltage	(✓)	(✓)	(✓)	(✓)
Bias current [μA]	(✓)	(✓)	(✗)	(✗)
Low power	(✓)	(✓)	(✗)	(✗)
High force	(✓)	(✗)	(✓)	(✓)
Scalability	(✓)	(✓)	(✗)	(✗)

investigate the characteristics of the voltage supply that can be used for N/MEMS implementations to reduce high peak-power and current spikes. In our proposed approach, we make the following main *contributions*:

- investigate power supply design for N/MEMS implementations to achieve reliable circuit operation,
- build a Verilog-AMS based N/MEMS mode simulator to study the impact of mixed electronic design,
- investigate lifetime reliability characterization of various N/MEMS,
- show a novel systematic optimization of N/MEMS parameters using finite element analysis (FEA) in multi-physics COMSOL tool, and
- validate using a number of benchmarks to show the comparative advantages and trade-offs of our approach.

To the best of our knowledge, this is the first approach that investigates (a) a systematic optimization of N/MEMS-based relay through parametric sweep in COMSOL tool, (b) reliability characteristics and limitations of N/MEMS based power gating implementations. The rest of this paper is organized as follows. Section II gives the background of N/MEMS devices. Section III shows modelling approach of N/MEMS, and energy-latency optimization by using finite element analysis (FEA) method. The N/MEMS reliability characterization is described in Section IV. Verilog-AMS switch model simulator based on 3D FEA is illustrated in Section V. Experimental results are presented in Section VI. Section VII concludes the paper.

II. Background

In this section we briefly introduce Nano/micro-elecromechanical switch (N/MEMS), which is used to control power gating in our approach. Due to recent advances in planar fabrication process, mechanical computing has been revived for energy-constrained applications [5], [16], [17]. Typically, N/MEM relays can be classified, based on the method of actuation into electrothermal, magnetostatic, electrostatic, and piezoelectric. Each type of actuation scheme has specific drawbacks and advantages as listed in Table II. It can be deduced from Table II that the electrostatic actuated N/MEMS is attractive candidate for digital logic applications due to its scalability, low active power consumption, fast switching, and ease of manufacture using conventional planar processing techniques [16]. Alternatively, they could also be classified according to the contact interface (ohmic or capacitive), axis of deflection (lateral, vertical), and geometric shape (cantilever beam (CB), see-saw beam (SS), clamped-clamped beam (CC), dual bridge (DB), sidewall perimeter beam (SW), parallel plate (PP)). Table III summarises the

Table III: key Features of the fabricated N/MEM relays.

Ref.	No.	Ge.	A.D	Life span	C.R(Ω)	Es(pJ)
[3]	4	PP	V	NR	NR	1
[16]	4	PP	V	2.1× 10^9	1.4k	1.8
[17]	3	CB	L	NR	5K	0.082

key features of various N/MEM switches. These features including the geometric shape (Ge.), number of terminals (No.), actuation direction (A.D), life span, contact resistance (C.R), and switching energy (E_s). In the present work, for coherent comparison analysis, relays in Table III are simulated using the COMSOL multiphysics tool with comparable footprint size (see Section III).

Their principle of operation, in general, can be summarised as in Fig. 1: when the gate-body voltage increases above the "pull-in voltage" ($|V_{gb}| \geq V_{pi}$), a contact dimple touches the source and drain terminal, causing the current to flow. The electrical contact is broken when the gate-body voltage decreases below the "pull-out voltage" ($|V_{gb}| \leq V_{po}$).

III. MEM Relay Modelling

Finite element analysis (FEA) is a numerical analysis method used to solve large number of partial differential equations (PDEs) for any design. This method is capable of handling multiphysics phenomena and accurately simulating static and dynamic behaviour. To model and capture the physical behaviour of MEMS accurately, COMSOL multiphysics tool has been used in our work. Fig. 2(a) shows the simulated pull-in voltage by using FEA, while Fig. 2(b) depicts the adopted MEMS in our analysis.

An extensive parametric sweep simulation is performed to estimate the range of electo-mechanical parameters, as shown in Table IV, thereby energy-latency of N/MEMS can be optimised. In order to obtain a precise analytical formula of pull-in voltage, which is used in Section (IV), sensitivity analysis coupled with parametric sweep have been performed. As a result, our analytical model of evaluating pull-in voltage at various gaps demonstrates a close fit to the one obtained from FEA, as shown in Fig. 3.

$$V_{pi} \simeq \sqrt[2]{\frac{\beta \times Lg^3}{\varepsilon_0 WA}}; \beta = 3.87 \times 10^{-4}. \quad (1)$$

The following section describes how to evaluate energy-latency trade-offs:

A. Structural Stiffness

The structural stiffness of N/MEM relays subjected to an electrostatic force is modelled using FEA. In this paper, It

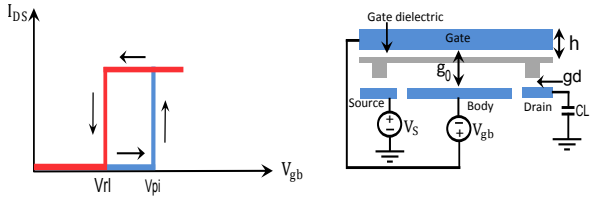

Figure 1: Cross-section of N/MEMS with its V_{gb} vs. I_{ds} curve.

Table IV: Current and scaled MEM relay physical parameters based on COMSOL multiphysics tool.

MEMS Area (um^2)	Pull-in voltage(v)	Switching energy (pJ)	Mechanical delay(μs)	Stiffness (N/m)	Mass (pg)	Damping (μN.s/m)	Actuation gap(nm)	Actuation Capacitance(fF)
450 (existed)	11.3-2.6	0.1-3.2	0.15-0.69	10.14-192.6	1.1-2.9	50	200	40
45 (NEMS)	0.19-1.97	0.049-0.003	0.06-0.28	5.51-68.2	0.15-0.25	0.07	40	17
4.5 (NEMS)	0.1-0.31	(0.037-0.36)$\times$ 10^{-3}	(24-85)$\times$ 10^{-3}	0.15-1.51	(3-3.77)$\times$ 10^{-3}	0.007	20	3.54

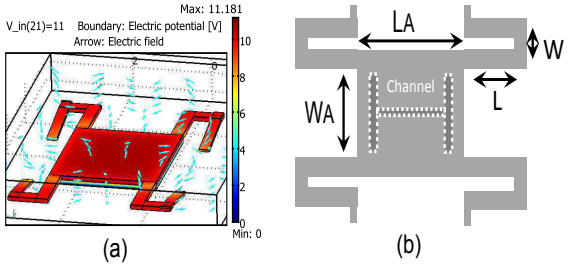

Figure 2: Demonstrates the: (a) FEA-simulated pull-in voltage; (b) simplified sketch, symbols L, W, LA, and WA denote, respectively, spring (length/width), and actuation area (length/width) [16].

is assumed that MEMS exhibit a linear elastic deformation. To solve coupled problems with complex geometry, Arbitrary Lagrangian-Eulerian (ALE) was used by the COMSOL tool to obtain the equilibrium point between electrostatic force and mechanical structure. This method diverges as the N/MEMS displacement approaches the pull-in point. This is attributed to the fact that this is the last point where behind it N/MEMS collapses non-linearly. At this point, electrostatic force equals to the spring restoring force. Having calculated the pull-in voltage (V_{pi}) and correspond displacement (Z) by the COMSOL tool, the structural spring constant can be calculated as follows:

$$F_{ele.}\,|_{pullin} = F_{spring} \Longrightarrow k\,|_{structure} = \frac{V_{pi}^2}{2Z}\frac{\partial C(Z)}{\partial Z} \quad . \quad (2)$$

B. Damping Analysis

Squeeze film damping is the most affecting damping component on the dynamic behaviour of N/MEMS, especially at low ambient pressure [18]. Estimate damping components of N/MEMS is strongly demanded for accurate analysis, especially at nanoscale size. This is attributed to the fact that the rarefied air in the gap damps the movements of the mechanical parts. Consequently, it significantly influences the switching time, mechanical quality factor, and impact bounce of contacting. Generally, squeeze film damping consists of viscous and electrical damping. Electrical damping due to air compression is often underestimated especially at nano-scale geometry, therefore it has been neglected in our analysis. Viscous damping is modelled using Rayleigh damping by COMOSL tool as:

$$2\zeta_n\omega_n = \alpha_{dM} + \beta_{dK}\omega_n^2 \quad , \quad (3)$$

where α_{dM} dampens low frequency response and β_{dK} dampens high frequency response, ω_n represents natural frequency, and ζ is damping ratios ($\zeta = \frac{1}{2Q}$).

For digital logic applications it is preferable to set $Q = \frac{\sqrt{mk}}{c}$ factor ≤ 1, to avoid non ideal switching effect such as long settle time and contact bouncing. Fig. 4 indicates that increasing damping coefficient resulting in a corresponding reduction in the N/MEMS contact damping and bouncing.

C. Energy-Latency Analysis of N/MEMS

An extensive parametric sweep simulation is performed using the COMSOL multiphysics tool, in this work, to estimate the range of electro-mechanical parameters for both fabricated 450um^2 and scaled 45um^2, and 4.5um^2 relays respectively, thereby energy-latency trade-offs of N/MEMS can be optimised. These parameters can be seen in Table IV.

The result in Fig. 5 (a) shows the switching energy consumption of N/MEMS by using 3D FEA as a function of the dimple gap (g_d), and resonant frequency (w). As can be seen, increasing (g_d) causes an almost linear increase in switching energy at low (w). Alternatively, switching energy increases exponentially with increasing resonant frequency (w) by sweeping the ratio of (L/W), at high (g_d). Fig. 5 (b) shows the simulation results of mechanical delay time as a function of the gap ratio (g_d/g_0), and resonant frequency (w). One

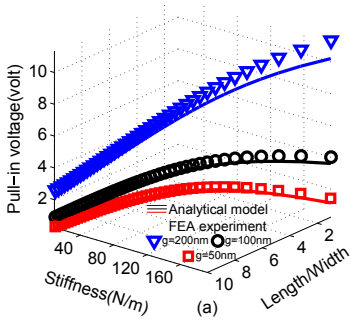

Figure 3: A comparison of the pull-in voltage for three different gaps obtained from full finite element model and the analytical model.

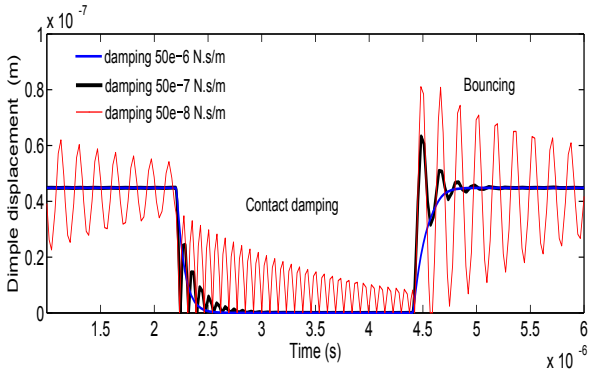

Figure 4: Impact of increasing structure damping coefficient on bouncing and contact damping based 4-terminal MEMS, A=450um^2, g_0=200nm, g_d=40nm, stiffness=150N/m, mass=0.29$\times$ 10^{-10}kg.

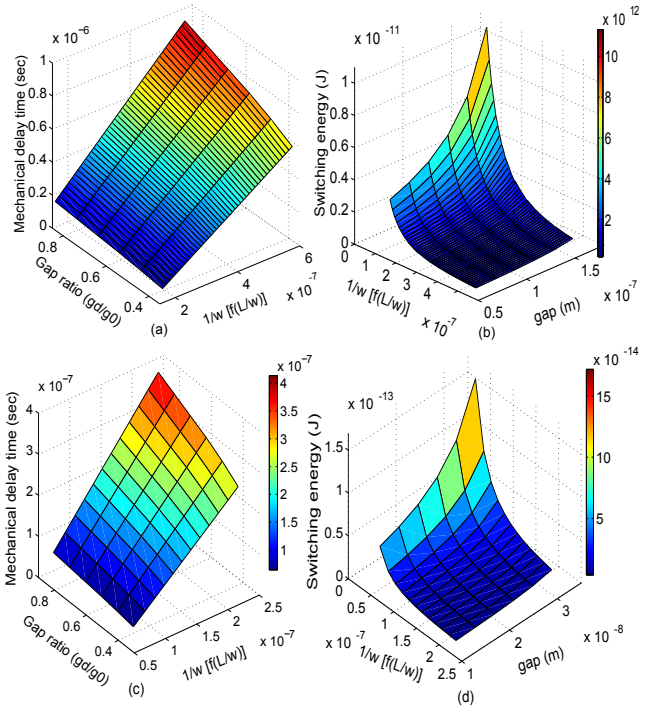

Figure 5: Illustrates that: (a) switching energy based FEA at g_0=200nm and A=450um^2 as a function of g_d and resonant frequency (w); (b) $T_{mech.}$ as a function of gap ratio and resonant frequency obtained from 3D FEA at A=450um^2; (c) $T_{mech.}$ of the scaled relay at g_0=40nm and A=45um^2 as a function of g_d and resonant frequency; (d) switching energy of the scaled relay.

observation which can be made is that T_{mech} is inversely proportional to (w), and it is linearly proportional with the increase in (g_d/g_0), which is consistent with the theoretical predictive analytical equation in the previous study [19].

Fig. 5 (d) demonstrates a significant reduction in the switching energy of the scaled MEMS. Furthermore, these results clearly indicate a better trade-off between switching energy and mechanical delay time compared to that of the fabricated MEMS (A=450um^2). As an example, it is found that at, (g_d/g_0)=0.5, every $\sim 5\times$ increase in switching energy can be trade-doff for a $\sim 5\times$ reduction in the scaled delay, as can be seen in Fig. 5 (c-d).

IV. N/MEMS Reliability Characterizations

Reliability assessment of the N/MEMS has been investigated in the context of the harsh environment impact [20], contact resistance stability [21] [22], and contact adhesion impact [23]. This section, in contrast, will mainly focus on the reliability characterization and limitations of using N/MEM relays as a power control switches of the integrated circuits. Furthermore, the key criteria for using N/MEM relays without exhibiting any operation failure in the power-gated digital circuits also have been investigated in this paper.

A. Natural and resonant frequency

The natural and resonant frequencies of N/MEMS are modelled by solving the 3D FEA models in the COMSOL tool with the frequency response solver. The frequency when the system vibrates naturally once it has been set into motion is called

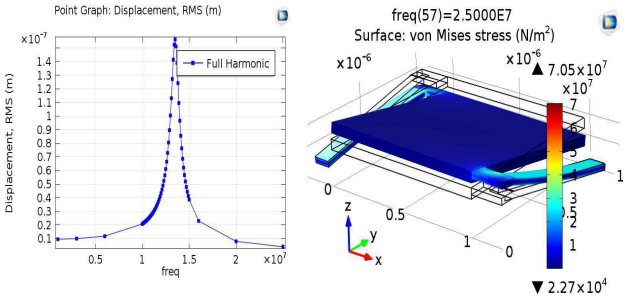

Figure 6: Resonant frequency of the 2-spring N/MEMS.

the natural frequency. The calculated natural frequencies using COMSOL tool of the relays in [3], [16], and [17] are equal to 1.2×10^6Hz, 146×10^6Hz, and 179×10^6Hz, respectively. These values of frequencies represent the maximum allowable power gate switching as the N/MEMS will oscillate beyond these frequencies, thereby causing an operation failure. For demonstration purposes, Fig. 6 shows the displacement versus resonant frequencies for the 2-spring MEMS. It is clearly shown that as the natural frequency is approached, which is equal to 13×10^6Hz, the MEMS will vibrate and bend out of plane. It should be noted that for coherent analysis, these relays are simulated with comparable footprint size of 450 μm^2.

B. Surface Stress

In this paper, a comparative study has been conducted to understand the surface stress impact. Our findings show that the MEMS in Fig. 7(b) suffers from high surface stress compared to the others. The MEMS in Fig. 6 and 7(a) exhibit the lower surface stress due to its anchor shape at the expense of high pull in voltage. Although the MEMS in Fig. 2 shows a moderate surface stress with lower pull in voltage, it has been selected in our simulation, Section VI, due to its high measured on/off life span compared with the others.

C. Contact Damping/Bouncing

An accurate estimate of bounce dynamics, the amount of time during and between bounces, is important to predict delay. Furthermore, it is necessary to prevent any operation failure of the power-gated circuits that may happen when heigh current is passed in the on-state followed by no current as the relay floating. In the literature, it is suggested to investigate the designing of supply voltage for N/MEMS implementation due to the mentioned drawbacks [10]. To mitigate the impact of current rushing, i.e unlike CMOS transistor V_{gs} of N/MEMS is linearly proportional to the I_{ds}, and bouncing impact, a ramped supply voltage technique is proposed. Fig. 8(a-b) illustrates that to avoid any operation failure the condition of $\tau_{mech.}$+τ_{stable} << $\tau_{evaluate}$ must be met. Therefore, Fig. 8(b) illustrates that as the contact bouncing exceed $\tau_{evaluate}$ the power-gated circuits would experience an operation failure, as can be described in Section VI.

V. Switch Model Simulator Based on (FEA)

Although switch mode simulators using Verilog-AMS have been investigated in [24] [25], these are either based on

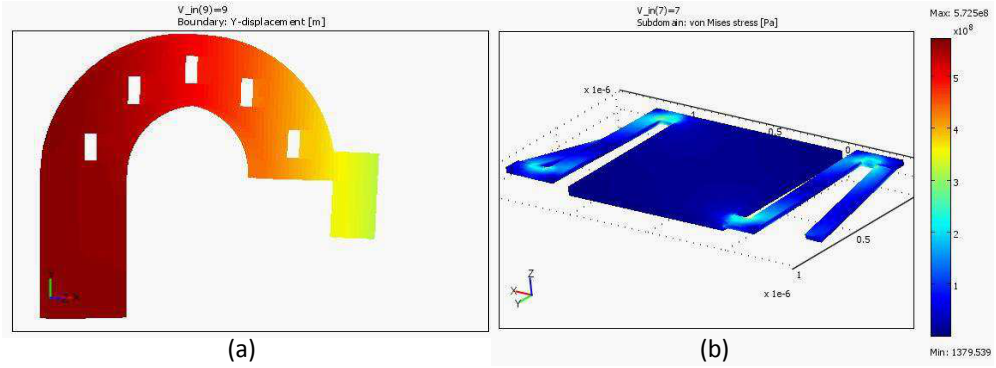

Figure 7: 3D FEA illustration shows surface stress of: (a) anchor MEMS [17]; (b) 4-terminals with double spring MEMS [3].

predicted parameters or lack the ability to simulate any customized N/MEMS. Fig. 9 shows the hierarchical structure of our proposed switch model simulator, which is based on the lumped N/MEMS parameters. It is clearly shown that lumped electrical parameters are either based on the fabricated MEMS (A=450 um^2) or predicted NEMS [16]. Alternatively, lumped mechanical parameters are evaluated by using 3D FEA, which is performed in the COMSOL multiphysics tool. As can be seen, at each gate voltage (V_g) step, the F_{ele} and F_{vdw} are evaluated by the simulator. As a result, the corresponding displacement (Z) of the gate terminal is generated and used as feedback of a new input to the design. This process is iterated until the dimple touches the drain-source terminal.

This simulator is characterized by the ease of simulation of various technology sizes by performing sensitivity analysis coupled with the parametric sweep. This can be achieved by using (1) to evaluate the accurate spring constant at any given ratio of ($\frac{L}{W}$). Other mechanical parameters, such as effective mass and damping coefficient, can be evaluated by using the same methodology within the COMSOL tool [26].

VI. Proposed Reliable Approach and Experimental Results

A. Proposed design

Typically, power gating circuitry uses power switches (P_{sw}) to shut-off the leakage current when the circuits enter into a sleep mode. This technique is expanded to utilize the clock signal to control turning on/off the power switches (P_{sw}). Fig. 10 (a)-(c) illustrate that the P_{sw} are fully turned on only at each half clock cycle. This means that outer power (∅=V_{dd}) is provided to the circuit every half clock cycle. Consequently, a ramp V_{sw} voltage is generated when the clock signal transits from low to high. Using this supply voltage leads to a greater energy saving as the transferred energy is governed by E=2R$C^2V_{dd}^2$/T. This attributes to the fact that a longer T, slower charging of the load capacitance, will lead to less energy dissipation. This approach is widely used in the adiabatic digital circuit. Fig. 10 (b) depicts the 3D schematic view of the mixed N/MEMS-CMOS electronic design with supply voltage of V_{dd}=0.6V. Table V illustrates the total energy consumption of the 32-tap FIR filter implemented at various data rates.

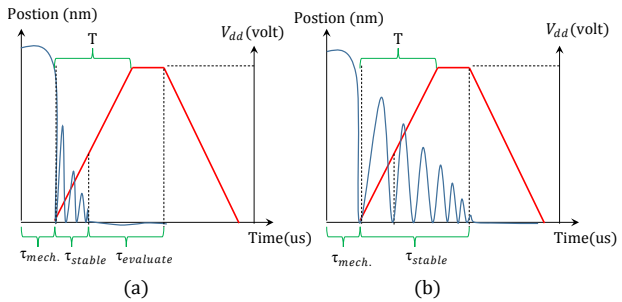

Figure 8: Contact bouncing impact when using ramped V_{dd} (a) safe bouncing; (b) unstable bouncing cause operation failure of power-gated circuits.

B. Experimental Results

Our approach was evaluated and compared with different configurations in previous work. All these configurations are supplied by various power domain and data rates. The total energy consumption of each configuration as well as the overall energy overhead of the proposed approach caused by adding N/MEMS and the charge pump were evaluated. In our experiment a complex combinational circuit, such as 32-tap FIR filter, is used. This is because, unlike CMOS power switch

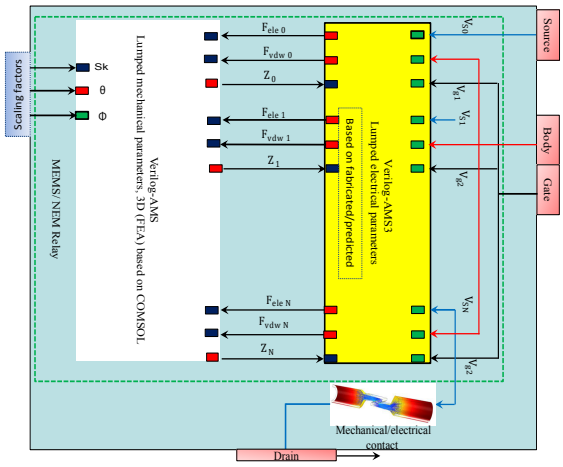

Figure 9: Graphic illustration of the hierarchical model of the switch simulator. The highlighted regions represent the electrical and mechanical lumped parameters, which is written in Verilog-AMS and co-simulated in The Spectre spice tool.

Table V: Energy consumption for 32-tap FIR filter at various asynchronous PG setups.

	No PG	With CMOS PG		With MEMS PG [3]		Proposed PG (MEMS)		
Data-rate(KHz)	Energy (nJ)	Total energy (nJ)	Saving (%)	Total energy (nJ)	Saving (%)	T (μs)	Total energy (nJ)	Saving (%)
1	6.778	4.10	39.5	2.10	69.0	250	1.48	78.0
10	0.80	0.49	38.0	0.30	62.5	25.0	0.232	71.0
100	0.60	0.41	31.0	0.31	48.3	2.50	0.258	57.0
400	0.45	0.38	15.0	0.315	30.0	0.625	0.27	40.0
800	0.389	0.35	10.2	0.32	17.7	0.125	0.311	20.0
1000	0.34	0.345	-1.4	0.32	5.80	0.25	0.312	8.0
10000	0.3	0.38	-26.0	0.45	-50.0	0.025	0.432	-44.0

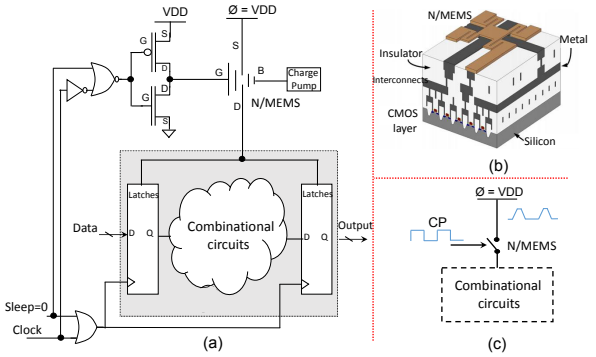

Figure 10: Illustrates that (a) proposed architecture; (b) 3D schematic of N/MEMS integration with CMOS circuitry; (c) operation principle.

[27], N/MEMS favour a complex design architecture coupled with low duty cycle implementations. It should be noted that our proposed approach only differs from [3] by using a ramp supply voltage with various T. These results indicate that at low data rate our approach can achieve greater energy savings by about 9% compared to the previously reported results. This can, firstly, be attributed to completely cutting off the leakage dissipation during the idle state. Secondly, the dynamic energy of the FIR filter is significantly minimized due to mitigation of the contact bouncing and current rushing by slow charging of the load capacitance. However, increasing the data rate will lead to increase switching energy of the MEMS-based power gating, which outweigh its leakage power savings, as shown in Table V. It should be noted that in this experiment the damping coefficient was chosen to be equal to 50×10^{-7}N.s/m. Reducing the damping coefficient to 50×10^{-8}N.s/m has led the simulator to diverge, hence no useful results are obtained due to the large bouncing time (floating).

VII. Conclusion

We presented an investigation into lifetime reliability issues of N/MEMS based power controllers of digital integrated circuits. This study demonstrated the limitations at which N/MEMS can be adopted without any potential failure of the power-gated circuits. Furthermore, this study showed the threshold at which N/MEMS can achieve greater energy saving compared to that of CMOS transistor.

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