Analogue-Asynchronous Co-design for On-Chip Machine Learning

[A 4-year fully-funded industrial CASE PhD fellowship – suitable for candidates from all nationalities]

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Project Summary

Newcastle Microsystems Research Group is widely known for its international leadership in autonomous and self-timed systems design. Over the years, the group has generated top-tier scholarly publications, taped out numerous microchips and attracted major funding from national and international sources with significant impact.

This project, jointly funded by Engineering and Physical Sciences Research Council (EPSRC) and HiSilicon, is looking for an ambitious and aspiring postgraduate researcher to join the team members working on new machine learning circuits and systems.

Machine learning algorithms capable of training and making decisions on the microchip are increasingly becoming popular for new electronic applications at the micro-edge. However, for realising this on-chip capability – there are conflicting design challenges involving performance and energy consumption. The data pre-processing routines coupled with the machine learning algorithms in these systems require at-speed performance with a large volume of data. Using traditionally clocked digital designs for achieving this performance is challenging due to high computational complexity and subsequently large energy consumption.

Asynchronous design methods are known for their flexibility of event-driven controls, precluding complex clock-based management hierarchies. These methods are ideally suited for interfacing analogue circuits, such as those in data pre-processing routines, that have long been known for poor controllability over their functional correctness despite high-speed and ultra-low-power.

This project will develop a new methodology for designing low power and high-speed analogue systems with asynchronous circuits used as control for analogue parts (i.e. data pre-processing circuits) and as front-end for mixed signal interfaces (i.e. interfaces between data pre-processing and machine learning routines implementing Tsetlin Machines). By processing data analogously and on-demand using a sequence of coordinated events, our aim is to significantly cut down the computational costs of on-chip training/inference and enable at-speed performance. Our aim is to design a prototype system-on-chip and relevant libraries that will be demonstrated for a number of on-chip machine learning use cases.

Novel Challenges

The novel research challenges this project will address are:

Challenge 1: *Controllability and Concurrency*: Managing functional correctness under varying power levels is challenging for analogue circuits. We aim to address this by developing tools that can embed suitably chosen event-driven interface circuits and determine their timing boundaries appropriately for better controllability.

Challenge 2: *Compositionality*: Designing analogue circuits into micrograniular blocks will provide a high level of controllability with significant overheads. Conversely, designing larger analogue blocks exhibits poor controllability properties with reduced overall overheads. As such a key challenge is to identify suitable analogue-asynchronous compositionality for balancing the performance and energy tradeoffs.

Brief Work Plan

The following research will be undertaken over the 4 years:

Year 1: Using our in-house software along with standard electronic design automation tools we will architect high-speed front-end for encoding real-world analogue data into digital form with in-situ asynchronous controls.

Year 2: Using the analogue-to-digital converters, we will design new generation of data encoding units that are highly configurable and suited for new logic-based Machine Learning algorithm co-pioneered by our group.

Year 3: We will integrate data pre-processing with Machine Learning algorithms for enabling a number of on-chip learning use case scenarios. These scenarios, once validated, will allow us to investigate further architectural leverages required for the scalable machine learning System-on-Chip designs.

Year 4: A prototype System-on-Chip will be validated and then sent for fabrication. The experimental results will be written up with relevant details in the form the PhD dissertation.

Our research above will provide opportunities for circuit/microchip designs as well as reporting their results in several major publications, eventually leading to the final dissertation. Example avenues of publications include, Nature Electronics, IEEE Journal of Solid State Circuits and IEEE Transactions on Computers.

PhD Candidate Requirements

This is a well-funded and prestigious, 4-year PhD position. Students from any nationality can apply.

Ideally the candidate is expected to have a MSc/MEng degree with 2:1 minimum – however, candidate with a BEng degree and outstanding academic credentials and some industrial experience is equally acceptable. There must be a strong commitment to innovation and scholarly activities, such as attending conferences, writing journal/conference articles and presenting to technical/non-technical audience. The candidate is also expected to be hard working and an ambitious individual.

Some prior industrial experience in hardware design is desirable but not essential.

The student will be working with the supervisory team primarily. Should there be a need, professional training will be arranged for improving the candidate's skills and capabilities, e.g. hardware design, Verilog, EDA tools, Python, C/C++.. Also, the candidate is expected to work in a team of researchers who are contributing to different aspects of Machine Learning and Pervasive Systems Design research. As such, good interpersonnel skills are essential.

How to Apply

You must apply through the University's online postgraduate application system. You will need to:

1. Insert the programme code **8060F** in the programme of study section
2. Select **'PhD Electrical and Electronic Engineering (full time) - Computer Engineering'** as the programme of study
3. Insert the studentship code **ICASE211** in the studentship/partnership reference field
   attach a covering letter and CV. The covering letter must state the title of the studentship, quote reference code **ICASE211** and state how your interests and experience relate to the project
4. Attach degree transcripts and certificates and, if English is not your first language, a copy of your English language qualifications

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